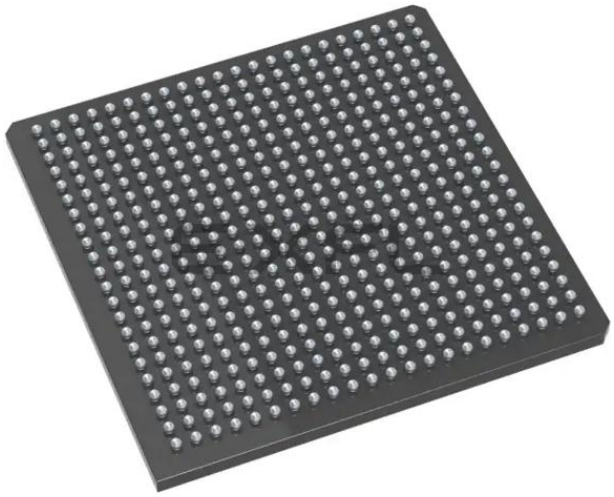

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 110592 |
| Number of I/O | 172 |
| Number of Gates | 600000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/afs600-fg484 |

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.

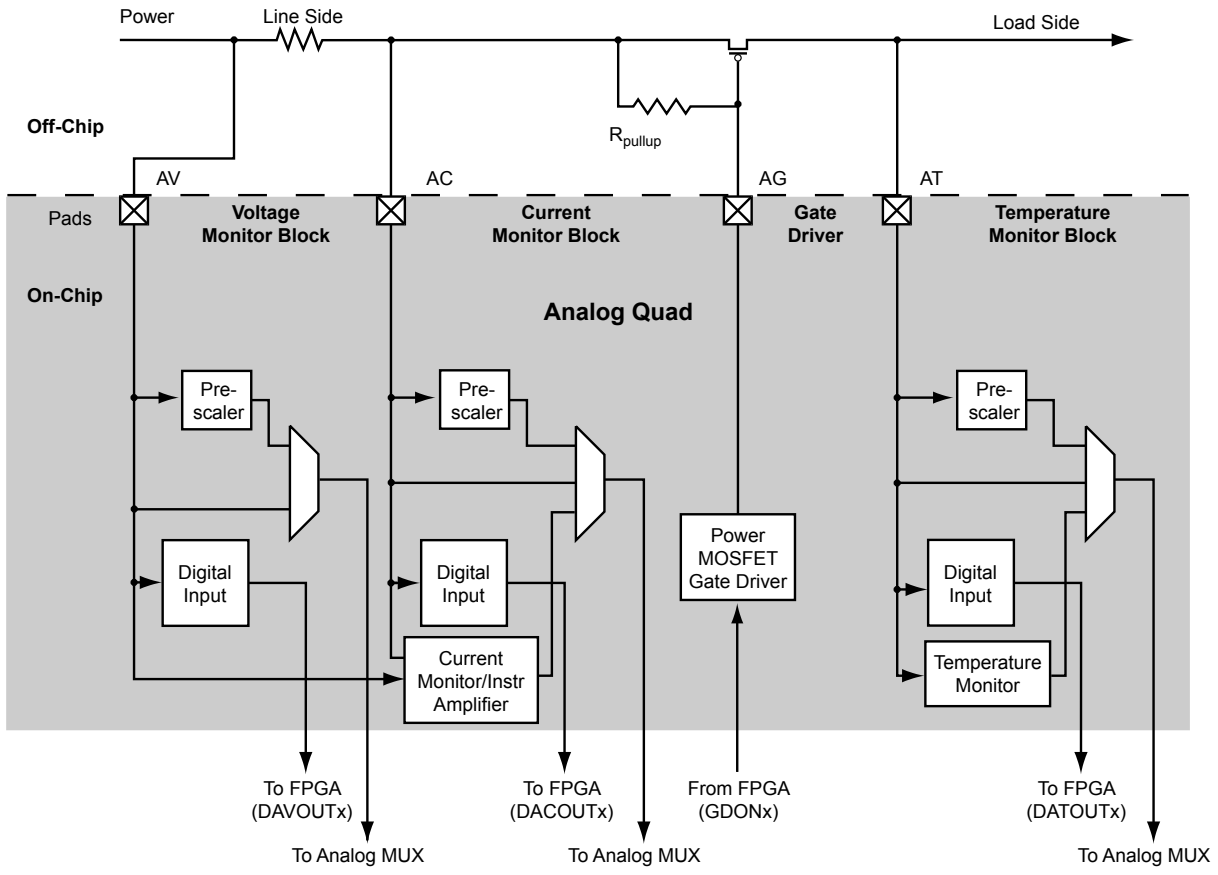



***Figure 1-1 •*** **Analog Quad**

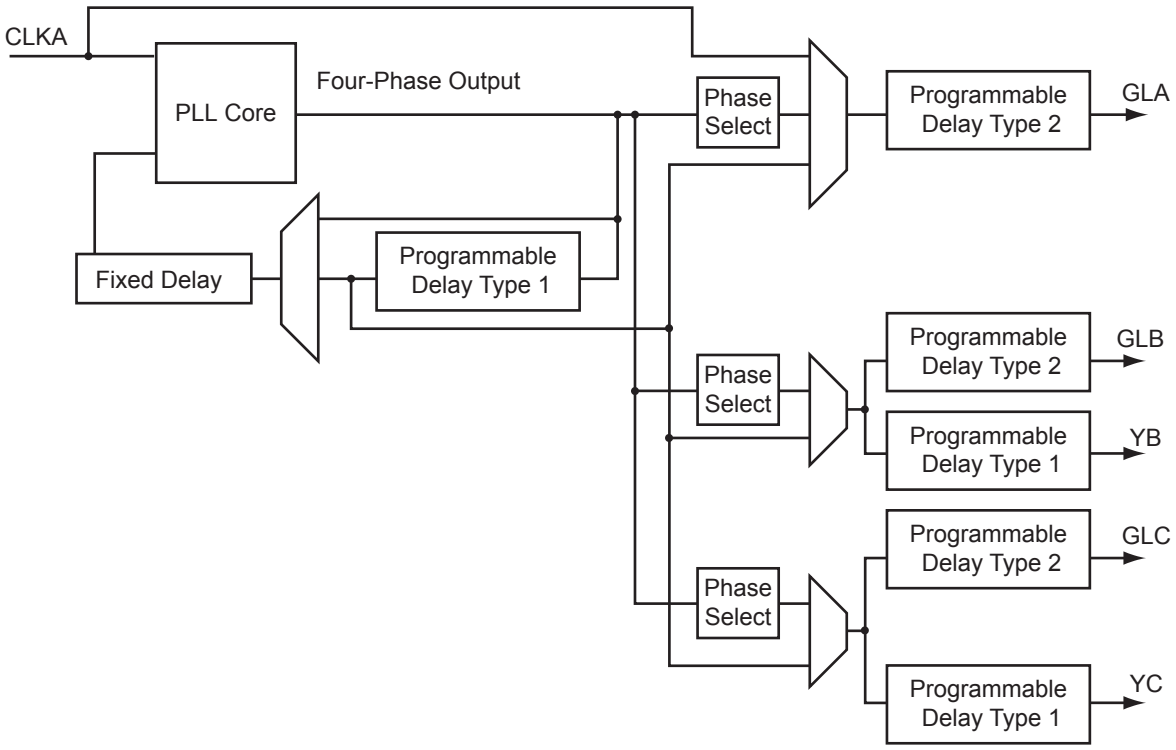
## CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

### CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.




*Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.*

***Figure 2-23 •*** **PLL Block**

## No-Glitch MUX (NGMUX)

Positioned downstream from the PLL/CCC blocks, the NGMUX provides a special switching sequence between two asynchronous clock domains that prevents generating any unwanted narrow clock pulses. The NGMUX is used to switch the source of a global between three different clock sources. Allowable inputs are either two PLL/CCC outputs or a PLL/CCC output and a regular net, as shown in Figure 2-24. The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). These are set by SmartGen during design but can also be changed by dynamically reconfiguring the PLL. The GLMUXSEL[1:0] bits control which clock source is passed through the NGMUX to the global network (GL). See Table 2-13.

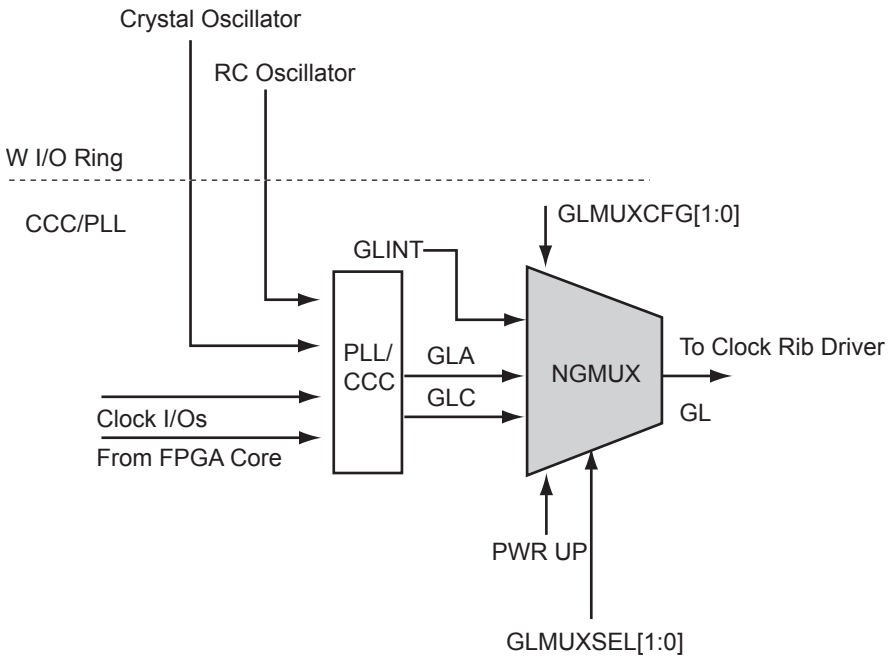



***Figure 2-24 •*** **NGMUX**

***Table 2-13 •*** **NGMUX Configuration and Selection Table**

| GLMUXCFG[1:0] | GLMUXSEL[1:0] | | Selected Input Signal | MUX Type |
|---|---|---|---|---|
| 00 | X | 0 | GLA | 2-to-1 GLMUX |
| | X | 1 | GLC | |
| 01 | X | 0 | GLA | 2-to-1 GLMUX |
| | X | 1 | GLINT | |

### Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-37.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')

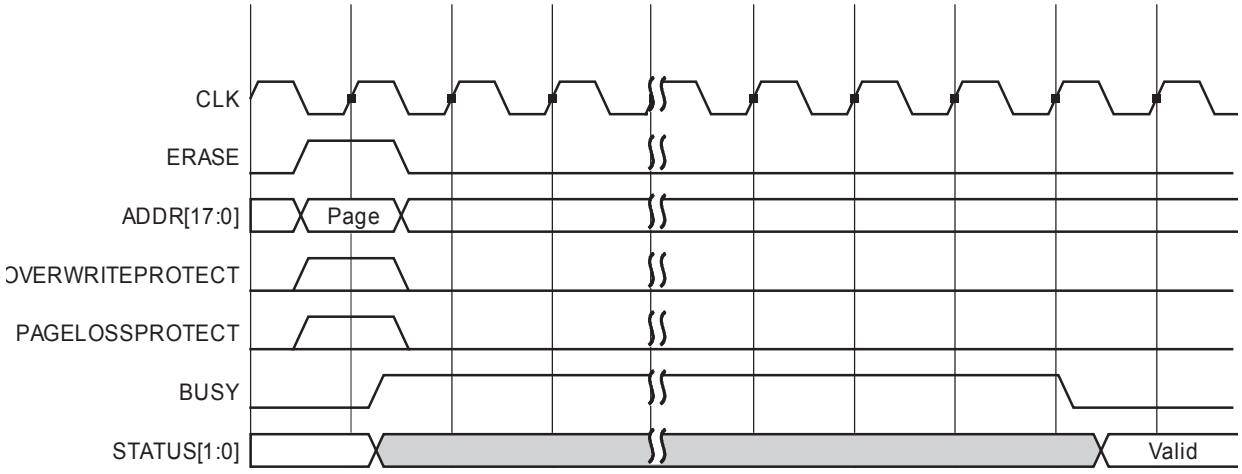



***Figure 2-37 •*** **FB Erase Page Waveform**

### Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-40 and Figure 2-41.

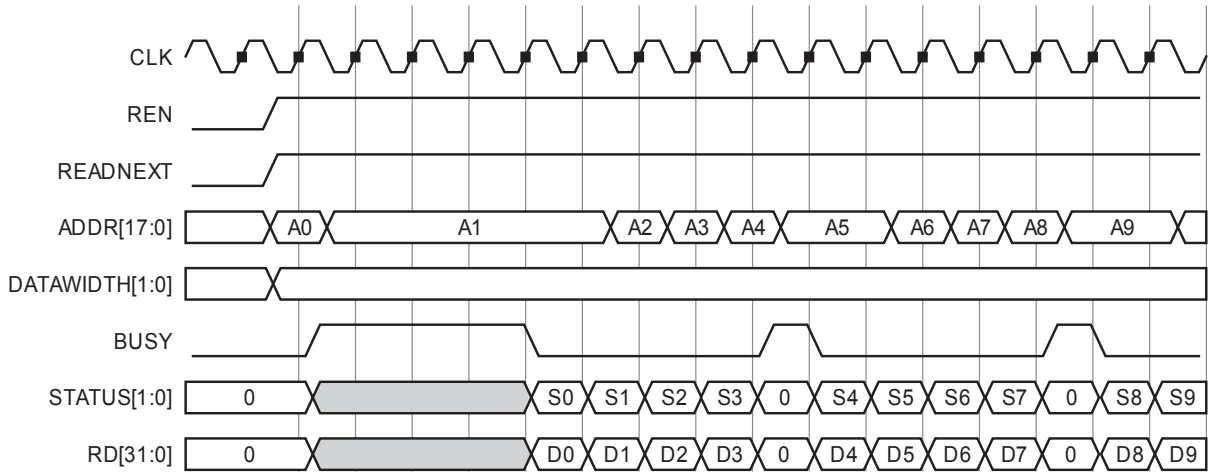



***Figure 2-40* • Read Next Waveform (Non-Pipe Mode, 32-bit access)**

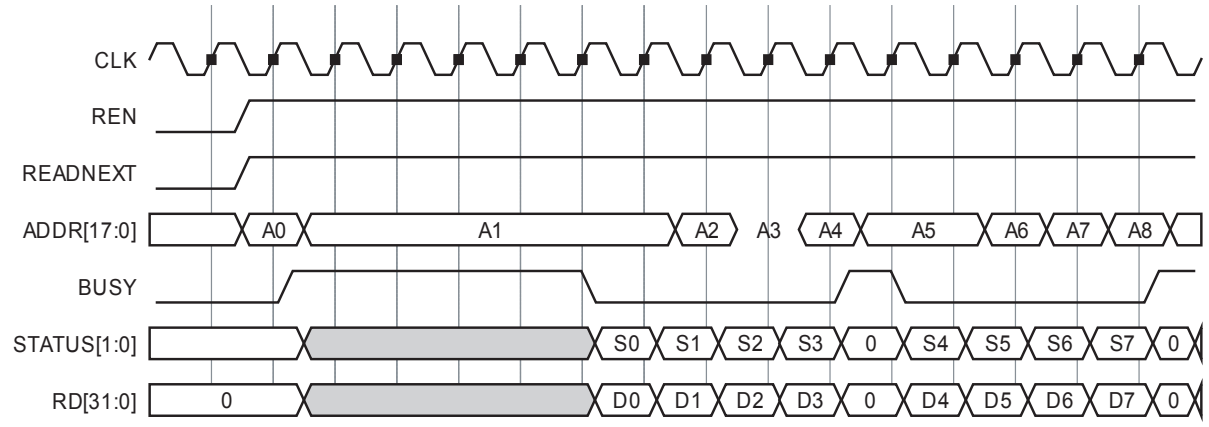



***Figure 2-41* • Read Next WaveForm (Pipe Mode, 32-bit access)**

There are several popular ADC architectures, each with advantages and limitations.
The analog-to-digital converter in Fusion devices is a switched-capacitor Successive Approximation Register (SAR) ADC. It supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (ksps). Built-in bandgap circuitry offers 1% internal voltage reference accuracy or an external reference voltage can be used.

As shown in Figure 2-81, a SAR ADC contains N capacitors with binary-weighted values.

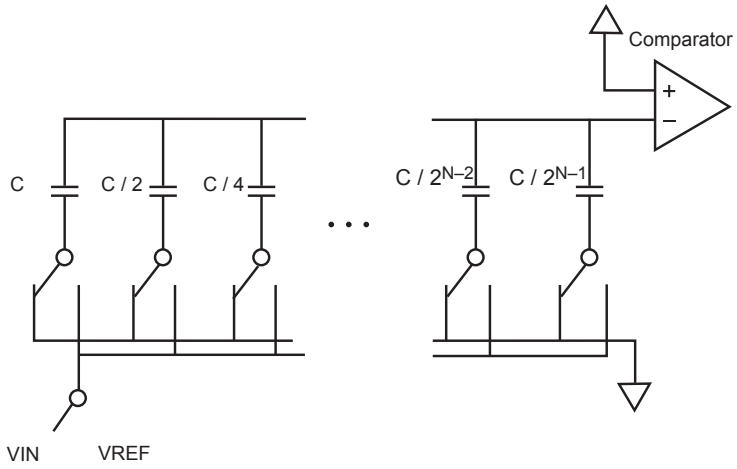



***Figure 2-81* • Example SAR ADC Architecture**

To begin a conversion, all of the capacitors are quickly discharged. Then VIN is applied to all the capacitors for a period of time (acquisition time) during which the capacitors are charged to a value very close to VIN. Then all of the capacitors are switched to ground, and thus –VIN is applied across the comparator. Now the conversion process begins. First, C is switched to VREF. Because of the binary weighting of the capacitors, the voltage at the input of the comparator is then shown by EQ 11.

$$\text{Voltage at input of comparator} = -\text{VIN} + \text{VREF} / 2$$

*EQ 11*

If VIN is greater than VREF / 2, the output of the comparator is 1; otherwise, the comparator output is 0. A register is clocked to retain this value as the MSB of the result. Next, if the MSB is 0, C is switched back to ground; otherwise, it remains connected to VREF, and C / 2 is connected to VREF. The result at the comparator input is now either –VIN + VREF / 4 or –VIN + 3 VREF / 4 (depending on the state of the MSB), and the comparator output now indicates the value of the next most significant bit. This bit is likewise registered, and the process continues for each subsequent bit until a conversion is completed. The conversion process requires some acquisition time plus N + 1 ADC clock cycles to complete.

This process results in a binary approximation of VIN. Generally, there is a fixed interval T, the sampling period, between the samples. The inverse of the sampling period is often referred to as the sampling frequency $f_S$ = 1 / T. The combined effect is illustrated in Figure 2-82.

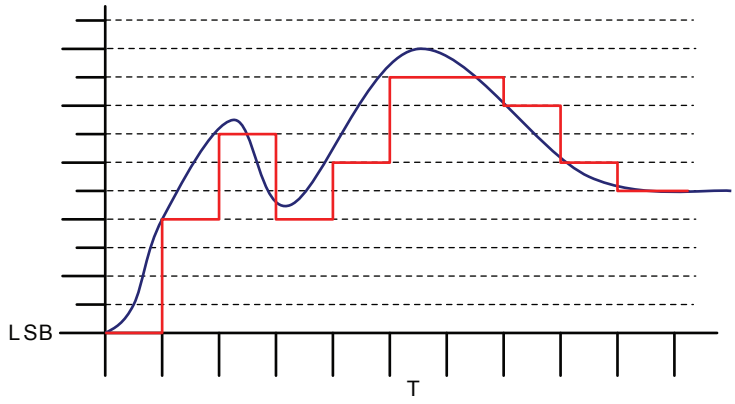



***Figure 2-82* • Conversion Example**

Figure 2-82 demonstrates that if the signal changes faster than the sampling rate can accommodate, or if the actual value of VIN falls between counts in the result, this information is lost during the conversion. There are several techniques that can be used to address these issues.

First, the sampling rate must be chosen to provide enough samples to adequately represent the input signal. Based on the Nyquist-Shannon Sampling Theorem, the minimum sampling rate must be at least twice the frequency of the highest frequency component in the target signal (Nyquist Frequency). For example, to recreate the frequency content of an audio signal with up to 22 KHz bandwidth, the user must sample it at a minimum of 44 ksps. However, as shown in Figure 2-82, significant post-processing of the data is required to interpolate the value of the waveform during the time between each sample.

Similarly, to re-create the amplitude variation of a signal, the signal must be sampled with adequate resolution. Continuing with the audio example, the dynamic range of the human ear (the ratio of the amplitude of the threshold of hearing to the threshold of pain) is generally accepted to be 135 dB, and the dynamic range of a typical symphony orchestra performance is around 85 dB. Most commercial recording media provide about 96 dB of dynamic range using 16-bit sample resolution. But 16-bit fidelity does not necessarily mean that you need a 16-bit ADC. As long as the input is sampled at or above the Nyquist Frequency, post-processing techniques can be used to interpolate intermediate values and reconstruct the original input signal to within desired tolerances.

If sophisticated digital signal processing (DSP) capabilities are available, the best results are obtained by implementing a reconstruction filter, which is used to interpolate many intermediate values with higher resolution than the original data. Interpolating many intermediate values increases the effective number of samples, and higher resolution increases the effective number of bits in the sample. In many cases, however, it is not cost-effective or necessary to implement such a sophisticated reconstruction algorithm. For applications that do not require extremely fine reproduction of the input signal, alternative methods can enhance digital sampling results with relatively simple post-processing. The details of such techniques are out of the scope of this chapter; refer to the *Improving ADC Results through Oversampling and Post-Processing of Data* white paper for more information.

## 5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, Fusion I/Os can directly drive signals into 5 V TTL receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceed the VIL = 0.8 V and VIH = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

## Simultaneously Switching Outputs and PCB Layout

- Simultaneously switching outputs (SSOs) can produce signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and VCCI dip noise. These two noise types are caused by rapidly changing currents through GND and VCCI package pin inductances during switching activities:
- Ground bounce noise voltage = L(GND) * di/dt
- VCCI dip noise voltage = L(VCCI) * di/dt

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

## Overview of I/O Performance

### Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Pro I/Os**

| I/O Standard | Drive Strength | Slew Rate | VIL | | VIH | | VOL | VOH | IOL | IOH |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5 V LVCMOS | 12 mA | High | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3 V PCI | Per PCI Specification | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X Specification | | | | | | | | | |
| 3.3 V GTL | 20 mA[2] | High | –0.3 | VREF – 0.05 | VREF + 0.05 | 3.6 | 0.4 | – | 20 | 20 |
| 2.5 V GTL | 20 mA[2] | High | –0.3 | VREF – 0.05 | VREF + 0.05 | 3.6 | 0.4 | – | 20 | 20 |
| 3.3 V GTL+ | 35 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.6 | – | 35 | 35 |
| 2.5 V GTL+ | 33 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.6 | – | 33 | 33 |
| HSTL (I) | 8 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 8 | 8 |
| HSTL (II) | 15 mA[2] | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 15 | 15 |
| SSTL2 (I) | 15 mA | High | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI – 0.62 | 15 | 15 |
| SSTL2 (II) | 18 mA | High | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI – 0.43 | 18 | 18 |
| SSTL3 (I) | 14 mA | High | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI – 1.1 | 14 | 14 |
| SSTL3 (II) | 21 mA | High | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI – 0.9 | 21 | 21 |

*Notes:*

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output slew rate can be extracted by the IBIS models.*

**Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Advanced I/Os**

| I/O Standard | Drive Strength | Slew Rate | VIL | | VIH | | VOL | VOH | IOL | IOH |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5 V LVCMOS | 12 mA | High | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3 V PCI | Per PCI specifications | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X specifications | | | | | | | | | |

*Note: Currents are measured at 85°C junction temperature.*

### 3.3 V PCI, 3.3 V PCI-X

The Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

**Table 2-134 • Minimum and Maximum DC Input and Output Levels**

| 3.3 V PCI/PCI-X | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-123.

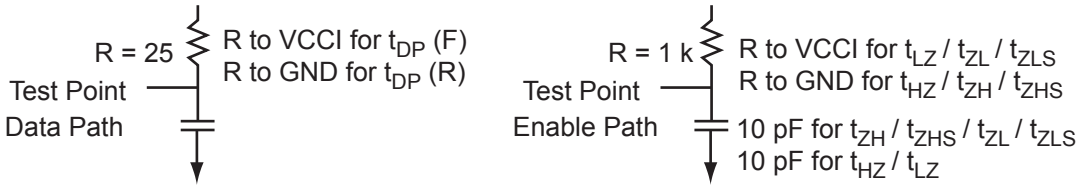



**Figure 2-123 • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the data path; Microsemi loading for tristate is described in Table 2-135.

**Table 2-135 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 0.285 * VCCI for $t_{DP(R)}$<br>0.615 * VCCI for $t_{DP(F)}$ | – | 10 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

### 2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

**Table 2-141 • Minimum and Maximum DC Input and Output Levels**

| 2.5 GTL | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 20 mA[3] | –0.3 | VREF – 0.05 | VREF + 0.05 | 3.6 | 0.4 | – | 20 | 20 | 124 | 169 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

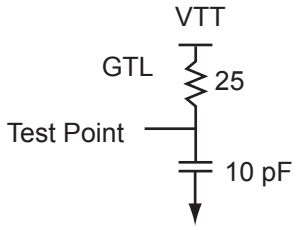



**Figure 2-125 • AC Loading**

**Table 2-142 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.05 | VREF + 0.05 | 0.8 | 0.8 | 1.2 | 10 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-143 • 2.5 V GTL**
**Commercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.13 | 0.04 | 2.46 | 0.43 | 2.16 | 2.13 | | | 4.40 | 4.36 | ns |
| –1 | 0.56 | 1.81 | 0.04 | 2.09 | 0.36 | 1.84 | 1.81 | | | 3.74 | 3.71 | ns |
| –2 | 0.49 | 1.59 | 0.03 | 1.83 | 0.32 | 1.61 | 1.59 | | | 3.28 | 3.26 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### 3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

**Table 2-144 • Minimum and Maximum DC Input and Output Levels**

| 3.3 V GTL+ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 35 mA | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.6 | – | 35 | 35 | 181 | 268 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

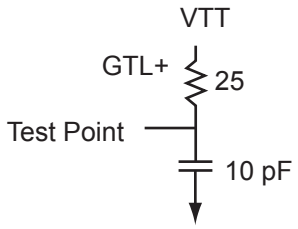



**Figure 2-126 • AC Loading**

**Table 2-145 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.1 | VREF + 0.1 | 1.0 | 1.0 | 1.5 | 10 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-146 • 3.3 V GTL+**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.0 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.06 | 0.04 | 1.59 | 0.43 | 2.09 | 2.06 | | | 4.33 | 4.29 | ns |
| –1 | 0.56 | 1.75 | 0.04 | 1.35 | 0.36 | 1.78 | 1.75 | | | 3.68 | 3.65 | ns |
| –2 | 0.49 | 1.53 | 0.03 | 1.19 | 0.32 | 1.56 | 1.53 | | | 3.23 | 3.20 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-156 • Minimum and Maximum DC Input and Output Levels**

| SSTL2 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 15 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI – 0.62 | 15 | 15 | 87 | 83 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

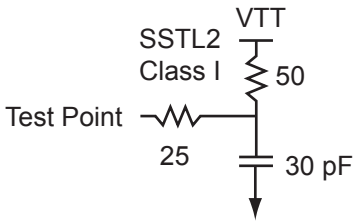



**Figure 2-130 • AC Loading**

**Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-158 • SSTL 2 Class I**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.13 | 0.04 | 1.33 | 0.43 | 2.17 | 1.85 | | | 4.40 | 4.08 | ns |
| –1 | 0.56 | 1.81 | 0.04 | 1.14 | 0.36 | 1.84 | 1.57 | | | 3.74 | 3.47 | ns |
| –2 | 0.49 | 1.59 | 0.03 | 1.00 | 0.32 | 1.62 | 1.38 | | | 3.29 | 3.05 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-162 • Minimum and Maximum DC Input and Output Levels**

| SSTL3 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 14 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI – 1.1 | 14 | 14 | 54 | 51 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

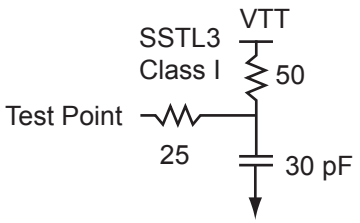



**Figure 2-132 • AC Loading**

**Table 2-163 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-164 • SSTL3 Class I**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.31 | 0.04 | 1.25 | 0.43 | 2.35 | 1.84 | | | 4.59 | 4.07 | ns |
| –1 | 0.56 | 1.96 | 0.04 | 1.06 | 0.36 | 2.00 | 1.56 | | | 3.90 | 3.46 | ns |
| –2 | 0.49 | 1.72 | 0.03 | 0.93 | 0.32 | 1.75 | 1.37 | | | 3.42 | 3.04 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### Input Register

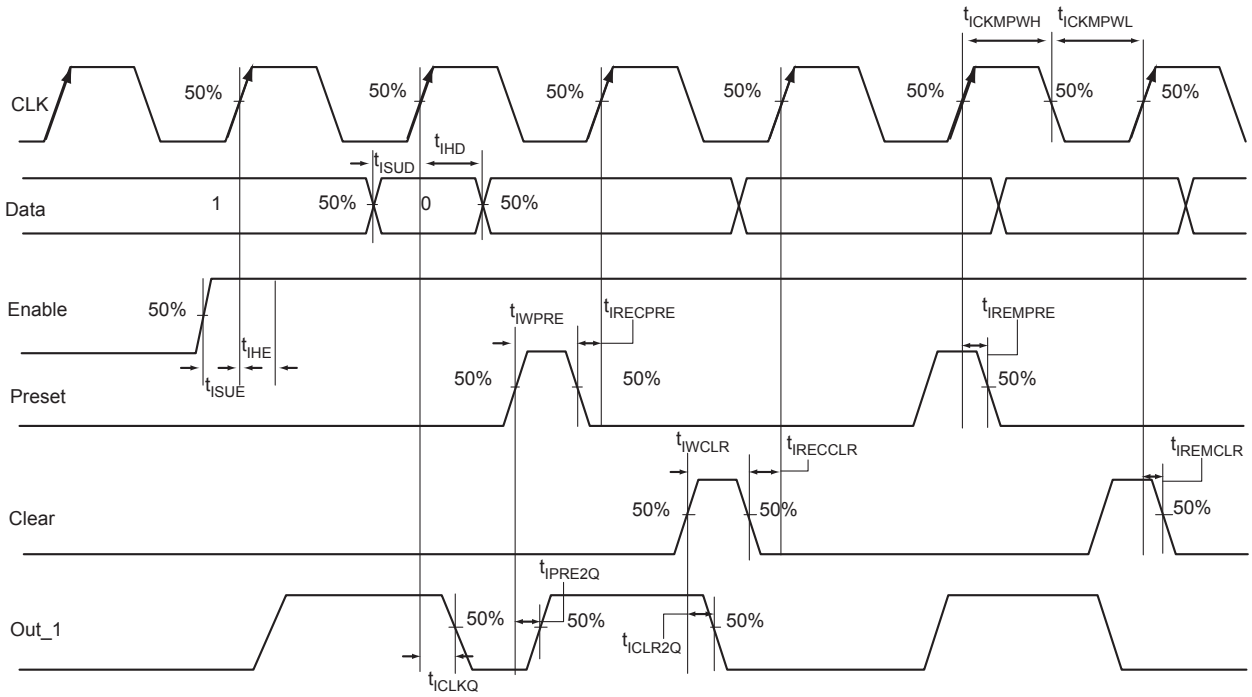



***Figure 2-139* • Input Register Timing Diagram**

### Timing Characteristics

***Table 2-176* • Input Data Register Propagation Delays**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.24 | 0.27 | 0.32 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.26 | 0.30 | 0.35 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 0.37 | 0.42 | 0.50 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.32 | 0.37 | 0.43 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**XTAL2 Crystal Oscillator Circuit Input**

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

# Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the *Fusion Security* application note.

## 128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has $3.4 \times 10^{38}$ possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note *Fusion Security* for more details.

## AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

# Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

***Table 3-2 •*** **Recommended Operating Conditions**[1]

| Symbol | Parameter[2] | | Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature | | 0 to +85 | –40 to +100 | °C |
| VCC | 1.5 V DC core supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP | Programming voltage | Programming mode[3] | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation[4] | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL | Analog power supply (PLL) | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCCI | 1.5 V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8 V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5 V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3 V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | LVDS differential I/O | | 2.375 to 2.625 | 2.375 to 2.625 | V |
| | LVPECL differential I/O | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| VCC33A | +3.3 V power supply | | 2.97 to 3.63 | 2.97 to 3.63 | V |
| VCC33PMP | +3.3 V power supply | | 2.97 to 3.63 | 2.97 to 3.63 | V |
| VAREF | Voltage reference for ADC | | 2.527 to 2.593 | 2.527 to 2.593 | V |
| VCC15A [5] | Digital power supply for the analog system | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCCNVM | Embedded flash power supply | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCCOSC | Oscillator power supply | | 2.97 to 3.63 | 2.97 to 3.63 | V |
| AV, AC [6] | Unpowered, ADC reset asserted or unconfigured | | –10.5 to 12.0 | –10.5 to 11.6 | V |
| | Analog input (+16 V to +2 V prescaler range) | | –0.3 to 12.0 | –0.3 to 11.6 | V |
| | Analog input (+1 V to + 0.125 V prescaler range) | | –0.3 to 3.6 | –0.3 to 3.6 | V |
| | Analog input (–16 V to –2 V prescaler range) | | –10.5 to 0.3 | –10.5 to 0.3 | V |
| | Analog input (–1 V to –0.125 V prescaler range) | | –3.6 to 0.3 | –3.6 to 0.3 | V |
| | Analog input (direct input to ADC) | | –0.3 to 3.6 | –0.3 to 3.6 | V |
| | Digital input | | –0.3 to 12.0 | –0.3 to 11.6 | V |
| AG [6] | Unpowered, ADC reset asserted or unconfigured | | –10.5 to 12.0 | –10.5 to 11.6 | V |
| | Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA) | | –0.3 to 12.0 | –0.3 to 11.6 | V |
| | Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA) | | –10.5 to 0.3 | –10.5 to 0.3 | V |
| | High Current Mode [7] | | –10.5 to 12.0 | –10.5 to 11.6 | V |
| AT [6] | Unpowered, ADC reset asserted or unconfigured | | –0.3 to 15.5 | –0.3 to 14.5 | V |
| | Analog input (+16 V, +4 V prescaler range) | | –0.3 to 15.5 | –0.3 to 14.5 | V |
| | Analog input (direct input to ADC) | | –0.3 to 3.6 | –0.3 to 3.6 | V |
| | Digital input | | –0.3 to 15.5 | –0.3 to 14.5 | V |

*Notes:*

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-157.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.*
4. *VPUMP can be left floating during normal operation (not programming mode).*
5. *Violating the $V_{CC15A}$ recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.*
6. *The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.*
7. *The AG pad should also conform to the limits as specified in Table 2-48 on page 2-114.*

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + (\alpha_1 / 2) * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

$F_{CLK}$ is the global clock signal frequency.

***Standby Mode and Sleep Mode***

$P_{S\text{-}CELL} = 0$ W

### Combinatorial Cells Dynamic Contribution—$P_{C\text{-}CELL}$

***Operating Mode***

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

$F_{CLK}$ is the global clock signal frequency.

***Standby Mode and Sleep Mode***

$P_{C\text{-}CELL} = 0$ W

Routing Net Dynamic Contribution—$P_{NET}$

***Operating Mode***

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

$F_{CLK}$ is the global clock signal frequency.

***Standby Mode and Sleep Mode***

$P_{NET} = 0$ W

### I/O Input Buffer Dynamic Contribution—$P_{INPUTS}$

***Operating Mode***

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 3-16 on page 3-27.

$F_{CLK}$ is the global clock signal frequency.

***Standby Mode and Sleep Mode***

$P_{INPUTS} = 0$ W

### I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

***Operating Mode***

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 3-16 on page 3-27.

$\beta_1$ is the I/O buffer enable rate—guidelines are provided in Table 3-17 on page 3-27.

$F_{CLK}$ is the global clock signal frequency.

***Standby Mode and Sleep Mode***

$P_{OUTPUTS} = 0$ W

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| A1 | NC |
| A2 | GND |
| A3 | NC |
| A4 | NC |
| A5 | GND |
| A6 | NC |
| A7 | NC |
| A8 | GND |
| A9 | IO17NDB0V2 |
| A10 | IO17PDB0V2 |
| A11 | GND |
| A12 | IO18NDB0V2 |
| A13 | IO18PDB0V2 |
| A14 | IO20NDB0V2 |
| A15 | IO20PDB0V2 |
| A16 | GND |
| A17 | IO21PDB0V2 |
| A18 | IO21NDB0V2 |
| A19 | GND |
| A20 | IO39NDB1V2 |
| A21 | IO39PDB1V2 |
| A22 | GND |
| A23 | NC |
| A24 | NC |
| A25 | GND |
| A26 | NC |
| AA1 | NC |
| AA2 | VCCIB4 |
| AA3 | IO93PDB4V0 |
| AA4 | GND |
| AA5 | IO93NDB4V0 |
| AA6 | GEB2/IO86PDB4V0 |
| AA7 | IO86NDB4V0 |
| AA8 | AV0 |
| AA9 | GNDA |
| AA10 | AV1 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| AA11 | AV2 |
| AA12 | GNDA |
| AA13 | AV3 |
| AA14 | AV6 |
| AA15 | GNDA |
| AA16 | AV7 |
| AA17 | AV8 |
| AA18 | GNDA |
| AA19 | AV9 |
| AA20 | VCCIB2 |
| AA21 | IO68PPB2V0 |
| AA22 | TCK |
| AA23 | GND |
| AA24 | IO76PPB2V0 |
| AA25 | VCCIB2 |
| AA26 | NC |
| AB1 | GND |
| AB2 | NC |
| AB3 | GEC2/IO87PDB4V0 |
| AB4 | IO87NDB4V0 |
| AB5 | GEA2/IO85PDB4V0 |
| AB6 | IO85NDB4V0 |
| AB7 | NCAP |
| AB8 | AC0 |
| AB9 | VCC33A |
| AB10 | AC1 |
| AB11 | AC2 |
| AB12 | VCC33A |
| AB13 | AC3 |
| AB14 | AC6 |
| AB15 | VCC33A |
| AB16 | AC7 |
| AB17 | AC8 |
| AB18 | VCC33A |
| AB19 | AC9 |
| AB20 | ADCGNDREF |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| AB21 | PTBASE |
| AB22 | GNDNVM |
| AB23 | VCCNVM |
| AB24 | VPUMP |
| AB25 | NC |
| AB26 | GND |
| AC1 | NC |
| AC2 | NC |
| AC3 | NC |
| AC4 | GND |
| AC5 | VCCIB4 |
| AC6 | VCCIB4 |
| AC7 | PCAP |
| AC8 | AG0 |
| AC9 | GNDA |
| AC10 | AG1 |
| AC11 | AG2 |
| AC12 | GNDA |
| AC13 | AG3 |
| AC14 | AG6 |
| AC15 | GNDA |
| AC16 | AG7 |
| AC17 | AG8 |
| AC18 | GNDA |
| AC19 | AG9 |
| AC20 | VAREF |
| AC21 | VCCIB2 |
| AC22 | PTEM |
| AC23 | GND |
| AC24 | NC |
| AC25 | NC |
| AC26 | NC |
| AD1 | NC |
| AD2 | NC |
| AD3 | GND |
| AD4 | NC |

# 5 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 6 (March 2014) | Note added for the discontinuance of QN108 and QN180 packages to the "Package I/Os: Single-/Double-Ended (Analog)" table and the "Temperature Grade Offerings" table (SAR 55113, PDN 1306). | II and IV |
| | Updated details about page programming time in the "Program Operation" section (SAR 49291). | 2-46 |
| | ADC_START changed to ADCSTART in the "ADC Operation" section (SAR 44104). | 2-104 |
| Revision 5 (January 2014) | Calibrated offset values (AFS090, AFS250) of the external temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 51464). | 2-117 |
| | Specifications for the internal temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 50870). | 2-117 |
| Revision 4 (January 2013) | The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43177). | III |
| | The note in Table 2-12 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42563). | 2-28 |
| | Table 2-49 • Analog Channel Specifications was modified to update the uncalibrated offset values (AFS250) of the external and internal temperature monitors (SAR 43134). | 2-117 |
| | In Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3), changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 20812). | 2-130 |
| | The values for the Speed Grade (-1 and Std.) for FDDRIMAX (Table 2-180 • Input DDR Propagation Delays) and values for the Speed Grade (-2 and Std.) for FDDOMAX (Table 2-182 • Output DDR Propagation Delays) had been inadvertently interchanged. This has been rectified (SAR 38514). | 2-220, 2-222 |
| | Added description about what happens if a user connects VAREF to an external 3.3 V on their board to the "VAREF Analog Reference Voltage" section (SAR 35188). | 2-225 |
| | Added a note to Table 3-2 • Recommended Operating Conditions1 (SAR 43429): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C. | 3-3 |
| | Added the Package Thermal details for AFS600-PQ208 and AFS250-PQ208 to Table 3-6 • Package Thermal Resistance (SAR 37816). Deleted the Die Size column from the table (SAR 43503). | 3-7 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 42495).<br>Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 3 (August 2012) | Microblade U1AFS250 and U1AFS1500 devices were added to the product tables. | I – IV |
| | A sentence pertaining to the analog I/Os was added to the "Specifying I/O States During Programming" section (SAR 34831). | 1-9 |