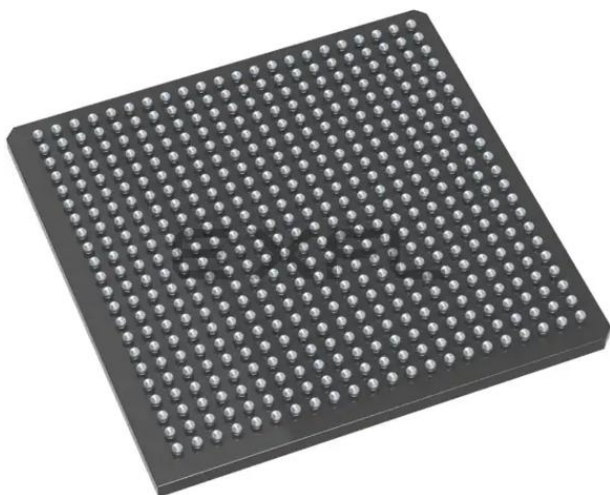




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs600-fg484i

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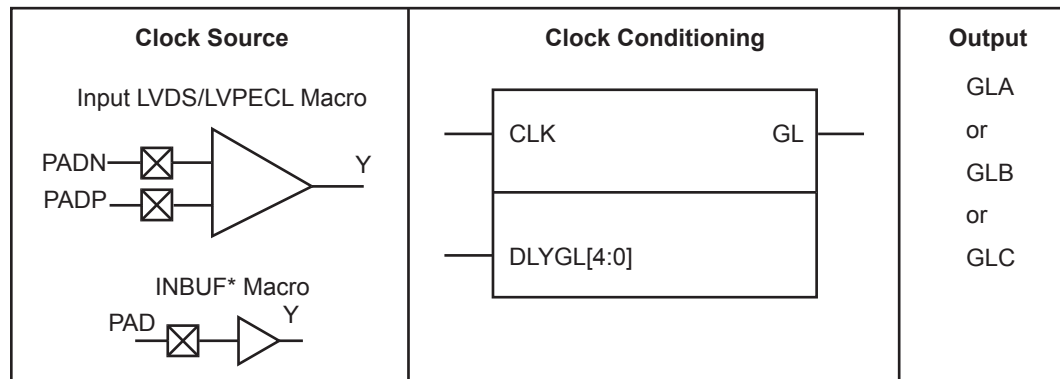
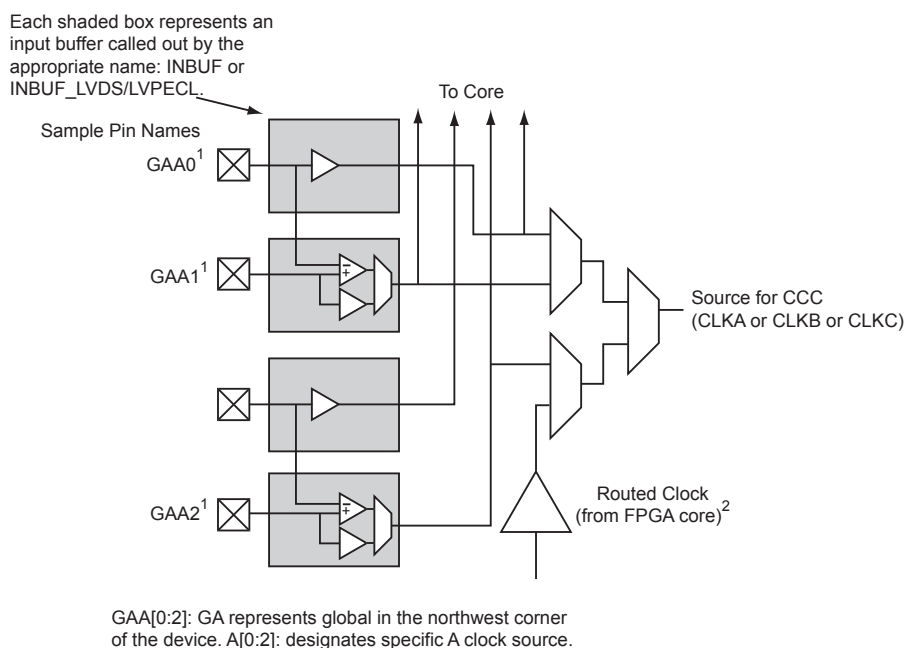


Figure 2-21 • Fusion CCC Options: Global Buffers with Programmable Delay

Global Input Selections

Each global buffer, as well as the PLL reference clock, can be driven from one of the following (Figure 2-22):

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core



Notes:

1. Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the ["User I/O Naming Convention"](#) section on page 2-158 for more information.
2. Instantiate the routed clock source input as follows:
 - a) Connect the output of a logic element to the clock input of the PLL, CLKDLY, or CLKINT macro.
 - b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS) in a relevant global pin location.
3. LVDS-based clock sources are available in the east and west banks on all Fusion devices.

Figure 2-22 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT

Table 2-16 • RTC Control/Status Register

Bit	Name	Description	Default Value
7	rtc_rst	RTC Reset 1 – Resets the RTC 0 – Deassert reset on after two ACM_CLK cycle.	
6	cntr_en	Counter Enable 1 – Enables the counter; rtc_rst must be deasserted as well. First counter increments after 64 RTCCLK positive edges. 0 – Disables the crystal prescaler but does not reset the counter value. Counter value can only be updated when the counter is disabled.	0
5	vr_en_mat	Voltage Regulator Enable on Match 1 – Enables RTCMATCH and RTCPSMMATCH to output 1 when the counter value equals the Match Register value. This enables the 1.5 V voltage regulator when RTCPSMMATCH connects to the RTCPSMMATCH signal in VRPSM. 0 – RTCMATCH and RTCPSMMATCH output 0 at all times.	0
4:3	xt_mode[1:0]	Crystal Mode Controls RTCXTLMODE[1:0]. Connects to RTC_MODE signal in XTLOSC. XTL_MODE uses this value when xtal_en is 1. See the "Crystal Oscillator" section on page 2-20 for mode configuration.	00
2	rst_cnt_omat	Reset Counter on Match 1 – Enables the sync clear of the counter when the counter value equals the Match Register value. The counter clears on the rising edge of the clock. If all the Match Registers are set to 0, the clear is disabled. 0 – Counter increments indefinitely	0
1	rstb_cnt	Counter Reset, active Low 0 - Resets the 40-bit counter value	0
0	xtal_en	Crystal Enable Controls RTCXTLSEL. Connects to SELMODE signal in XTLOSC. 0 – XTLOSC enables control by FPGA_EN; xt_mode is not used. Sleep mode requires this bit to equal 0. 1 – Enables XTLOSC, XTL_MODE control by xt_mode Standby mode requires this bit to be set to 1. See the "Crystal Oscillator" section on page 2-20 for further details on SELMODE configuration.	0

Flash Memory Block Characteristics

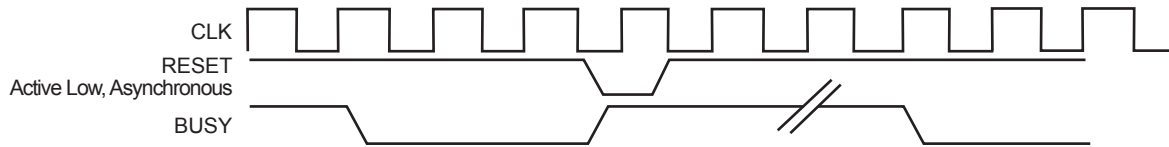


Figure 2-44 • Reset Timing Diagram

Table 2-25 • Flash Memory Block Timing
 Commercial Temperature Range Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{CLK2RD}	Clock-to-Q in 5-cycle read mode of the Read Data	7.99	9.10	10.70	ns
	Clock-to-Q in 6-cycle read mode of the Read Data	5.03	5.73	6.74	ns
t_{CLK2BUSY}	Clock-to-Q in 5-cycle read mode of BUSY	4.95	5.63	6.62	ns
	Clock-to-Q in 6-cycle read mode of BUSY	4.45	5.07	5.96	ns
$t_{\text{CLK2STATUS}}$	Clock-to-Status in 5-cycle read mode	11.24	12.81	15.06	ns
	Clock-to-Status in 6-cycle read mode	4.48	5.10	6.00	ns
t_{DSUNVM}	Data Input Setup time for the Control Logic	1.92	2.19	2.57	ns
t_{DHNVM}	Data Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{ASUNVM}	Address Input Setup time for the Control Logic	2.76	3.14	3.69	ns
t_{AHNVM}	Address Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{SUDWNVM}	Data Width Setup time for the Control Logic	1.85	2.11	2.48	ns
t_{HDDWNVM}	Data Width Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{SURENNVM}	Read Enable Setup time for the Control Logic	3.85	4.39	5.16	ns
t_{HDRENNVM}	Read Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
t_{SUWENNVN}	Write Enable Setup time for the Control Logic	2.37	2.69	3.17	ns
t_{HDWENNVN}	Write Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUPROGNVM}}$	Program Setup time for the Control Logic	2.16	2.46	2.89	ns
$t_{\text{HDPROGNVM}}$	Program Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUSPAREPAGE}}$	SparePage Setup time for the Control Logic	3.74	4.26	5.01	ns
$t_{\text{HDSPAREPAGE}}$	SparePage Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{SUAUXBLK}	Auxiliary Block Setup Time for the Control Logic	3.74	4.26	5.00	ns
t_{HDAUXBLK}	Auxiliary Block Hold Time for the Control Logic	0.00	0.00	0.00	ns
t_{SURDNEXT}	ReadNext Setup Time for the Control Logic	2.17	2.47	2.90	ns
t_{HDRDNEXT}	ReadNext Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUERASEPG}}$	Erase Page Setup Time for the Control Logic	3.76	4.28	5.03	ns
$t_{\text{HDERASEPG}}$	Erase Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUUNPROTECTPG}}$	Unprotect Page Setup Time for the Control Logic	2.01	2.29	2.69	ns
$t_{\text{HDUNPROTECTPG}}$	Unprotect Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUDISCARDPG}}$	Discard Page Setup Time for the Control Logic	1.88	2.14	2.52	ns
$t_{\text{HDDISCARDPG}}$	Discard Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUOVERWRPRO}}$	Overwrite Protect Setup Time for the Control Logic	1.64	1.86	2.19	ns
$t_{\text{HDOVERWRPRO}}$	Overwrite Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns

SRAM Characteristics

Timing Waveforms

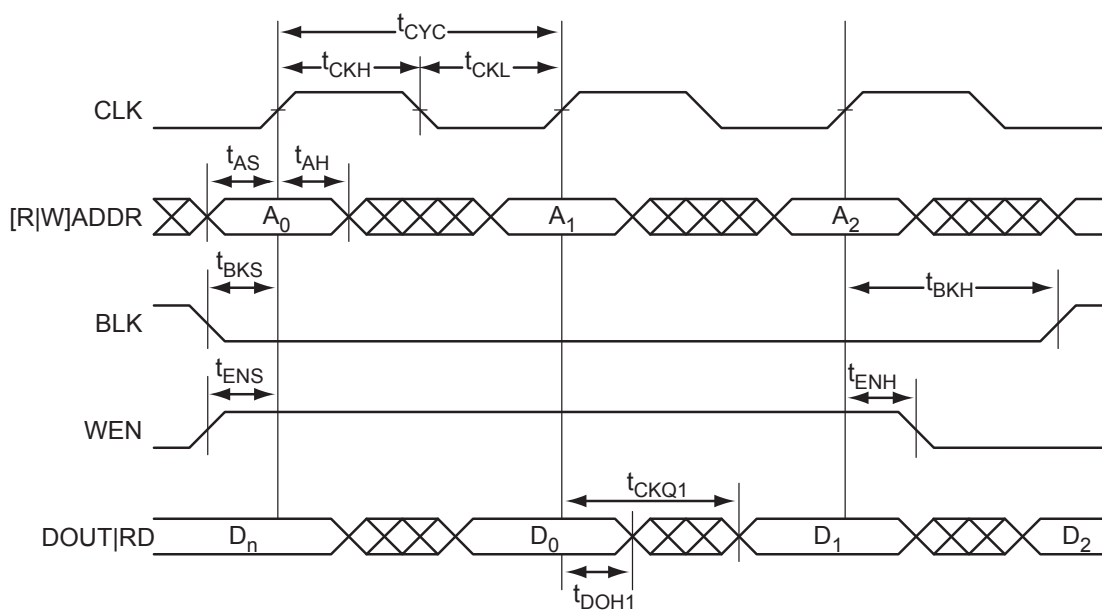


Figure 2-50 • RAM Read for Flow-Through Output. Applicable to both RAM4K9 and RAM512x18.

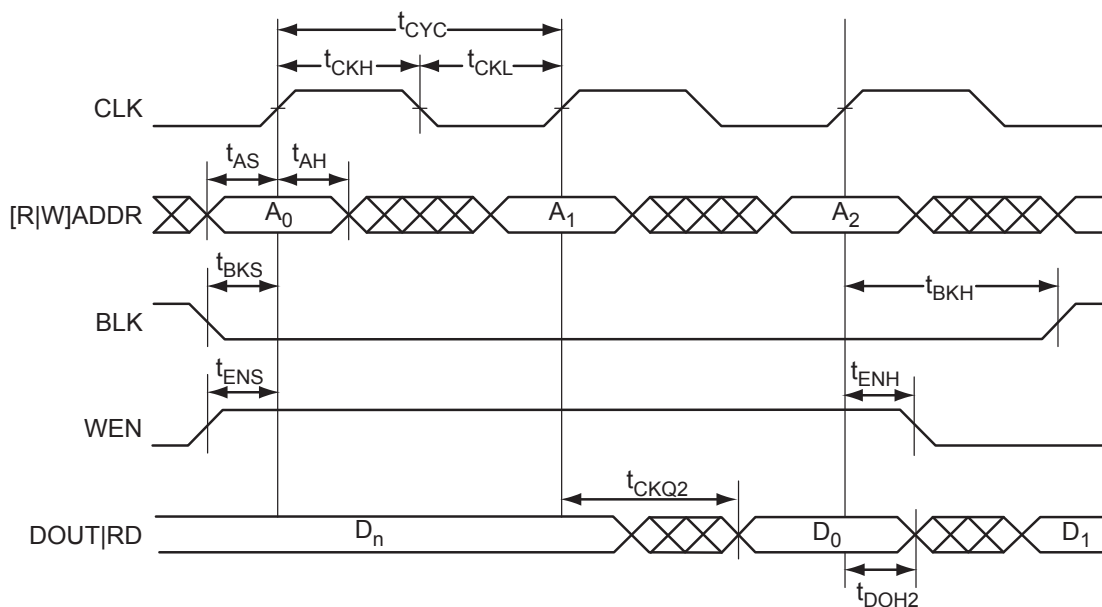


Figure 2-51 • RAM Read for Pipelined Output. Applicable to both RAM4K9 and RAM512x18.

Analog Block

With the Fusion family, Microsemi has introduced the world's first mixed-mode FPGA solution. Supporting a robust analog peripheral mix, Fusion devices will support a wide variety of applications. It is this Analog Block that separates Fusion from all other FPGA solutions on the market today.

By combining both flash and high-speed CMOS processes in a single chip, these devices offer the best of both worlds. The high-performance CMOS is used for building RAM resources. These high-performance structures support device operation up to 350 MHz. Additionally, the advanced Microsemi 0.13 μm flash process incorporates high-voltage transistors and a high-isolation, triple-well process. Both of these are suited for the flash-based programmable logic and nonvolatile memory structures.

High-voltage transistors support the integration of analog technology in several ways. They aid in noise immunity so that the analog portions of the chip can be better isolated from the digital portions, increasing analog accuracy. Because they support high voltages, Microsemi flash FPGAs can be connected directly to high-voltage input signals, eliminating the need for external resistor divider networks, reducing component count, and increasing accuracy. By supporting higher internal voltages, the Microsemi advanced flash process enables high dynamic range on analog circuitry, increasing precision and signal-noise ratio. Microsemi flash FPGAs also drive high-voltage outputs, eliminating the need for external level shifters and drivers.

The unique triple-well process enables the integration of high-performance analog features with increased noise immunity and better isolation. By increasing the efficiency of analog design, the triple-well process also enables a smaller overall design size, reducing die size and cost.

The Analog Block consists of the Analog Quad I/O structure, RTC (for details refer to the ["Real-Time Counter System" section on page 2-31](#)), ADC, and ACM. All of these elements are combined in the single Analog Block macro, with which the user implements this functionality ([Figure 2-64](#)).

The Analog Block needs to be reset/reinitialized after the core powers up or the device is programmed. An external reset/initialize signal, which can come from the internal voltage regulator when it powers up, must be applied.

Fusion uses a remote diode as a temperature sensor. The Fusion Temperature Monitor uses a differential input; the AT pin and ATRTN (AT Return) pin are the differential inputs to the Temperature Monitor. There is one Temperature Monitor in each Quad. A simplified block diagram is shown in [Figure 2-77](#).

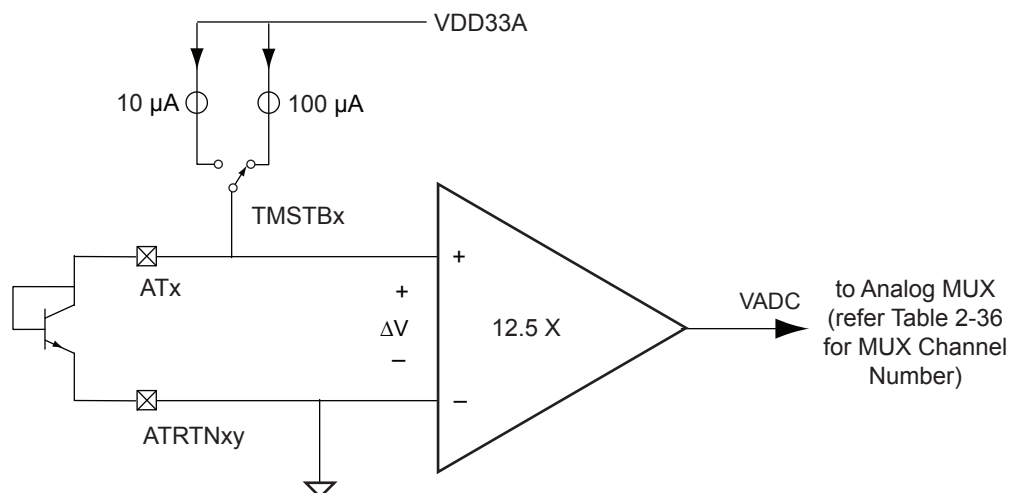


Figure 2-77 • Block Diagram for Temperature Monitor Circuit

The Fusion approach to measuring temperature is forcing two different currents through the diode with a ratio of 10:1. The switch that controls the different currents is controlled by the Temperature Monitor Strobe signal, TMSTB. Setting TMSTB to '1' will initiate a Temperature reading. The TMSTB should remain '1' until the ADC finishes sampling the voltage from the Temperature Monitor. The minimum sample time for the Temperature Monitor cannot be less than the minimum strobe high time minus the setup time. [Figure 2-78](#) shows the timing diagram.

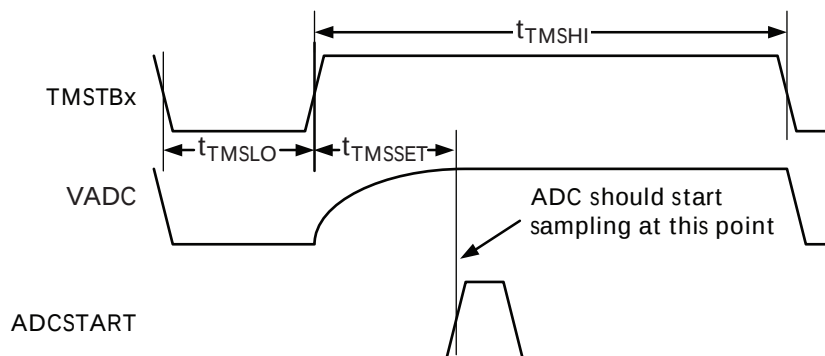


Figure 2-78 • Timing Diagram for the Temperature Monitor Strobe Signal

Note: When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device.

Typical Performance Characteristics

Temperature Error vs. Die Temperature

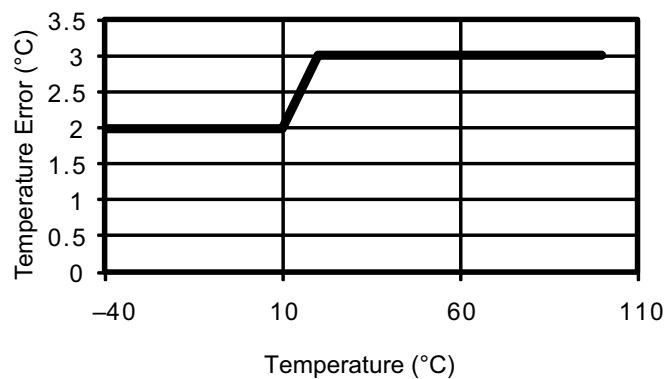


Figure 2-94 • Temperature Error

Temperature Error vs. Interconnect Capacitance

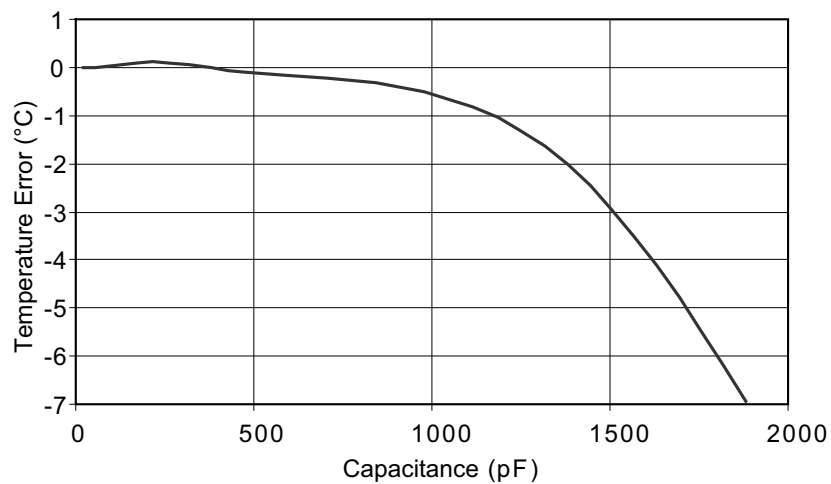


Figure 2-95 • Effect of External Sensor Capacitance

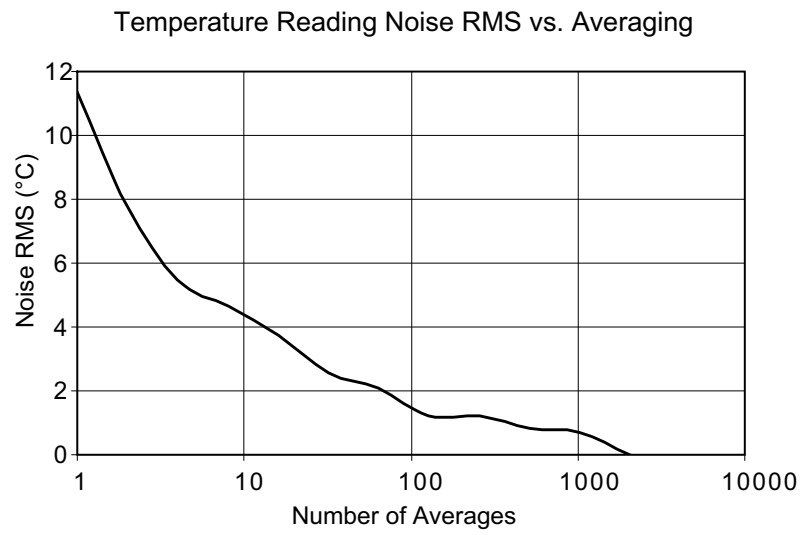


Figure 2-96 • Temperature Reading Noise When Averaging is Used

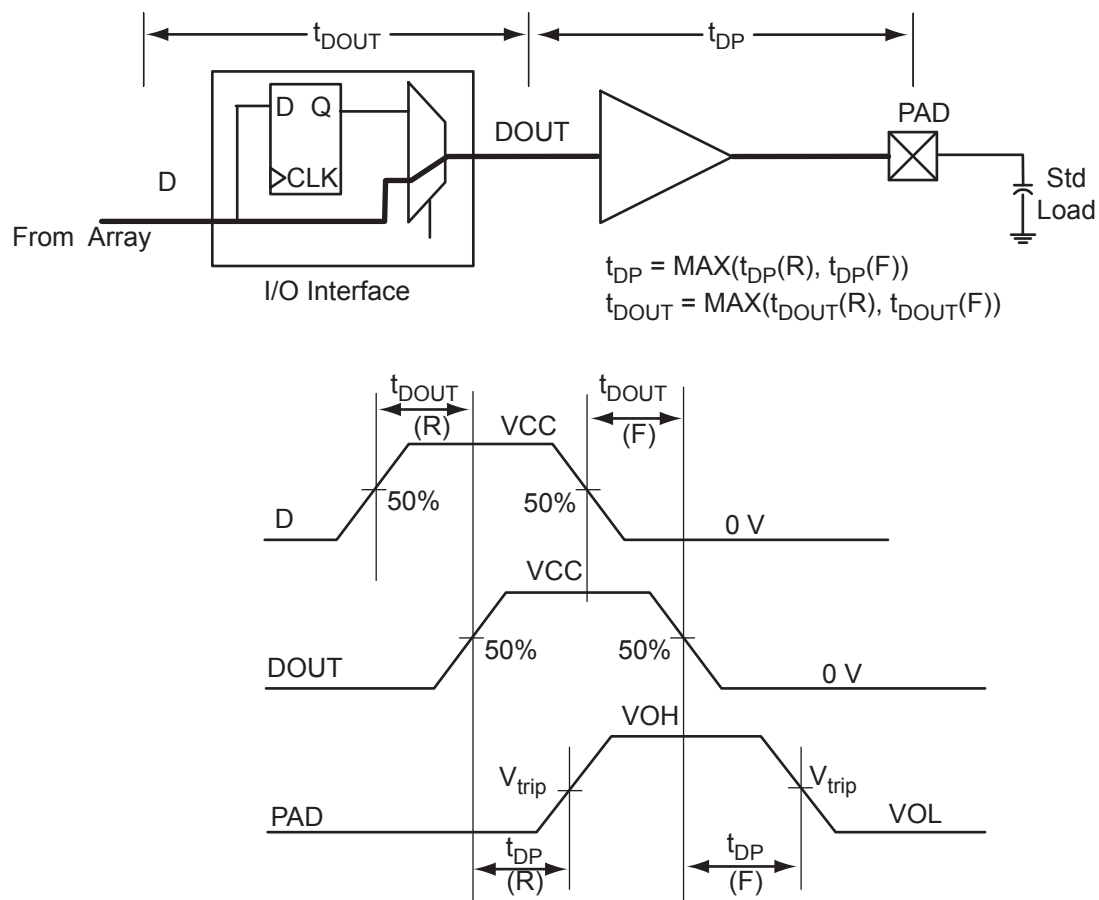


Figure 2-117 • Output Buffer Model and Delays (example)

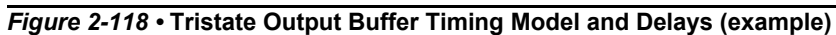


Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = \text{I/O Standard Dependent}$
Applicable to Pro I/Os

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	$t_{PY S}$	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTTL/ 3.3 V LVCMOS	12 mA	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
2.5 V LVCMOS	12 mA	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
1.8 V LVCMOS	12 mA	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
1.5 V LVCMOS	12 mA	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
3.3 V PCI	Per PCI spec	High	10	25 ²	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 ²	0.49	2.09	0.03	0.77	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V GTL	20 mA	High	10	25	0.49	1.55	0.03	2.19	–	0.32	1.52	1.55	0.00	0.00	3.19	3.22	ns
2.5 V GTL	20 mA	High	10	25	0.49	1.59	0.03	1.83	–	0.32	1.61	1.59	0.00	0.00	3.28	3.26	ns
3.3 V GTL+	35 mA	High	10	25	0.49	1.53	0.03	1.19	–	0.32	1.56	1.53	0.00	0.00	3.23	3.20	ns
2.5 V GTL+	33 mA	High	10	25	0.49	1.65	0.03	1.13	–	0.32	1.68	1.57	0.00	0.00	3.35	3.24	ns
HSTL (I)	8 mA	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	0.00	0.00	4.09	4.02	ns
HSTL (II)	15 mA	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	0.00	0.00	3.97	3.70	ns
SSTL2 (I)	17 mA	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	0.00	0.00	3.29	3.05	ns
SSTL2 (II)	21 mA	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	0.00	0.00	3.32	2.99	ns
SSTL3 (I)	16 mA	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	0.00	0.00	3.42	3.04	ns
SSTL3 (II)	24 mA	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	0.00	0.00	3.24	2.92	ns
LVDS	24 mA	High	–	–	0.49	1.57	0.03	1.36	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.49	1.60	0.03	1.22	–	–	–	–	–	–	–	–	ns

Notes:

1. For specific junction temperature and voltage-supply levels, refer to [Table 3-6 on page 3-7](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-123 on page 2-197](#) for connectivity. This resistor is not required during normal operation.

Detailed I/O DC Characteristics

Table 2-95 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0$, $f = 1.0$ MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0$, $f = 1.0$ MHz		8	pF

Table 2-96 • I/O Output Buffer Maximum Resistances ¹

Standard	Drive Strength	$R_{PULL-DOWN}$ (ohms) ²	$R_{PULL-UP}$ (ohms) ³
Applicable to Pro I/O Banks			
3.3 V LVTTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA	11	–
2.5 V GTL	20 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = V_{OLspec} / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Timing Characteristics

Table 2-112 • 2.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	12.00	0.04	1.51	1.66	0.43	12.23	11.61	2.72	2.20	14.46	13.85	ns
	–1	0.51	10.21	0.04	1.29	1.41	0.36	10.40	9.88	2.31	1.87	12.30	11.78	ns
	–2	0.45	8.96	0.03	1.13	1.24	0.32	9.13	8.67	2.03	1.64	10.80	10.34	ns
8 mA	Std.	0.60	8.73	0.04	1.51	1.66	0.43	8.89	8.01	3.10	2.93	11.13	10.25	ns
	–1	0.51	7.43	0.04	1.29	1.41	0.36	7.57	6.82	2.64	2.49	9.47	8.72	ns
	–2	0.45	6.52	0.03	1.13	1.24	0.32	6.64	5.98	2.32	2.19	8.31	7.65	ns
12 mA	Std.	0.66	6.77	0.04	1.51	1.66	0.43	6.90	6.11	3.37	3.39	9.14	8.34	ns
	–1	0.56	5.76	0.04	1.29	1.41	0.36	5.87	5.20	2.86	2.89	7.77	7.10	ns
	–2	0.49	5.06	0.03	1.13	1.24	0.32	5.15	4.56	2.51	2.53	6.82	6.23	ns
16 mA	Std.	0.66	6.31	0.04	1.51	1.66	0.43	6.42	5.73	3.42	3.52	8.66	7.96	ns
	–1	0.56	5.37	0.04	1.29	1.41	0.36	5.46	4.87	2.91	3.00	7.37	6.77	ns
	–2	0.49	4.71	0.03	1.13	1.24	0.32	4.80	4.28	2.56	2.63	6.47	5.95	ns
24 mA	Std.	0.66	5.93	0.04	1.51	1.66	0.43	6.04	5.70	3.49	4.00	8.28	7.94	ns
	–1	0.56	5.05	0.04	1.29	1.41	0.36	5.14	4.85	2.97	3.40	7.04	6.75	ns
	–2	0.49	4.43	0.03	1.13	1.24	0.32	4.51	4.26	2.61	2.99	6.18	5.93	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Output Register

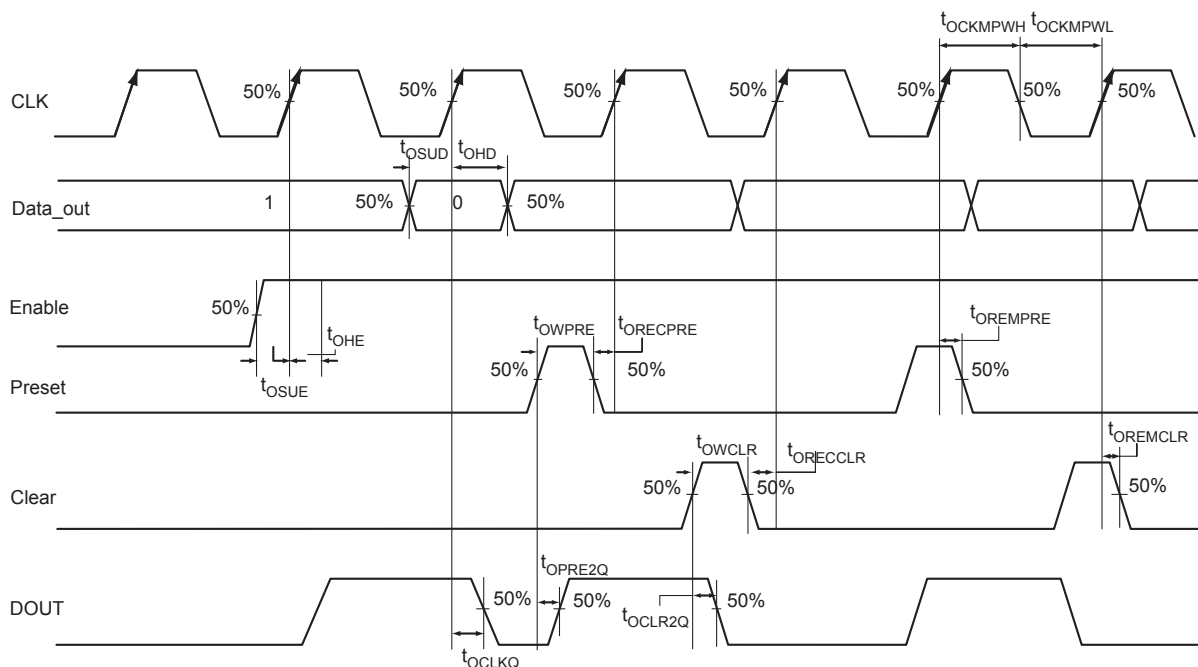


Figure 2-140 • Output Register Timing Diagram

Timing Characteristics

Table 2-177 • Output Data Register Propagation Delays
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCLKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCLKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the [Fusion Security](#) application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note [Fusion Security](#) for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Applicable to Pro I/O Banks				
Single-Ended				
3.3 V LVTTTL/LVCMOS	35	3.3	—	474.70
2.5 V LVCMOS	35	2.5	—	270.73
1.8 V LVCMOS	35	1.8	—	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	—	104.55
3.3 V PCI	10	3.3	—	204.61
3.3 V PCI-X	10	3.3	—	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	—	24.08
2.5 V GTL	10	2.5	—	13.52
3.3 V GTL+	10	3.3	—	24.10
2.5 V GTL+	10	2.5	—	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS	—	2.5	7.70	89.62
LVPECL	—	3.3	19.42	168.02
Applicable to Advanced I/O Banks				
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	—	468.67
2.5 V LVCMOS	35	2.5	—	267.48
1.8 V LVCMOS	35	1.8	—	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	—	103.12
3.3 V PCI	10	3.3	—	201.02
3.3 V PCI-X	10	3.3	—	201.02

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.
2. PDC8 is the static power (where applicable) measured on V_{CCI}.
3. PAC10 is the total dynamic power measured on V_{CC} and V_{CCI}.

$$P_{S-CELL} = N_{S-CELL} * (PAC5 + (\alpha_1 / 2) * PAC6) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-16 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{S-CELL} = 0 \text{ W}$$

Combinatorial Cells Dynamic Contribution— P_{C-CELL}

Operating Mode

$$P_{C-CELL} = N_{C-CELL} * (\alpha_1 / 2) * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-16 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{C-CELL} = 0 \text{ W}$$

Routing Net Dynamic Contribution— P_{NET}

Operating Mode

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * (\alpha_1 / 2) * PAC8 * F_{CLK}$$

N_{S-CELL} is the number VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-16 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{NET} = 0 \text{ W}$$

I/O Input Buffer Dynamic Contribution— P_{INPUTS}

Operating Mode

$$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 3-16 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{INPUTS} = 0 \text{ W}$$

I/O Output Buffer Dynamic Contribution— $P_{OUTPUTS}$

Operating Mode

$$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 3-16 on page 3-27](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 3-17 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{OUTPUTS} = 0 \text{ W}$$

RAM Dynamic Contribution— P_{MEMORY}

Operating Mode

$$P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE-CLOCK})$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in [Table 3-17 on page 3-27](#).

β_3 the RAM enable rate for write operations—guidelines are provided in [Table 3-17 on page 3-27](#).

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

Standby Mode and Sleep Mode

$$P_{MEMORY} = 0 \text{ W}$$

PLL/CCC Dynamic Contribution— P_{PLL}

Operating Mode

$$P_{PLL} = PAC13 * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Standby Mode and Sleep Mode

$$P_{PLL} = 0 \text{ W}$$

Nonvolatile Memory Dynamic Contribution— P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

$$P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * PAC15 * F_{READ-NVM} \text{ when } F_{READ-NVM} \leq 33 \text{ MHz,}$$

$$P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * (PAC16 + PAC17 * F_{READ-NVM} \text{ when } F_{READ-NVM} > 33 \text{ MHz}$$

$N_{NVM-BLOCKS}$ is the number of NVM blocks used in the design (2 in AFS600).

β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state).

$F_{READ-NVM}$ is the NVM read clock frequency.

Standby Mode and Sleep Mode

$$P_{NVM} = 0 \text{ W}$$

Crystal Oscillator Dynamic Contribution— $P_{XTL-OSC}$

Operating Mode

$$P_{XTL-OSC} = PAC18$$

Standby Mode

$$P_{XTL-OSC} = PAC18$$

Sleep Mode

$$P_{XTL-OSC} = 0 \text{ W}$$

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.

Revision	Changes	Page
Advance v0.3 (continued)	The "Temperature Monitor" section was updated.	2-96
	EQ 2 is new.	2-103
	The "ADC Description" section was updated.	2-102
	Figure 2-16 • Fusion Clocking Options was updated.	2-20
	Table 2-46 • Analog Channel Specifications was updated.	2-118
	The notes in Table 2-72 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities were updated.	2-144
	The "Simultaneously Switching Outputs and PCB Layout" section is new.	2-149
	LVPECL and LVDS were updated in Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications.	2-157
	LVPECL and LVDS were updated in Table 2-82 • Fusion Pro I/O Attributes vs. I/O Standard Applications.	2-158
	The "Timing Model" was updated.	2-161
	All voltage-referenced Minimum and Maximum DC Input and Output Level tables were updated.	N/A
	All Timing Characteristic tables were updated	N/A
	Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated.	2-165
	Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated.	2-134
	Table 2-93 • I/O Output Buffer Maximum Resistances ¹ was updated.	2-171
	The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet.	2-211
	The "CoreMP7 and Cortex-M1 Software Tools" section is new.	2-257
	Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated.	2-165
	Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated.	2-134
	Table 2-93 • I/O Output Buffer Maximum Resistances ¹ was updated.	2-171
	The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet.	2-211
	The "108-Pin QFN" table for the AFS090 device is new.	3-2
	The "180-Pin QFN" table for the AFS090 device is new.	3-4
	The "208-Pin PQFP" table for the AFS090 device is new.	3-8
	The "256-Pin FBGA" table for the AFS090 device is new.	3-12
	The "256-Pin FBGA" table for the AFS250 device is new.	3-12