# E·XFL



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs600-fgg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a highly secure, low power, single-chip solution that is Instant On. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

## Flash Advantages

## Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flashbased Fusion devices are Instant On and do not need to be loaded from an external boot PROM.

On-board security mechanisms prevent access to the programming information and enable remote updates of the FPGA logic that are protected with high level security. Designers can perform remote insystem reprogramming to support future design iterations and field upgrades, with confidence that valuable IP is highly unlikely to be compromised or copied. ISP can be performed using the

industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

## Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a

built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with

AES-based security provide a high level of protection for remote field updates over public networks, such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with

industry-standard security, making remote ISP possible. A Fusion device provides the best available security for programmable logic designs.

## Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.



## **Fusion Stack Architecture**

To manage the unprecedented level of integration in Fusion devices, Microsemi developed the Fusion technology stack (Figure 2-1). This layered model offers a flexible design environment, enabling design at very high and very low levels of abstraction. Fusion peripherals include hard analog IP and hard and soft digital IP. Peripherals communicate across the FPGA fabric via a layer of soft gates—the Fusion backbone. Much more than a common bus interface, this Fusion backbone integrates a micro-sequencer within the FPGA fabric and configures the individual peripherals and supports low-level processing of peripheral data. Fusion applets are application building blocks that can control and respond to peripherals and other system signals. Applets can be rapidly combined to create large applications. The technology is scalable across devices, families, design types, and user expertise, and supports a well-defined interface for external IP and tool integration.

At the lowest level, Level 0, are Fusion peripherals. These are configurable functional blocks that can be hardwired structures such as a PLL or analog input channel, or soft (FPGA gate) blocks such as a UART or two-wire serial interface. The Fusion peripherals are configurable and support a standard interface to facilitate communication and implementation.

Connecting and controlling access to the peripherals is the Fusion backbone, Level 1. The backbone is a soft-gate structure, scalable to any number of peripherals. The backbone is a bus and much more; it manages peripheral configuration to ensure proper operation. Leveraging the common peripheral interface and a low-level state machine, the backbone efficiently offloads peripheral management from the system design. The backbone can set and clear flags based upon peripheral behavior and can define performance criteria. The flexibility of the stack enables a designer to configure the silicon, directly bypassing the backbone if that level of control is desired.

One step up from the backbone is the Fusion applet, Level 2. The applet is an application building block that implements a specific function in FPGA gates. It can react to stimuli and board-level events coming through the backbone or from other sources, and responds to these stimuli by accessing and manipulating peripherals via the backbone or initiating some other action. An applet controls or responds to the peripheral(s). Applets can be easily imported or exported from the design environment. The applet structure is open and well-defined, enabling users to import applets from Microsemi, system developers, third parties, and user groups.



Note: Levels 1, 2, and 3 are implemented in FPGA logic gates.

Figure 2-1 • Fusion Architecture Stack



## **Array Coordinates**

During many place-and-route operations in the Microsemi Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

		Vers	saTiles		Memor	y Rows	All		
Device	Min.		Max.		Bottom	Тор	Min.	Max.	
	x	У	x	У	(x, y)	(x, y)	(x, y)	(x, y)	
AFS090	3	2	98	25	None	(3, 26)	(0, 0)	(101, 29)	
AFS250	3	2	130	49	None	(3, 50)	(0, 0)	(133, 53)	
AFS600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)	
AFS1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 129)	

#### Table 2-3 • Array Coordinates









## Table 2-7 • AFS250 Global Resource Timing<br/>Commercial Temperature Range Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V

Paramotor	Description	_	·2	-	-1	St	Unite	
Faranieter	Description	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Units
t <sub>RCKL</sub>	Input Low Delay for Global Clock	0.89	1.12	1.02	1.27	1.20	1.50	ns
t <sub>RCKH</sub>	Input High Delay for Global Clock	0.88	1.14	1.00	1.30	1.17	1.53	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width High for Global Clock							ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width Low for Global Clock							ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.26		0.30		0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

## Table 2-8 • AFS090 Global Resource Timing

Commercial Temperature Range Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-	2	-	1	S	Unite	
Falailletei	Description	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Units
t <sub>RCKL</sub>	Input Low Delay for Global Clock	0.84	1.07	0.96	1.21	1.13	1.43	ns
t <sub>RCKH</sub>	Input High Delay for Global Clock	0.83	1.10	0.95	1.25	1.12	1.47	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width High for Global Clock							ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width Low for Global Clock							ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.27		0.30		0.36	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

#### **Program Operation**

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, the total programming (including erase) time per page of the eNVM is 6.8 ms. While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified. Program errors include the following:

- 1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
- 2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
- Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
- 4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
- 5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
- 6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
- 7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in Figure 2-36.



#### Figure 2-36 • FB Program Waveform

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.

#### Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven
  onto the RD bus in the same clock cycle following RA and REN valid. The read address is
  registered on the read port clock active edge, and data appears at RD after the RAM access time.
  Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is High. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "SRAM Characteristics" section on page 2-63 and the "FIFO Characteristics" section on page 2-72.

#### **RAM** Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG IEEE 1532" section on page 2-229 and the *Fusion SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.



The following signals are used to configure the FIFO4K18 memory element.

#### WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-33).

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WW2, WW1, WW0	RW2, RW1, RW0	D×W
000	000	4k×1
001	001	2k×2
010	010	1k×4
011	011	512×9
100	100	256×18
101, 110, 111	101, 110, 111	Reserved

#### WBLK and RBLK

These signals are active low and will enable the respective ports when Low. When the RBLK signal is High, the corresponding port's outputs hold the previous value.

#### WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

#### WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

#### **RPIPE**

This signal is used to specify pipelined read on the output. A Low on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

#### RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins Low, the FULL and AFULL pins Low, and the EMPTY and AEMPTY pins High (Table 2-34).

Table 2-34 • Input Data Signal Usage for Different Aspect Ratios

D×W	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	-

#### WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-34).

#### RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-34).



To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least  $t_{CMSLO}$  in order to discharge the previous measurement. Then CMSTB must be asserted high for at least  $t_{CMSET}$  prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is de-asserted by the AB macro. Note that the minimum sample time cannot be less than  $t_{CMSHI}$ . Figure 2-71 shows the timing diagram of CMSTB in relationship with the ADC control signals.



Figure 2-71 • Timing Diagram for Current Monitor Strobe

Figure 2-72 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050  $\Omega$  sense resistor, The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$||| = (ADC \times V_{AREF}) / (10 \times 2^{N} \times R_{sense})$$

EQ 3

where

I is the current flowing through the sense resistor

ADC is the result from the ADC

VAREF is the Reference voltage

N is the number of bits

Rsense is the resistance of the sense resistor

The diode's voltage is measured at each current level and the temperature is calculated based on EQ 7.

$$V_{\text{TMSLO}} - V_{\text{TMSHI}} = n \frac{kT}{q} \left( \ln \frac{I_{\text{TMSLO}}}{I_{\text{TMSHI}}} \right)$$

EQ 7

where

 $\textit{I}_{\textit{TMSLO}}$  is the current when the Temperature Strobe is Low, typically 100  $\mu A$ 

 $I_{TMSHI}$  is the current when the Temperature Strobe is High, typically 10  $\mu A$ 

*V<sub>TMSLO</sub>* is diode voltage while Temperature Strobe is Low

 $V_{TMSHI}$  is diode voltage while Temperature Strobe is High

n is the non-ideality factor of the diode-connected transistor. It is typically 1.004 for the Microsemirecommended transistor type 2N3904.

- $K = 1.3806 \text{ x } 10^{-23} \text{ J/K}$  is the Boltzman constant
- $Q = 1.602 \times 10^{-19} C$  is the charge of a proton

When  $I_{TMSLO} / I_{TMSHI} = 10$ , the equation can be simplified as shown in EQ 8.

$$\Delta V = V_{\text{TMSLO}} - V_{\text{TMSHI}} = 1.986 \times 10^{-4} nT$$

EQ 8

In the Fusion TMB, the ideality factor *n* for 2N3904 is 1.004 and  $\Delta V$  is amplified 12.5 times by an internal amplifier; hence the voltage before entering the ADC is as given in EQ 9.

$$V_{ADC} = \Delta V \times 12.5 = 2.5 \text{ mV}/(K \times T)$$

EQ 9

This means the temperature to voltage relationship is 2.5 mV per degree Kelvin. The unique design of Fusion has made the Temperature Monitor System simple for the user. When the 10-bit mode ADC is used, each LSB represents 1 degree Kelvin, as shown in EQ 10. That is, e. 25°C is equal to 293°K and is represented by decimal 293 counts from the ADC.

$$1K = 2.5 \text{ mV} \times \frac{2^{10}}{2.56 \text{ V}} = 1 \text{ LSB}$$

EQ 10

If 8-bit mode is used for the ADC resolution, each LSB represents 4 degrees Kelvin; however, the resolution remains as 1 degree Kelvin per LSB, even for 12-bit mode, due to the Temperature Monitor design. An example of the temperature data format for 10-bit mode is shown in Table 2-38.

Temperature	Temperature (K)	Digital Output (ADC 10-bit mode)
-40°C	233	00 1110 1001
–20°C	253	00 1111 1101
0°C	273	01 0001 0001
1°C	274	01 0001 0010
10 °C	283	01 0001 1011
25°C	298	01 0010 1010
50 °C	323	01 0100 0011
85 °C	358	01 0110 0110

Table 2-38 • Temperature Data Format



## **Hot-Swap Support**

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-74. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

Table 2-74 • Levels of Hot-Swap Support

Hot Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain Fusion Devices	Compliance of Fusion Devices
1	Cold-swap	No	-	_	_	System and card with Microsemi FPGA chip are powered down, then card gets plugged into system, then power supplies are turned on for system but not for FPGA on card.	Compliant I/Os can but do not have to be set to hot insertion mode.
2	Hot-swap while reset	Yes	Held in reset state	Must be made and maintained for 1 ms before, during, and after insertion/ removal	_	In PCI hot plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant I/Os can but do not have to be set to hot insertion mode.
3	Hot-swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/re moval)	Same as Level 2	Must remain glitch-free during power-up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on bus. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.
4	Hot-swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle.	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.



#### Table 2-85 • Fusion Pro I/O Attributes vs. I/O Standard Applications

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3	3	3	3	3
PCI (3.3 V)			3		3	3	3	3		
PCI-X (3.3 V)	3		3		3	3	3	3		
GTL+ (3.3 V)			3		3	3	3	3		3
GTL+ (2.5 V)			3		3	3	3	3		3
GTL (3.3 V)			3		3	3	3	3		3
GTL (2.5 V)			3		3	3	3	3		3
HSTL Class I			3		3	3	3	3		3
HSTL Class II			3		3	3	3	3		3
SSTL2 Class I and II			3		3	3	3	3		3
SSTL3 Class I and II			3		3	3	3	3		3
LVDS, BLVDS, M-LVDS			3			3	3	3		3
LVPECL						3	3	3		3



## Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions

			VIL		VIH		VOL	VOH	IOL	ЮН
I/O Standard	Drive Strength	Slew Rate	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	-0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	-0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4
1.5 V LVCMOS	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Applicable to Standard I/Os

*Note:* Currents are measured at 85°C junction temperature.

#### Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

Applicable to All I/O Bank Types

	Commercial <sup>1</sup>		Industrial <sup>2</sup>			
	IIL <sup>3</sup>	IIH <sup>4</sup>	IIL <sup>3</sup>	IIH <sup>4</sup>		
DC I/O Standards	μΑ	μΑ	μΑ	μA		
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15		
2.5 V LVCMOS	10	10	15	15		
1.8 V LVCMOS	10	10	15	15		
1.5 V LVCMOS	10	10	15	15		
3.3 V PCI	10	10	15	15		
3.3 V PCI-X	10	10	15	15		
3.3 V GTL	10	10	15	15		
2.5 V GTL	10	10	15	15		
3.3 V GTL+	10	10	15	15		
2.5 V GTL+	10	10	15	15		
HSTL (I)	10	10	15	15		
HSTL (II)	10	10	15	15		
SSTL2 (I)	10	10	15	15		
SSTL2 (II)	10	10	15	15		
SSTL3 (I)	10	10	15	15		
SSTL3 (II)	10	10	15	15		

Notes:

1. Commercial range ( $0^{\circ}C < T_J < 85^{\circ}C$ )

2. Industrial range  $(-40^{\circ}C < T_{J} < 100^{\circ}C)$ 

3. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

4. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.



## Table 2-96 • I/O Output Buffer Maximum Resistances <sup>1</sup> (continued)

Standard	Drive Strength	R <sub>PULL-DOWN</sub> (ohms) <sup>2</sup>	R <sub>PULL-UP</sub> (ohms) <sup>3</sup>							
Applicable to Standard I/O Banks										
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300							
	4 mA	100	300							
	6 mA	50	150							
	8 mA	50	150							
2.5 V LVCMOS	2 mA	100	200							
	4 mA	100	200							
	6 mA	50	100							
	8 mA	50	100							
1.8 V LVCMOS	2 mA	200	225							
	4 mA	100	112							
1.5 V LVCMOS	2 mA	200	224							

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.

2. R<sub>(PULL-DOWN-MAX)</sub> = VOLspec / I<sub>OLspec</sub>

3. R<sub>(PULL-UP-MAX)</sub> = (VCCImax – VOHspec) / IOHspec

#### Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	R <sub>(WEAK I</sub> (oh	PULL-UP) ms)	R <sub>(WEAK PULL-DOWN)</sub> <sup>2</sup> (ohms)		
VCCI	Min.	Max.	Min.	Max.	
3.3 V	10 k	45 k	10 k	45 k	
2.5 V	11 k	55 k	12 k	74 k	
1.8 V	18 k	70 k	17 k	110 k	
1.5 V	19 k	90 k	19 k	140 k	

Notes:

R<sub>(WEAK PULL-UP-MAX)</sub> = (VCCImax – VOHspec) / I<sub>WEAK PULL-UP-MIN</sub>
 R<sub>(WEAK PULL-DOWN-MAX)</sub> = VOLspec / I<sub>WEAK PULL-DOWN-MIN</sub>



#### Table 2-115 • 2.5 V LVCMOS High Slew

Commercial Temperature Range Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Advanced I/Os

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	Units
4 mA	Std.	0.66	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	-1	0.56	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	-2	0.49	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
8 mA	Std.	0.66	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	-1	0.56	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	-2	0.49	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	-1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	-2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
16 mA	Std.	0.66	3.35	0.04	1.31	0.43	3.41	3.06	3.36	3.55	5.65	5.30	ns
	-1	0.56	2.85	0.04	1.11	0.36	2.90	2.60	2.86	3.02	4.81	4.51	ns
	-2	0.49	2.50	0.03	0.98	0.32	2.55	2.29	2.51	2.65	4.22	3.96	ns
24 mA	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	-1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	-2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

#### Table 2-116 • 2.5 V LVCMOS Low Slew

Commercial Temperature Range Conditions:  $T_J$  = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Standard I/Os

Drive Strongth	Speed										Unito
Strength	Grade	LOOUT	۱DP	LDIN	٩PY	LEOUT	۲ZL	۲ZH	۲LZ	ЧНZ	Units
2 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	-1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	-2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
4 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	-1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	-2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
6 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	-1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	-2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns
8 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	-1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	-2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



#### SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-162 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL¹	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
14 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI - 1.1	14	14	54	51	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



#### Figure 2-132 • AC Loading

#### Table 2-163 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

#### Timing Characteristics

Table 2-164 • SSTL3 Class I

Commercial Temperature Range Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t <sub>dout</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
Std.	0.66	2.31	0.04	1.25	0.43	2.35	1.84			4.59	4.07	ns
-1	0.56	1.96	0.04	1.06	0.36	2.00	1.56			3.90	3.46	ns
-2	0.49	1.72	0.03	0.93	0.32	1.75	1.37			3.42	3.04	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



#### LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-136. The building blocks of the LVPECL transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.



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DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3	.0	3	.3	3.	6	V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

#### Table 2-171 • Minimum and Maximum DC Input and Output Levels

#### Table 2-172 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	
1.64	1.94	Cross point	_	

*Note:* \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

#### Timing Characteristics

#### Table 2-173 • LVPECL

Commercial Temperature Range Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/Os

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	Units
Std.	0.66	2.14	0.04	1.63	ns
-1	0.56	1.82	0.04	1.39	ns
-2	0.49	1.60	0.03	1.22	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

## Methodology

#### Total Power Consumption—PTOTAL

#### Operating Mode, Standby Mode, and Sleep Mode

 $P_{TOTAL} = P_{STAT} + P_{DYN}$ 

P<sub>STAT</sub> is the total static power consumption.

P<sub>DYN</sub> is the total dynamic power consumption.

#### Total Static Power Consumption—P<sub>STAT</sub>

#### **Operating Mode**

 $\label{eq:pstat} \begin{array}{l} \mathsf{P}_{\mathsf{STAT}} = \mathsf{PDC1} + (\mathsf{N}_{\mathsf{NVM-BLOCKS}} * \mathsf{PDC4}) + \mathsf{PDC5} + (\mathsf{N}_{\mathsf{QUADS}} * \mathsf{PDC6}) + (\mathsf{N}_{\mathsf{INPUTS}} * \mathsf{PDC7}) + (\mathsf{N}_{\mathsf{OUTPUTS}} * \mathsf{PDC8}) + (\mathsf{N}_{\mathsf{PLLS}} * \mathsf{PDC9}) \end{array}$ 

 $N_{\ensuremath{\mathsf{NVM}}\xspace-BLOCKS}$  is the number of NVM blocks available in the device.

 $N_{QUADS}$  is the number of Analog Quads used in the design.

N<sub>INPUTS</sub> is the number of I/O input buffers used in the design.

N<sub>OUTPUTS</sub> is the number of I/O output buffers used in the design.

N<sub>PLLS</sub> is the number of PLLs available in the device.

#### Standby Mode

P<sub>STAT</sub> = PDC2

#### Sleep Mode

P<sub>STAT</sub> = PDC3

#### Total Dynamic Power Consumption—P<sub>DYN</sub>

#### **Operating Mode**

P<sub>DYN</sub> = P<sub>CLOCK</sub> + P<sub>S-CELL</sub> + P<sub>C-CELL</sub> + P<sub>NET</sub> + P<sub>INPUTS</sub> + P<sub>OUTPUTS</sub> + P<sub>MEMORY</sub> + P<sub>PLL</sub> + P<sub>NVM</sub>+ P<sub>XTL-OSC</sub> + P<sub>RC-OSC</sub> + P<sub>AB</sub>

#### Standby Mode

 $P_{DYN} = P_{XTL-OSC}$ 

Sleep Mode

 $P_{DYN} = 0 W$ 

#### Global Clock Dynamic Contribution—P<sub>CLOCK</sub>

#### **Operating Mode**

 $P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$ 

N<sub>SPINE</sub> is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

N<sub>ROW</sub> is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

 $\mathsf{F}_{\mathsf{CLK}}$  is the global clock signal frequency.

N<sub>S-CELL</sub> is the number of VersaTiles used as sequential modules in the design.

#### Standby Mode and Sleep Mode

 $P_{CLOCK} = 0 W$ 

#### Sequential Cells Dynamic Contribution—P<sub>S-CELL</sub>

#### **Operating Mode**

## Example of Power Calculation

This example considers a shift register with 5,000 storage tiles, including a counter and memory that stores analog information. The shift register is clocked at 50 MHz and stores and reads information from a RAM.

The device used is a commercial AFS600 device operating in typical conditions.

The calculation below uses the power calculation methodology previously presented and shows how to determine the dynamic and static power consumption of resources used in the application.

Also included in the example is the calculation of power consumption in operating, standby, and sleep modes to illustrate the benefit of power-saving modes.

#### Global Clock Contribution—P<sub>CLOCK</sub>

 $F_{CLK}$  = 50 MHz Number of sequential VersaTiles: N<sub>S-CELL</sub> = 5,000 Estimated number of Spines: N<sub>SPINES</sub> = 5 Estimated number of Rows: N<sub>ROW</sub> = 313

#### **Operating Mode**

$$\begin{split} & \mathsf{P}_{\mathsf{CLOCK}} = (\mathsf{PAC1} + \mathsf{N}_{\mathsf{SPINE}} * \mathsf{PAC2} + \mathsf{N}_{\mathsf{ROW}} * \mathsf{PAC3} + \mathsf{N}_{\mathsf{S}\text{-}\mathsf{CELL}} * \mathsf{PAC4}) * \mathsf{F}_{\mathsf{CLK}} \\ & \mathsf{P}_{\mathsf{CLOCK}} = (0.0128 + 5 * 0.0019 + 313 * 0.00081 + 5,000 * 0.00011) * 50 \\ & \mathsf{P}_{\mathsf{CLOCK}} = 41.28 \ \mathsf{mW} \end{split}$$

#### Standby Mode and Sleep Mode

 $P_{CLOCK} = 0 W$ 

Logic—Sequential Cells, Combinational Cells, and Routing Net Contributions— $P_{S-CELL}$ ,  $P_{C-CELL}$ , and  $P_{NET}$ 

 $\label{eq:F_CLK} \ensuremath{\mathsf{F_{CLK}}}\xspace = 50 \ensuremath{\,\mathsf{MHz}}\xspace \\ \ensuremath{\mathsf{Number}}\xspace of sequential VersaTiles: \ensuremath{\mathsf{N}_{S-CELL}}\xspace = 5,000 \\ \ensuremath{\mathsf{Number}}\xspace of versaTiles: \ensuremath{\mathsf{N}_{C-CELL}}\xspace = 6,000 \\ \ensuremath{\mathsf{Estimated}}\xspace toggle rate of VersaTile outputs: \ensuremath{\alpha_1}\xspace = 0.1 \ensuremath{\,(10\%)}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{$ 

#### **Operating Mode**

$$\begin{split} \mathsf{P}_{S\text{-}CELL} &= \mathsf{N}_{S\text{-}CELL} * (\mathsf{P}_{\mathsf{AC5}}\text{+} (\alpha_1 \, / \, 2) * \mathsf{PAC6}) * \mathsf{F}_{\mathsf{CLK}} \\ \mathsf{P}_{S\text{-}CELL} &= 5,000 * (0.00007 + (0.1 \, / \, 2) * 0.00029) * 50 \\ \mathsf{P}_{S\text{-}CELL} &= 21.13 \text{ mW} \end{split}$$

 $P_{C-CELL} = N_{C-CELL}^* (\alpha_1 / 2) * PAC7 * F_{CLK}$  $P_{C-CELL} = 6,000 * (0.1 / 2) * 0.00029 * 50$  $P_{C-CELL} = 4.35 \text{ mW}$ 

$$\begin{split} \mathsf{P}_{\mathsf{NET}} &= (\mathsf{N}_{\mathsf{S}\text{-}\mathsf{CELL}} + \mathsf{N}_{\mathsf{C}\text{-}\mathsf{CELL}}) * (\alpha_1 \,/\, 2) * \mathsf{PAC8} * \mathsf{F}_{\mathsf{CLK}} \\ \mathsf{P}_{\mathsf{NET}} &= (5,000 + 6,000) * (0.1 \,/\, 2) * 0.0007 * 50 \\ \mathsf{P}_{\mathsf{NET}} &= 19.25 \text{ mW} \end{split}$$

 $P_{LOGIC} = P_{S-CELL} + P_{C-CELL} + P_{NET}$  $P_{LOGIC} = 21.13 \text{ mW} + 4.35 \text{ mW} + 19.25 \text{ mW}$  $P_{LOGIC} = 44.73 \text{ mW}$ 

Standby Mode and Sleep Mode

## **Microsemi**

Package Pin Assignments

	FG676		FG676		FG676
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	Pin Number	AFS1500 Function
A1	NC	AA11	AV2	AB21	PTBASE
A2	GND	AA12	GNDA	AB22	GNDNVM
A3	NC	AA13	AV3	AB23	VCCNVM
A4	NC	AA14	AV6	AB24	VPUMP
A5	GND	AA15	GNDA	AB25	NC
A6	NC	AA16	AV7	AB26	GND
A7	NC	AA17	AV8	AC1	NC
A8	GND	AA18	GNDA	AC2	NC
A9	IO17NDB0V2	AA19	AV9	AC3	NC
A10	IO17PDB0V2	AA20	VCCIB2	AC4	GND
A11	GND	AA21	IO68PPB2V0	AC5	VCCIB4
A12	IO18NDB0V2	AA22	ТСК	AC6	VCCIB4
A13	IO18PDB0V2	AA23	GND	AC7	PCAP
A14	IO20NDB0V2	AA24	IO76PPB2V0	AC8	AG0
A15	IO20PDB0V2	AA25	VCCIB2	AC9	GNDA
A16	GND	AA26	NC	AC10	AG1
A17	IO21PDB0V2	AB1	GND	AC11	AG2
A18	IO21NDB0V2	AB2	NC	AC12	GNDA
A19	GND	AB3	GEC2/IO87PDB4V0	AC13	AG3
A20	IO39NDB1V2	AB4	IO87NDB4V0	AC14	AG6
A21	IO39PDB1V2	AB5	GEA2/IO85PDB4V0	AC15	GNDA
A22	GND	AB6	IO85NDB4V0	AC16	AG7
A23	NC	AB7	NCAP	AC17	AG8
A24	NC	AB8	AC0	AC18	GNDA
A25	GND	AB9	VCC33A	AC19	AG9
A26	NC	AB10	AC1	AC20	VAREF
AA1	NC	AB11	AC2	AC21	VCCIB2
AA2	VCCIB4	AB12	VCC33A	AC22	PTEM
AA3	IO93PDB4V0	AB13	AC3	AC23	GND
AA4	GND	AB14	AC6	AC24	NC
AA5	IO93NDB4V0	AB15	VCC33A	AC25	NC
AA6	GEB2/IO86PDB4V0	AB16	AC7	AC26	NC
AA7	IO86NDB4V0	AB17	AC8	AD1	NC
AA8	AV0	AB18	VCC33A	AD2	NC
AA9	GNDA	AB19	AC9	AD3	GND
AA10	AV1	AB20	ADCGNDREF	AD4	NC



Revision	Changes	Page
Advance v1.5 (continued)	This bullet was added to the "Integrated A/D Converter (ADC) and Analog I/O" section: ADC Accuracy is Better than 1%	I
	In the "Integrated Analog Blocks and Analog I/Os" section, ±4 LSB was changed to 0.72. The following sentence was deleted:	1-4
	The input range for voltage signals is from $-12$ V to $+12$ V with full-scale output values from 0.125 V to 16 V.	l
	In addition, 2°C was changed to 3°C:	1
	"One analog input in each quad can be connected to an external temperature monitor diode and achieves detection accuracy of ±3°C."	1
	The following sentence was deleted:	1
	The input range for voltage signals is from $-12$ V to $+12$ V with full-scale output values from 0.125 V to 16 V.	1
	The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA.	N/A
Advance v1.4 (July 2008)	In Table 3-8 · Quiescent Supply Current Characteristics (IDDQ)1, footnote references were updated for $I_{DC2}$ and $I_{DC3}$ . Footnote 3 and 4 were updated and footnote 5 is new.	3-11
Advance v1 3	The "ADC Description" section was significantly updated. Please review carefully	2-102
(July 2008)		
Advance v1.2 (May 2008)	Table 2-25 • Flash Memory Block Timing was significantly updated.	2-55
	The "V <sub>AREF</sub> Analog Reference Voltage" pin description section was significantly update. Please review it carefully.	2-226
	Table 2-45 • ADC Interface Timing was significantly updated.	2-110
	Table 2-56 • Direct Analog Input Switch Control Truth Table—AV ( $x = 0$ ), AC ( $x = 1$ ), and AT ( $x = 3$ ) was significantly updated.	2-131
	The following sentence was deleted from the "Voltage Monitor" section:	2-86
	The Analog Quad inputs are tolerant up to 12 V + 10%.	l
	The "180-Pin QFN" figure was updated. D1 to D4 are new and the figure was changed to bottom view. The note below the figure is new.	3-3
Advance v1.1 (May 2008)	The following text was incorrect and therefore deleted:	2-204
	VCC33A Analog Power Filter	1
	Analog power pin for the analog power supply low-pass filter. An external 100 pF capacitor should be connected between this pin and ground.	l
	There is still a description of V <sub>CC33A</sub> on page 2-224.	L