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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 119 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-1fg256i |

1 – Fusion Device Family Overview

Introduction

The Fusion mixed signal FPGA satisfies the demand from system architects for a device that simplifies design and unleashes their creativity. As the world's first mixed signal programmable logic family, Fusion integrates mixed signal analog, flash memory, and FPGA fabric in a monolithic device. Fusion devices enable designers to quickly move from concept to completed design and then deliver feature-rich systems to market. This new technology takes advantage of the unique properties of Microsemi flash-based FPGAs, including a high-isolation, triple-well process and the ability to support high-voltage transistors to meet the demanding requirements of mixed signal system design.

Fusion mixed signal FPGAs bring the benefits of programmable logic to many application areas, including power management, smart battery charging, clock generation and management, and motor control. Until now, these applications have only been implemented with costly and space-consuming discrete analog components or mixed signal ASIC solutions. Fusion mixed signal FPGAs present new capabilities for system development by allowing designers to integrate a wide range of functionality into a single device, while at the same time offering the flexibility of upgrades late in the manufacturing process or after the device is in the field. Fusion devices provide an excellent alternative to costly and time-consuming mixed signal ASIC designs. In addition, when used in conjunction with the ARM Cortex-M1 processor, Fusion technology represents the definitive mixed signal FPGA platform.

Flash-based Fusion devices are Instant On. As soon as system power is applied and within normal operating specifications, Fusion devices are working. Fusion devices have a 128-bit flash-based lock and industry-leading AES decryption, used to secure programmed intellectual property (IP) and configuration data. Fusion devices are the most comprehensive single-chip analog and digital programmable logic solution available today.

To support this new ground-breaking technology, Microsemi has developed a series of major tool innovations to help maximize designer productivity. Implemented as extensions to the popular Microsemi Libero[®] System-on-Chip (SoC) software, these new tools allow designers to easily instantiate and configure peripherals within a design, establish links between peripherals, create or import building blocks or reference designs, and perform hardware verification. This tool suite will also add comprehensive hardware/software debug capability as well as a suite of utilities to simplify development of embedded soft-processor-based solutions.

General Description

The Fusion family, based on the highly successful ProASIC[®]3 and ProASIC3E flash FPGA architecture, has been designed as a high-performance, programmable, mixed signal platform. By combining an advanced flash FPGA core with flash memory blocks and analog peripherals, Fusion devices dramatically simplify system design and, as a result, dramatically reduce overall system cost and board space.

The state-of-the-art flash memory technology offers high-density integrated flash memory blocks, enabling savings in cost, power, and board area relative to external flash solutions, while providing increased flexibility and performance. The flash memory blocks and integrated analog peripherals enable true mixed-mode programmable logic designs. Two examples are using an on-chip soft processor to implement a fully functional flash MCU and using high-speed FPGA logic to offer system and power supervisory capabilities. Instant On, and capable of operating from a single 3.3 V supply, the Fusion family is ideally suited for system management and control applications.

The devices in the Fusion family are categorized by FPGA core density. Each family member contains many peripherals, including flash memory blocks, an analog-to-digital-converter (ADC), high-drive outputs, both RC and crystal oscillators, and a real-time counter (RTC). This provides the user with a high level of flexibility and integration to support a wide variety of mixed signal applications. The flash memory block capacity ranges from 2 Mbits to 8 Mbits. The integrated 12-bit ADC supports up to 30 independently configurable input channels.

VersaTile Characteristics

Sample VersaTile Specifications—Combinatorial Module

The Fusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library (Figure 2-3). For more details, refer to the *IGLOO*, *ProASIC3*, *SmartFusion*, and *Fusion Macro Library Guide*.

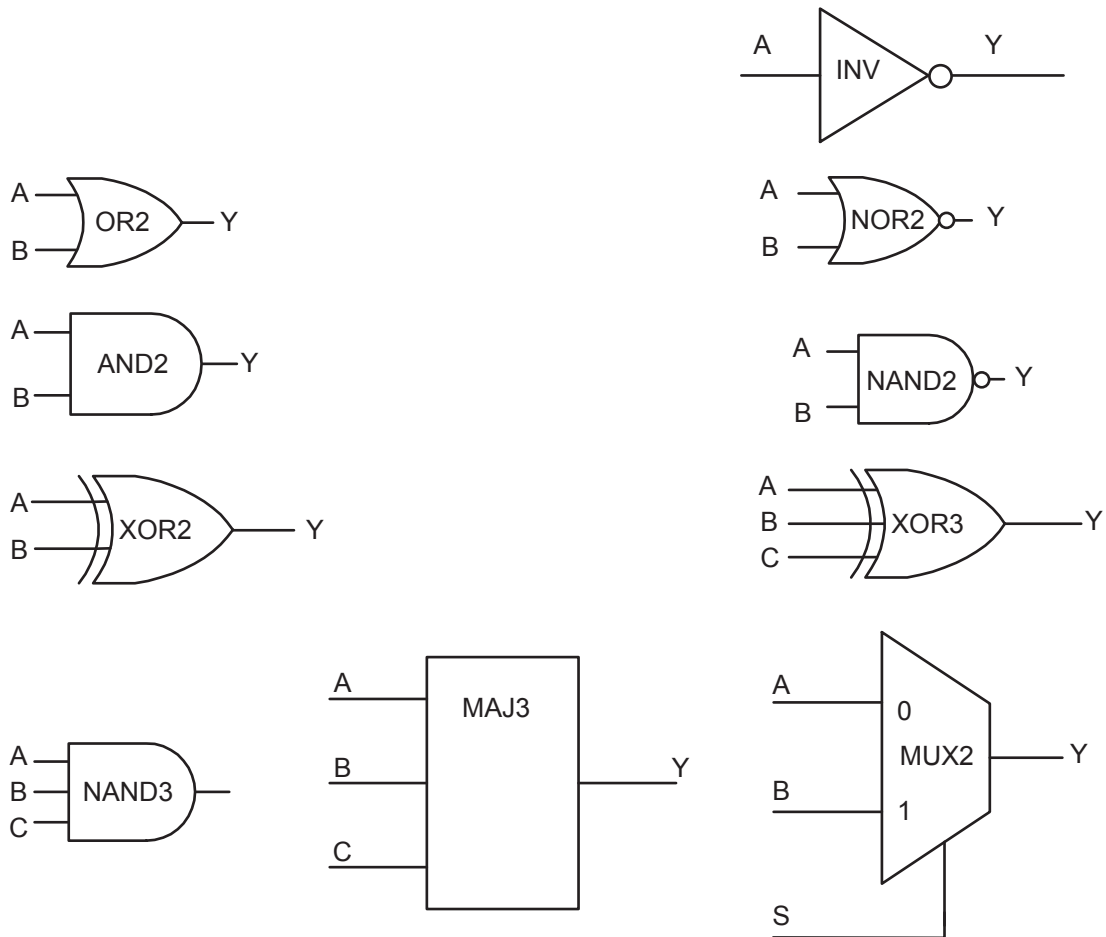


Figure 2-3 • Sample of Combinatorial Cells

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As [Figure 2-14](#) indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the [Using Global Resources in Actel Fusion Devices](#) application note.

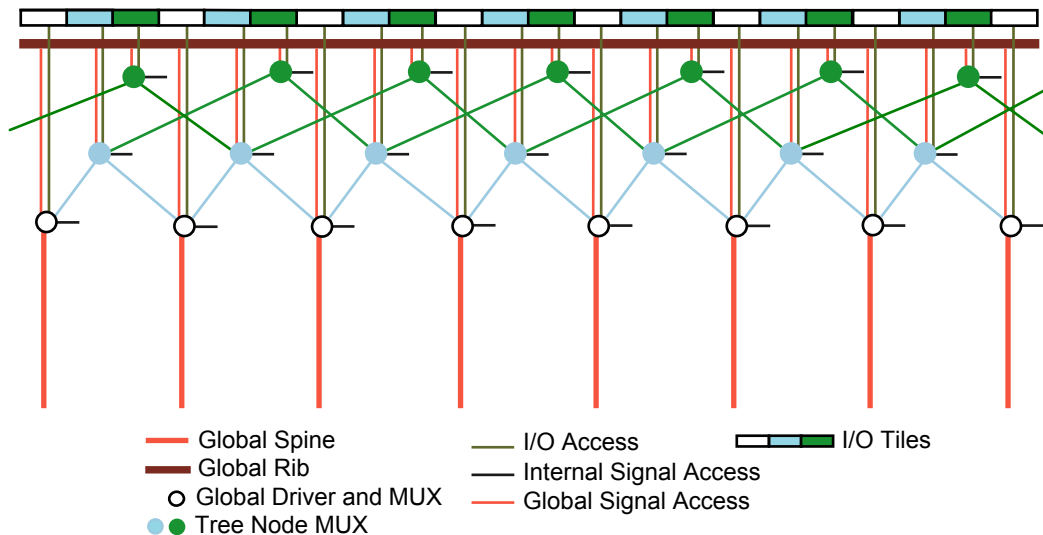
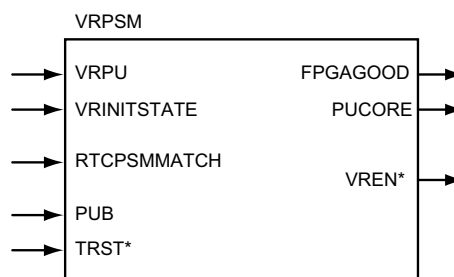


Figure 2-14 • Clock Aggregation Tree Architecture

Voltage Regulator and Power System Monitor (VRPSM)

The VRPSM macro controls the power-up state of the FPGA. The power-up bar (PUB) pin can turn on the voltage regulator when set to 0. TRST can enable the voltage regulator when deasserted, allowing the FPGA to power-up when user want access to JTAG ports. The inputs VRINITSTATE and RTCPSMMATCH come from the flash bits and RTC, and can also power up the FPGA.



Note: *Signals are hardwired internally and do not exist in the macro core.

Figure 2-30 • VRPSM Macro

Table 2-17 • VRPSM Signal Descriptions

| Signal Name | Width | Direction | Function |
|-------------|-------|-----------|--|
| VRPU | 1 | In | Voltage Regulator Power-Up 0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator. 1 – Voltage regulator enabled |
| VRINITSTATE | 1 | In | Voltage Regulator Initial State Defines the voltage Regulator status upon power-up of the 3.3 V. The signal is configured by Libero SoC when the VRPSM macro is generated. Tie off to 1 – Voltage regulator enables when 3.3 V is powered. Tie off to 0 – Voltage regulator disables when 3.3 V is powered. |
| RTCPSMMATCH | 1 | In | RTC Power System Management Match Connect from RTCPSMATCH signal from RTC in AB 0 transition to 1 turns on the voltage regulator |
| PUB | 1 | In | External pin, built-in weak pull-up Power-Up Bar 0 – Enables voltage regulator at all times |
| TRST* | 1 | In | External pin, JTAG Test Reset 1 – Enables voltage regulator at all times |
| FPGAGOOD | 1 | Out | Indicator that the FPGA is powered and functional No need to connect if it is not used. 1 – Indicates that the FPGA is powered up and functional. 0 – Not possible to read by FPGA since it has already powered off. |
| PUCORE | 1 | Out | Power-Up Core Inverted signal of PUB. No need to connect if it is not used. |
| VREN* | 1 | Out | Voltage Regulator Enable Connected to 1.5 V voltage regulator in Fusion device internally. 0 – Voltage regulator disables 1 – Voltage regulator enables |

Note: *Signals are hardwired internally and do not exist in the macro core.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

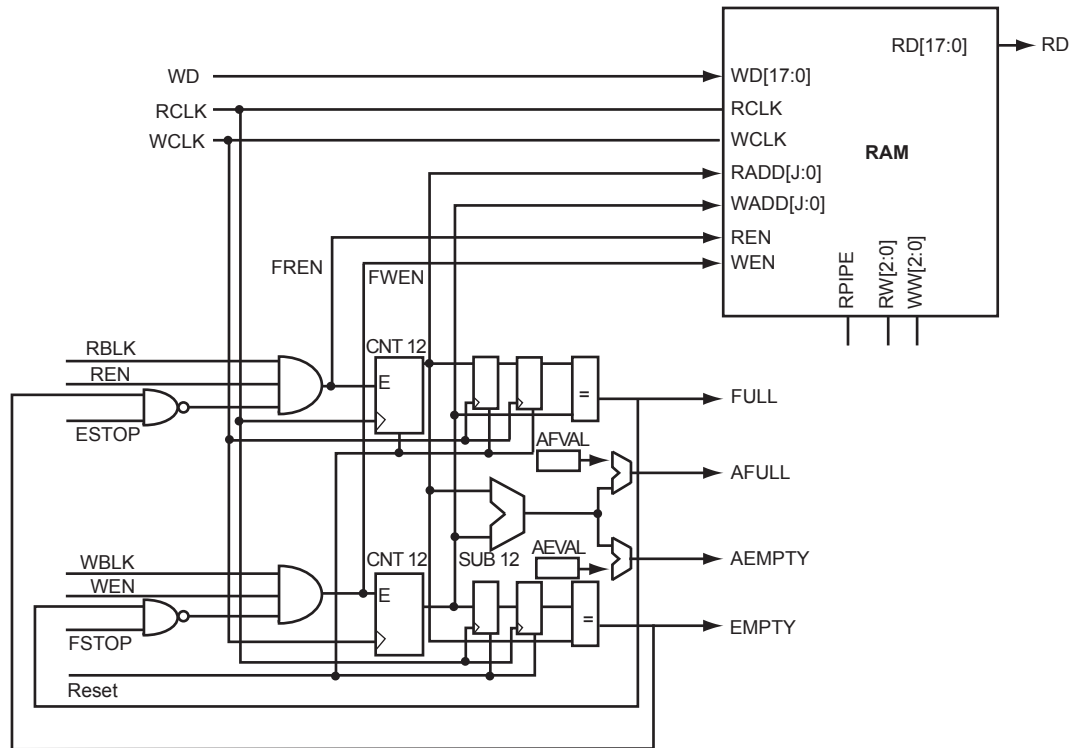


Figure 2-47 • Fusion RAM Block with Embedded FIFO Controller

Analog Block

With the Fusion family, Microsemi has introduced the world's first mixed-mode FPGA solution. Supporting a robust analog peripheral mix, Fusion devices will support a wide variety of applications. It is this Analog Block that separates Fusion from all other FPGA solutions on the market today.

By combining both flash and high-speed CMOS processes in a single chip, these devices offer the best of both worlds. The high-performance CMOS is used for building RAM resources. These high-performance structures support device operation up to 350 MHz. Additionally, the advanced Microsemi 0.13 μm flash process incorporates high-voltage transistors and a high-isolation, triple-well process. Both of these are suited for the flash-based programmable logic and nonvolatile memory structures.

High-voltage transistors support the integration of analog technology in several ways. They aid in noise immunity so that the analog portions of the chip can be better isolated from the digital portions, increasing analog accuracy. Because they support high voltages, Microsemi flash FPGAs can be connected directly to high-voltage input signals, eliminating the need for external resistor divider networks, reducing component count, and increasing accuracy. By supporting higher internal voltages, the Microsemi advanced flash process enables high dynamic range on analog circuitry, increasing precision and signal-noise ratio. Microsemi flash FPGAs also drive high-voltage outputs, eliminating the need for external level shifters and drivers.

The unique triple-well process enables the integration of high-performance analog features with increased noise immunity and better isolation. By increasing the efficiency of analog design, the triple-well process also enables a smaller overall design size, reducing die size and cost.

The Analog Block consists of the Analog Quad I/O structure, RTC (for details refer to the ["Real-Time Counter System" section on page 2-31](#)), ADC, and ACM. All of these elements are combined in the single Analog Block macro, with which the user implements this functionality ([Figure 2-64](#)).

The Analog Block needs to be reset/reinitialized after the core powers up or the device is programmed. An external reset/initialize signal, which can come from the internal voltage regulator when it powers up, must be applied.

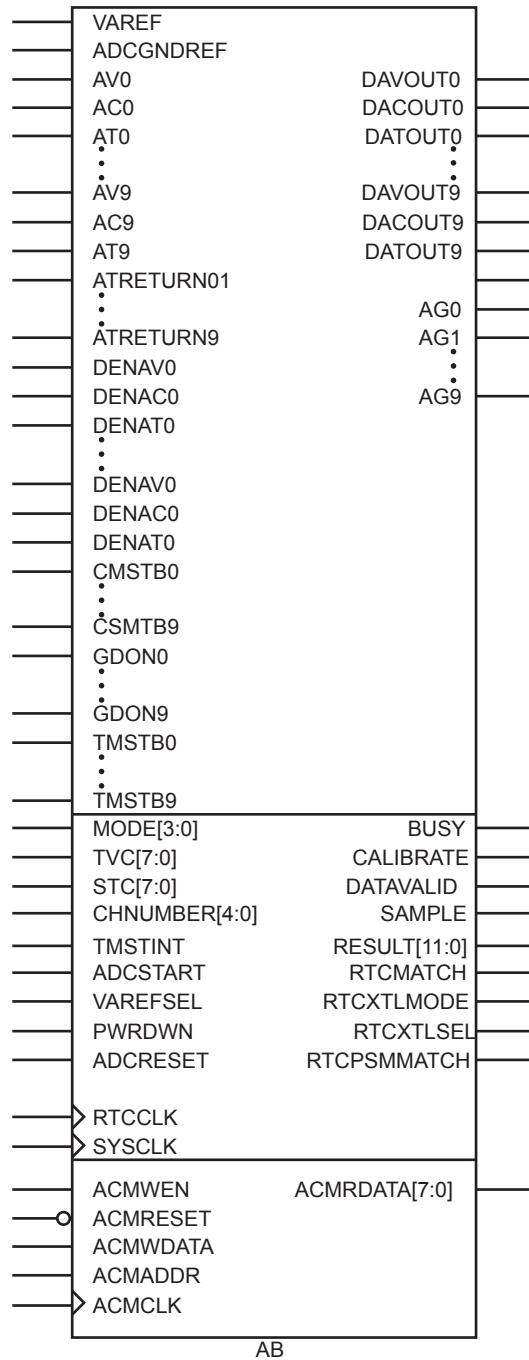


Figure 2-64 • Analog Block Macro

Temperature Monitor

The final pin in the Analog Quad is the Analog Temperature (AT) pin. The AT pin is used to implement an accurate temperature monitor in conjunction with an external diode-connected bipolar transistor (Figure 2-76). For improved temperature measurement accuracy, it is important to use the ATRTN pin for the return path of the current sourced by the AT pin. Each ATRTN pin is shared between two adjacent Analog Quads. Additionally, if not used for temperature monitoring, the AT pin can provide functionality similar to that of the AV pad. However, in this mode only positive voltages can be applied to the AT pin, and only two prescaler factors are available (16 V and 4 V ranges—refer to Table 2-57 on page 2-130).

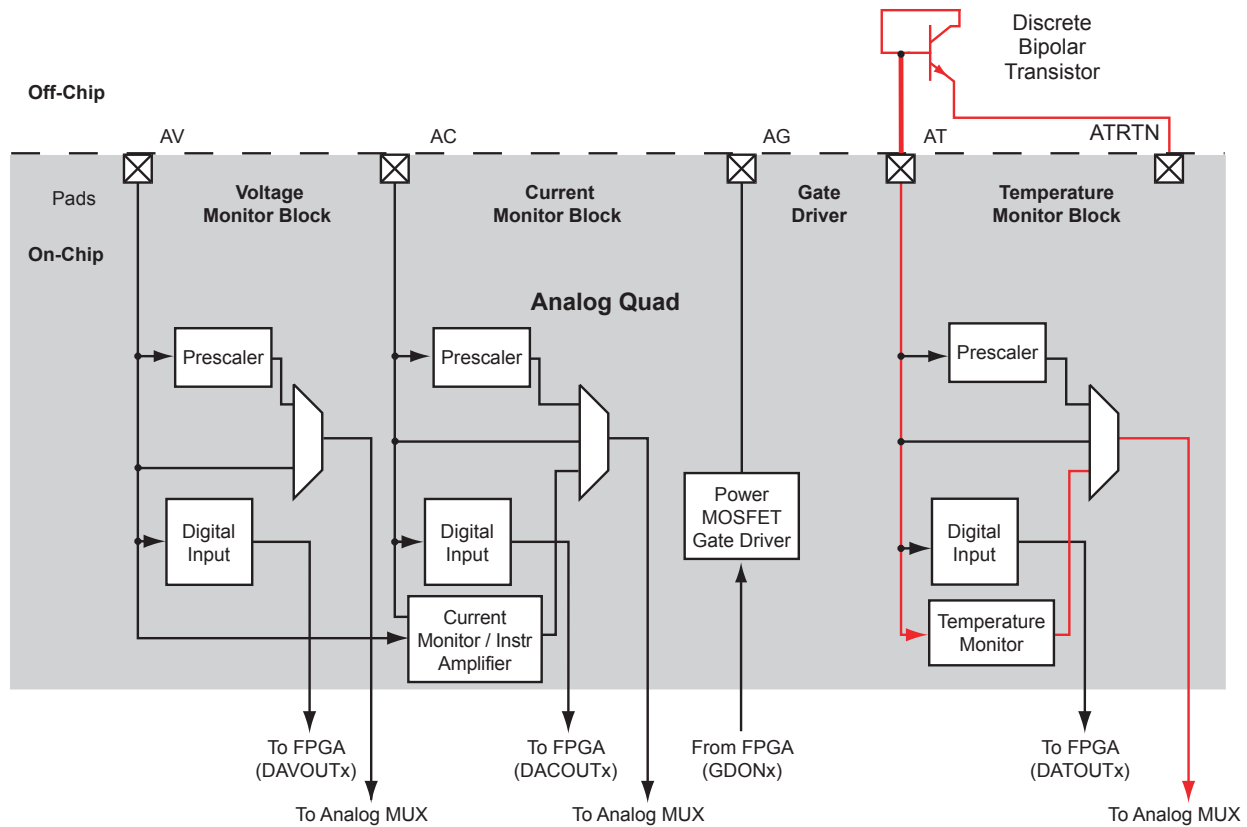


Figure 2-76 • Temperature Monitor Quad

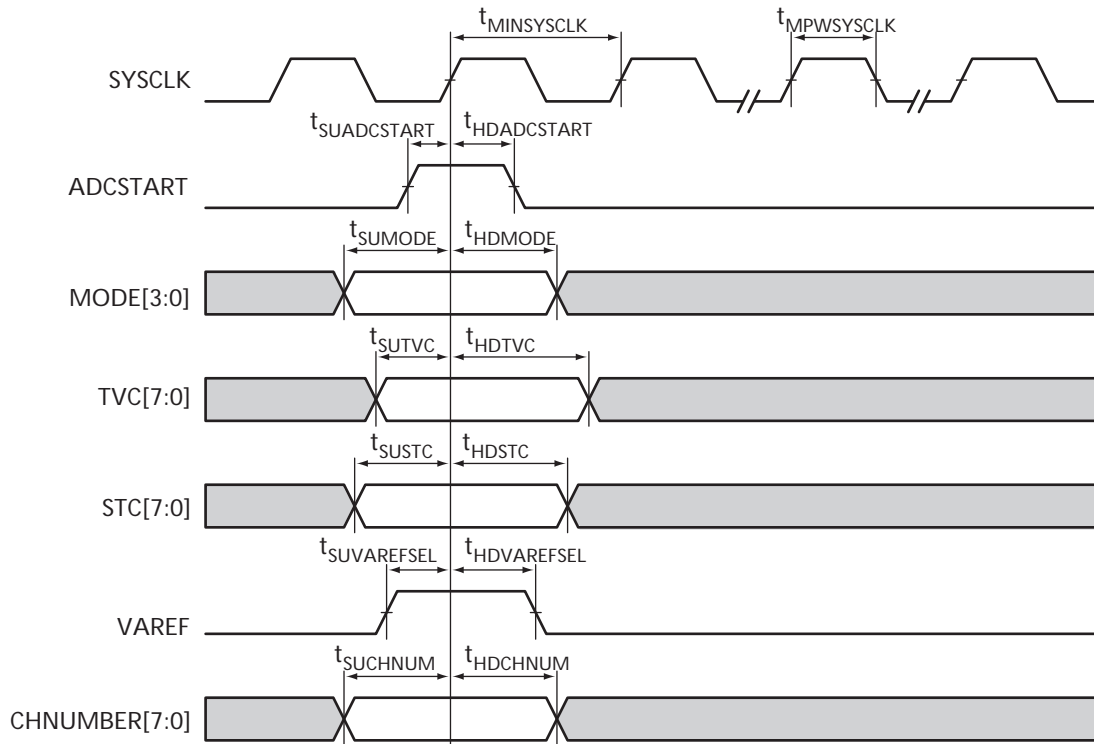
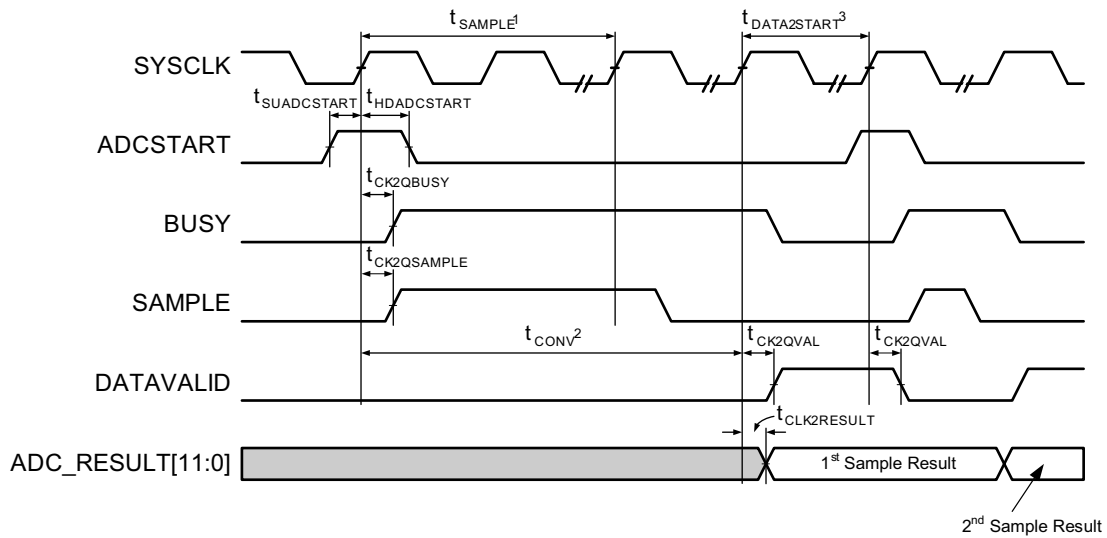


Figure 2-90 • Input Setup Time

Standard Conversion



Notes:

1. Refer to EQ 20 on page 2-109 for the calculation on the sample time, t_{SAMPLE} .
2. See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV} .
3. Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period

Figure 2-91 • Standard Conversion Status Signal Timing Diagram

ADC Interface Timing

Table 2-48 • ADC Interface Timing
 Commercial Temperature Range Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|--------------------------|--|--------|--------|--------|-------|
| t_{SUMODE} | Mode Pin Setup Time | 0.56 | 0.64 | 0.75 | ns |
| t_{HDMODE} | Mode Pin Hold Time | 0.26 | 0.29 | 0.34 | ns |
| t_{SUTVC} | Clock Divide Control (TVC) Setup Time | 0.68 | 0.77 | 0.90 | ns |
| t_{HDTVC} | Clock Divide Control (TVC) Hold Time | 0.32 | 0.36 | 0.43 | ns |
| t_{SUSTC} | Sample Time Control (STC) Setup Time | 1.58 | 1.79 | 2.11 | ns |
| t_{HDSTC} | Sample Time Control (STC) Hold Time | 1.27 | 1.45 | 1.71 | ns |
| $t_{\text{SUVAREFSEL}}$ | Voltage Reference Select (VAREFSEL) Setup Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{HDVAREFSEL}}$ | Voltage Reference Select (VAREFSEL) Hold Time | 0.67 | 0.76 | 0.89 | ns |
| t_{SUCHNUM} | Channel Select (CHNUMBER) Setup Time | 0.90 | 1.03 | 1.21 | ns |
| t_{HDCHNUM} | Channel Select (CHNUMBER) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SUADCSTART}}$ | Start of Conversion (ADCSTART) Setup Time | 0.75 | 0.85 | 1.00 | ns |
| $t_{\text{HDADCSTART}}$ | Start of Conversion (ADCSTART) Hold Time | 0.43 | 0.49 | 0.57 | ns |
| t_{CK2QBUSY} | Busy Clock-to-Q | 1.33 | 1.51 | 1.78 | ns |
| t_{CK2QCAL} | Power-Up Calibration Clock-to-Q | 0.63 | 0.71 | 0.84 | ns |
| t_{CK2QVAL} | Valid Conversion Result Clock-to-Q | 3.12 | 3.55 | 4.17 | ns |
| $t_{\text{CK2QSAMPLE}}$ | Sample Clock-to-Q | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{CK2QRESULT}}$ | Conversion Result Clock-to-Q | 2.53 | 2.89 | 3.39 | ns |
| $t_{\text{CLR2QBUSY}}$ | Busy Clear-to-Q | 2.06 | 2.35 | 2.76 | ns |
| t_{CLR2QCAL} | Power-Up Calibration Clear-to-Q | 2.15 | 2.45 | 2.88 | ns |
| t_{CLR2QVAL} | Valid Conversion Result Clear-to-Q | 2.41 | 2.74 | 3.22 | ns |
| $t_{\text{CLR2QSAMPLE}}$ | Sample Clear-to-Q | 2.17 | 2.48 | 2.91 | ns |
| $t_{\text{CLR2QRESULT}}$ | Conversion result Clear-to-Q | 2.25 | 2.56 | 3.01 | ns |
| t_{RECCLR} | Recovery Time of Clear | 0.00 | 0.00 | 0.00 | ns |
| t_{REMCLR} | Removal Time of Clear | 0.63 | 0.72 | 0.84 | ns |
| $t_{\text{MPWSYSCLK}}$ | Clock Minimum Pulse Width for the ADC | 4.00 | 4.00 | 4.00 | ns |
| $t_{\text{FMAXSYSCLK}}$ | Clock Maximum Frequency for the ADC | 100.00 | 100.00 | 100.00 | MHz |

Double Data Rate (DDR) Support

Fusion Pro I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in [Figure 2-101](#). Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on Fusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in [Figure 2-102 on page 2-140](#). New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the application note [Using DDR for Fusion Devices](#) for more information.

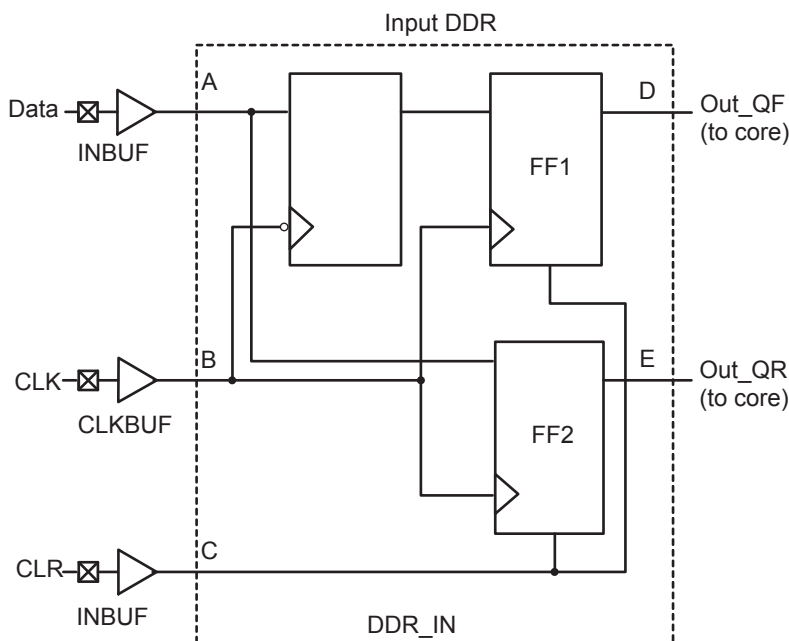


Figure 2-101 • DDR Input Register Support in Fusion Devices

5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, Fusion I/Os can directly drive signals into 5 V TTL receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceed the VIL = 0.8 V and VIH = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

Simultaneously Switching Outputs and PCB Layout

- Simultaneously switching outputs (SSOs) can produce signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and VCCI dip noise. These two noise types are caused by rapidly changing currents through GND and VCCI package pin inductances during switching activities:
- Ground bounce noise voltage = $L(\text{GND}) * di/dt$
- VCCI dip noise voltage = $L(\text{VCCI}) * di/dt$

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to be considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

Table 2-115 • 2.5 V LVCMOS High Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 8.66 | 0.04 | 1.31 | 0.43 | 7.83 | 8.66 | 2.68 | 2.30 | 10.07 | 10.90 | ns |
| | –1 | 0.56 | 7.37 | 0.04 | 1.11 | 0.36 | 6.66 | 7.37 | 2.28 | 1.96 | 8.56 | 9.27 | ns |
| | –2 | 0.49 | 6.47 | 0.03 | 0.98 | 0.32 | 5.85 | 6.47 | 2.00 | 1.72 | 7.52 | 8.14 | ns |
| 8 mA | Std. | 0.66 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | –1 | 0.56 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | –2 | 0.49 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 12 mA | Std. | 0.66 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | –1 | 0.56 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | –2 | 0.49 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 16 mA | Std. | 0.66 | 3.35 | 0.04 | 1.31 | 0.43 | 3.41 | 3.06 | 3.36 | 3.55 | 5.65 | 5.30 | ns |
| | –1 | 0.56 | 2.85 | 0.04 | 1.11 | 0.36 | 2.90 | 2.60 | 2.86 | 3.02 | 4.81 | 4.51 | ns |
| | –2 | 0.49 | 2.50 | 0.03 | 0.98 | 0.32 | 2.55 | 2.29 | 2.51 | 2.65 | 4.22 | 3.96 | ns |
| 24 mA | Std. | 0.66 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | –1 | 0.56 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | –2 | 0.49 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-116 • 2.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | –1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | –2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 4 mA | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | –1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | –2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 6 mA | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | –2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |
| 8 mA | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | –2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Voltage Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-138 • Minimum and Maximum DC Input and Output Levels

| 3.3 V GTL | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------------|--------|-------------|-------------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 20 mA ³ | −0.3 | VREF − 0.05 | VREF + 0.05 | 3.6 | 0.4 | − | 20 | 20 | 181 | 268 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

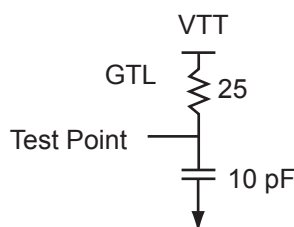


Figure 2-124 • AC Loading

Table 2-139 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF − 0.05 | VREF + 0.05 | 0.8 | 0.8 | 1.2 | 10 |

Note: *Measuring point = Vtrip. See [Table 2-90 on page 2-166](#) for a complete table of trip points.

Timing Characteristics

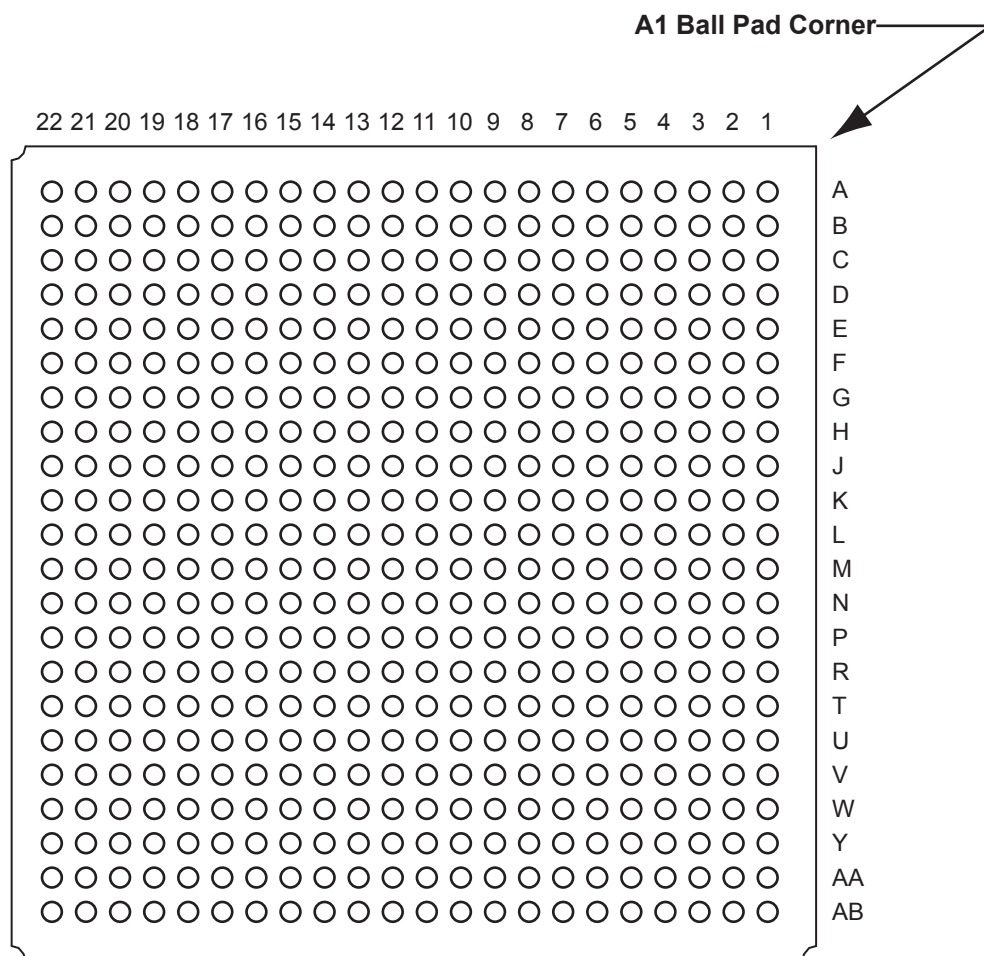
Table 2-140 • 3.3 V GTL

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 0.8 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.08 | 0.04 | 2.93 | 0.43 | 2.04 | 2.08 | | | 4.27 | 4.31 | ns |
| −1 | 0.56 | 1.77 | 0.04 | 2.50 | 0.36 | 1.73 | 1.77 | | | 3.63 | 3.67 | ns |
| −2 | 0.49 | 1.55 | 0.03 | 2.19 | 0.32 | 1.52 | 1.55 | | | 3.19 | 3.22 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/default.aspx>.

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| H13 | GND | GND |
| H14 | VCCIB1 | VCCIB1 |
| H15 | GND | GND |
| H16 | GND | GND |
| H17 | NC | IO53NDB2V0 |
| H18 | IO38PDB2V0 | IO57PDB2V0 |
| H19 | GCA2/IO39PDB2V0 | GCA2/IO59PDB2V0 |
| H20 | VCCIB2 | VCCIB2 |
| H21 | IO37NDB2V0 | IO54NDB2V0 |
| H22 | IO37PDB2V0 | IO54PDB2V0 |
| J1 | NC | IO112PPB4V0 |
| J2 | IO76NDB4V0 | IO113NDB4V0 |
| J3 | GFB2/IO74PDB4V0 | GFB2/IO109PDB4V0 |
| J4 | GFA2/IO75PDB4V0 | GFA2/IO110PDB4V0 |
| J5 | NC | IO112NPB4V0 |
| J6 | NC | IO104PDB4V0 |
| J7 | NC | IO111PDB4V0 |
| J8 | VCCIB4 | VCCIB4 |
| J9 | GND | GND |
| J10 | VCC | VCC |
| J11 | GND | GND |
| J12 | VCC | VCC |
| J13 | GND | GND |
| J14 | VCC | VCC |
| J15 | VCCIB2 | VCCIB2 |
| J16 | GCB2/IO40PDB2V0 | GCB2/IO60PDB2V0 |
| J17 | NC | IO58NDB2V0 |
| J18 | IO38NDB2V0 | IO57NDB2V0 |
| J19 | IO39NDB2V0 | IO59NDB2V0 |
| J20 | GCC2/IO41PDB2V0 | GCC2/IO61PDB2V0 |
| J21 | NC | IO55PSB2V0 |
| J22 | IO42PDB2V0 | IO56PDB2V0 |
| K1 | GFC2/IO73PDB4V0 | GFC2/IO108PDB4V0 |
| K2 | GND | GND |
| K3 | IO74NDB4V0 | IO109NDB4V0 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| K4 | IO75NDB4V0 | IO110NDB4V0 |
| K5 | GND | GND |
| K6 | NC | IO104NDB4V0 |
| K7 | NC | IO111NDB4V0 |
| K8 | GND | GND |
| K9 | VCC | VCC |
| K10 | GND | GND |
| K11 | VCC | VCC |
| K12 | GND | GND |
| K13 | VCC | VCC |
| K14 | GND | GND |
| K15 | GND | GND |
| K16 | IO40NDB2V0 | IO60NDB2V0 |
| K17 | NC | IO58PDB2V0 |
| K18 | GND | GND |
| K19 | NC | IO68NPB2V0 |
| K20 | IO41NDB2V0 | IO61NDB2V0 |
| K21 | GND | GND |
| K22 | IO42NDB2V0 | IO56NDB2V0 |
| L1 | IO73NDB4V0 | IO108NDB4V0 |
| L2 | VCCOSC | VCCOSC |
| L3 | VCCIB4 | VCCIB4 |
| L4 | XTAL2 | XTAL2 |
| L5 | GFC1/IO72PDB4V0 | GFC1/IO107PDB4V0 |
| L6 | VCCIB4 | VCCIB4 |
| L7 | GFB1/IO71PDB4V0 | GFB1/IO106PDB4V0 |
| L8 | VCCIB4 | VCCIB4 |
| L9 | GND | GND |
| L10 | VCC | VCC |
| L11 | GND | GND |
| L12 | VCC | VCC |
| L13 | GND | GND |
| L14 | VCC | VCC |
| L15 | VCCIB2 | VCCIB2 |
| L16 | IO48PDB2V0 | IO70PDB2V0 |

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

| Revision | Changes | Page |
|------------------------------|---|-----------------|
| Revision 6 (March 2014) | Note added for the discontinuance of QN108 and QN180 packages to the "Package I/Os: Single-/Double-Ended (Analog)" table and the "Temperature Grade Offerings" table (SAR 55113, PDN 1306). | II and IV |
| | Updated details about page programming time in the "Program Operation" section (SAR 49291). | 2-46 |
| | ADC_START changed to ADCSTART in the "ADC Operation" section (SAR 44104). | 2-104 |
| Revision 5 (January 2014) | Calibrated offset values (AFS090, AFS250) of the external temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 51464). | 2-117 |
| | Specifications for the internal temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 50870). | 2-117 |
| Revision 4 (January 2013) | The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43177). | III |
| | The note in Table 2-12 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42563). | 2-28 |
| | Table 2-49 • Analog Channel Specifications was modified to update the uncalibrated offset values (AFS250) of the external and internal temperature monitors (SAR 43134). | 2-117 |
| | In Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3), changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 20812). | 2-130 |
| | The values for the Speed Grade (-1 and Std.) for FDDRIMAX (Table 2-180 • Input DDR Propagation Delays) and values for the Speed Grade (-2 and Std.) for FDDOMAX (Table 2-182 • Output DDR Propagation Delays) had been inadvertently interchanged. This has been rectified (SAR 38514). | 2-220, 2-222 |
| | Added description about what happens if a user connects VAREF to an external 3.3 V on their board to the "VAREF Analog Reference Voltage" section (SAR 35188). | 2-225 |
| | Added a note to Table 3-2 • Recommended Operating Conditions ¹ (SAR 43429): The programming temperature range supported is T _{ambient} = 0°C to 85°C. | 3-3 |
| | Added the Package Thermal details for AFS600-PQ208 and AFS250-PQ208 to Table 3-6 • Package Thermal Resistance (SAR 37816). Deleted the Die Size column from the table (SAR 43503). | 3-7 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 42495). Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 3 (August 2012) | Microblade U1AFS250 and U1AFS1500 devices were added to the product tables. | I – IV |
| | A sentence pertaining to the analog I/Os was added to the "Specifying I/O States During Programming" section (SAR 34831). | 1-9 |

| Revision | Changes | Page |
|---------------------------|--|------------------------------|
| Revision 2 (continued) | A note was added to Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro) stating that the user is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off (SAR 21773). | 2-31 |
| | VPUMP was incorrectly represented as VPP in several places. This was corrected to VPUMP in the "Standby and Sleep Mode Circuit Implementation" section and Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics (21963). | 2-32, 3-10 |
| | Additional information was added to the Flash Memory Block "Write Operation" section, including an explanation of the fact that a copy-page operation takes no less than 55 cycles (SAR 26338). | 2-45 |
| | The "FlashROM" section was revised to refer to Figure 2-46 • FlashROM Timing Diagram and Table 2-26 • FlashROM Access Time rather than stating 20 MHz as the maximum FlashROM access clock and 10 ns as the time interval for D0 to become valid or invalid (SAR 22105). | 2-53, 2-54 |
| | The following figures were deleted (SAR 29991). Reference was made to a new application note, Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs , which covers these cases in detail (SAR 34862). Figure 2-55 • Write Access after Write onto Same Address Figure 2-56 • Read Access after Write onto Same Address Figure 2-57 • Write Access after Read onto Same Address | 2-63, 2-66, 2-65, 2-75 |
| | The port names in the SRAM "Timing Waveforms" , "Timing Characteristics" , SRAM tables, Figure 2-55 • RAM Reset . Applicable to both RAM4K9 and RAM512x18., and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35753). | |
| | In several places throughout the datasheet, GNDREF was corrected to ADCGNDREF (SAR 20783): Figure 2-64 • Analog Block Macro Table 2-36 • Analog Block Pin Description "ADC Operation" section | 2-77 2-78 2-104 |
| | The following note was added below Figure 2-78 • Timing Diagram for the Temperature Monitor Strobe Signal : When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 μ A sink into the Fusion device. (SAR 24796). | 2-93 |
| | The "Analog-to-Digital Converter Block" section was extensively revised, reorganizing the information and adding the "ADC Theory of Operation" section and "Acquisition Time or Sample Time Control" section. The "ADC Example" section was reworked and corrected (SAR 20577). | 2-96 |
| | Table 2-49 • Analog Channel Specifications was modified to include calibrated and uncalibrated values for offset (AFS090 and AFS250) for the external and internal temperature monitors. The "Offset" section was revised accordingly and now references Table 2-49 • Analog Channel Specifications (SARs 22647, 27015). | 2-95, 2-117 |
| | The "Intra-Conversion" section and "Injected Conversion" section had definitions incorrectly interchanged and have been corrected. Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram were also incorrectly interchanged and have been replaced correctly. Reference in the figure notes to EQ 10 has been corrected to EQ 23 (SAR 20547). | 2-110, 2-113, 2-113 |

| Revision | Changes | Page |
|--------------------------------|---|------------|
| Advance v1.0 (continued) | This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to V_{CC33A} . | 3-8 |
| Advance v0.9 (October 2007) | In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126 | II |
| | In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pin: B25 | 3-2 |
| | In the "180-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: B29 AFS250: B29 | 3-4 |
| | In the "208-Pin PQFP" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: 102 AFS250: 102 | 3-8 |
| | In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14 | 3-12 |
| Advance v0.9 (continued) | In the "484-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS600: AB18 AFS1500: AB18 | 3-20 |
| | In the "676-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS1500: AD20 | 3-28 |
| Advance v0.8 (June 2007) | Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC. | 2-20, 2-21 |
| | Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added. | 2-25 |
| | The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator. | 2-22 |
| | Table 2-11 • Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of $I_{DYNXTAL}$ for 0.032–0.2 MHz to 0.19. | 2-24 |
| | The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR. | 2-41 |
| | The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR. | 2-41 |

| Revision | Changes | Page |
|-----------------------------|--|-------|
| Advance v0.6 (continued) | The "Analog-to-Digital Converter Block" section was updated with the following statement: "All results are MSB justified in the ADC." | 2-99 |
| | The information about the ADCSTART signal was updated in the "ADC Description" section. | 2-102 |
| | Table 2-46 · Analog Channel Specifications was updated. | 2-118 |
| | Table 2-47 · ADC Characteristics in Direct Input Mode was updated. | 2-121 |
| | Table 2-51 · ACM Address Decode Table for Analog Quad was updated. | 2-127 |
| | In Table 2-53 · Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated. | 2-130 |
| | The "Introduction" section was updated to include information about digital inputs, outputs, and buffers. | 2-133 |
| | In Table 2-69 · Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features: Single-ended receiver Voltage-referenced differential receiver LVDS/LVPECL differential receiver features | 2-137 |
| | The "User I/O Naming Convention" section was updated to include "V" and "Z" descriptions | 2-159 |
| | The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw. | 2-224 |
| | The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw. | 2-224 |
| | The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and VCCI pins within a given I/O bank. | 2-185 |
| | The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The "PTM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090. | 3-8 |