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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-1fgg484

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.

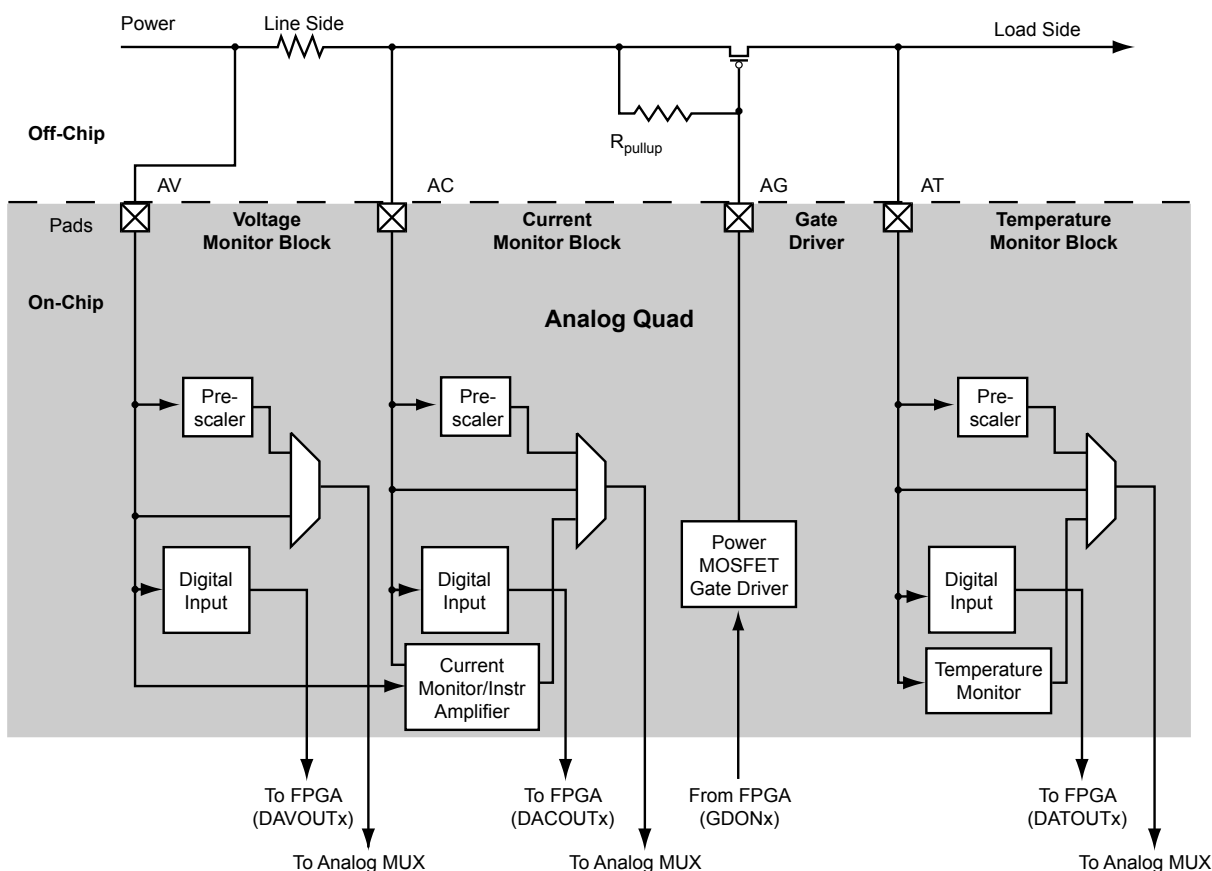


Figure 1-1 • Analog Quad

The FlashPoint tool in the Fusion development software solutions, Libero SoC and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

Clock Resources

PLLs and Clock Conditioning Circuits (CCCs)

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. In the two larger family members, two of these CCCs also include a PLL; the smaller devices support one PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
 - 100 MHz on-chip RC oscillator
 - Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
 - 70 ps at 350 MHz
 - 90 ps at 100 MHz
 - 180 ps at 24 MHz
 - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 μs
- Low power consumption of 5 mW

Crystal Oscillator

The Crystal Oscillator (XTLOSC) is source that generates the clock from an external crystal. The output of XTLOSC CLKOUT signal can be selected as an input to the PLL. Refer to the ["Clock Conditioning Circuits" section](#) for more details. The XTLOSC can operate in normal operations and Standby mode (RTC is running and 1.5 V is not present).

In normal operation, the internal FPGA_EN signal is '1' as long as 1.5 V is present for VCC. As such, the internal enable signal, XTL_EN, for Crystal Oscillator is enabled since FPGA_EN is asserted. The XTL_MODE has the option of using MODE or RTC_MODE, depending on SELMODE.

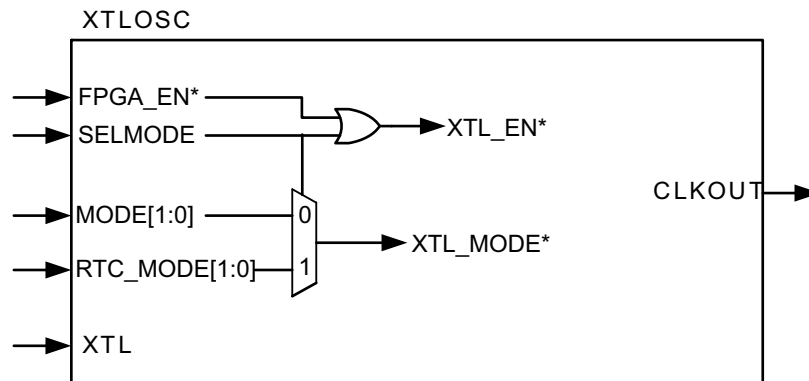
During Standby, 1.5 V is not available, as such, and FPGA_EN is '0'. SELMODE must be asserted in order for XTL_EN to be enabled; hence XTL_MODE relies on RTC_MODE. SELMODE and RTC_MODE must be connected to RTCXTLSEL and RTCXTLMODE from the AB respectively for correct operation during Standby (refer to the ["Real-Time Counter System" section on page 2-31](#) for a detailed description).

The Crystal Oscillator can be configured in one of four modes:

- RC network, 32 KHz to 4 MHz
- Low gain, 32 to 200 KHz
- Medium gain, 0.20 to 2.0 MHz
- High gain, 2.0 to 20.0 MHz

In RC network mode, the XTAL1 pin is connected to an RC circuit, as shown in [Figure 2-16 on page 2-18](#). The XTAL2 pin should be left floating. The RC value can be chosen based on [Figure 2-18](#) for any desired frequency between 32 KHz and 4 MHz. The RC network mode can also accommodate an external clock source on XTAL1 instead of an RC circuit.

In Low gain, Medium gain, and High gain, an external crystal component or ceramic resonator can be added onto XTAL1 and XTAL2, as shown in [Figure 2-16 on page 2-18](#). In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.



Note: *Internal signal—does not exist in macro.

Figure 2-17 • XTLOSC Macro

Table 2-19 • Flash Memory Block Pin Names (continued)

Interface Name	Width	Direction	Description
STATUS[1:0]	2	Out	Status of the last operation completed: 00: Successful completion 01: Read-/Unprotect-Page: single error detected and corrected Write: operation addressed a write-protected page Erase-Page: protection violation Program: Page Buffer is unmodified Protection violation 10: Read-/Unprotect-Page: two or more errors detected 11: Write: attempt to write to another page before programming current page Erase-Page/Program: page write count has exceeded the 10-year retention threshold
UNPROTECTPAGE	1	In	When asserted, the page addressed is copied into the Page Buffer and the Page Buffer is made writable.
WD[31:0]	32	In	Write data
WEN	1	In	When asserted, stores WD in the page buffer.

All flash memory block input signals are active high, except for RESET.

Flash Memory Block Diagram

A simplified diagram of the flash memory block is shown in Figure 2-33.

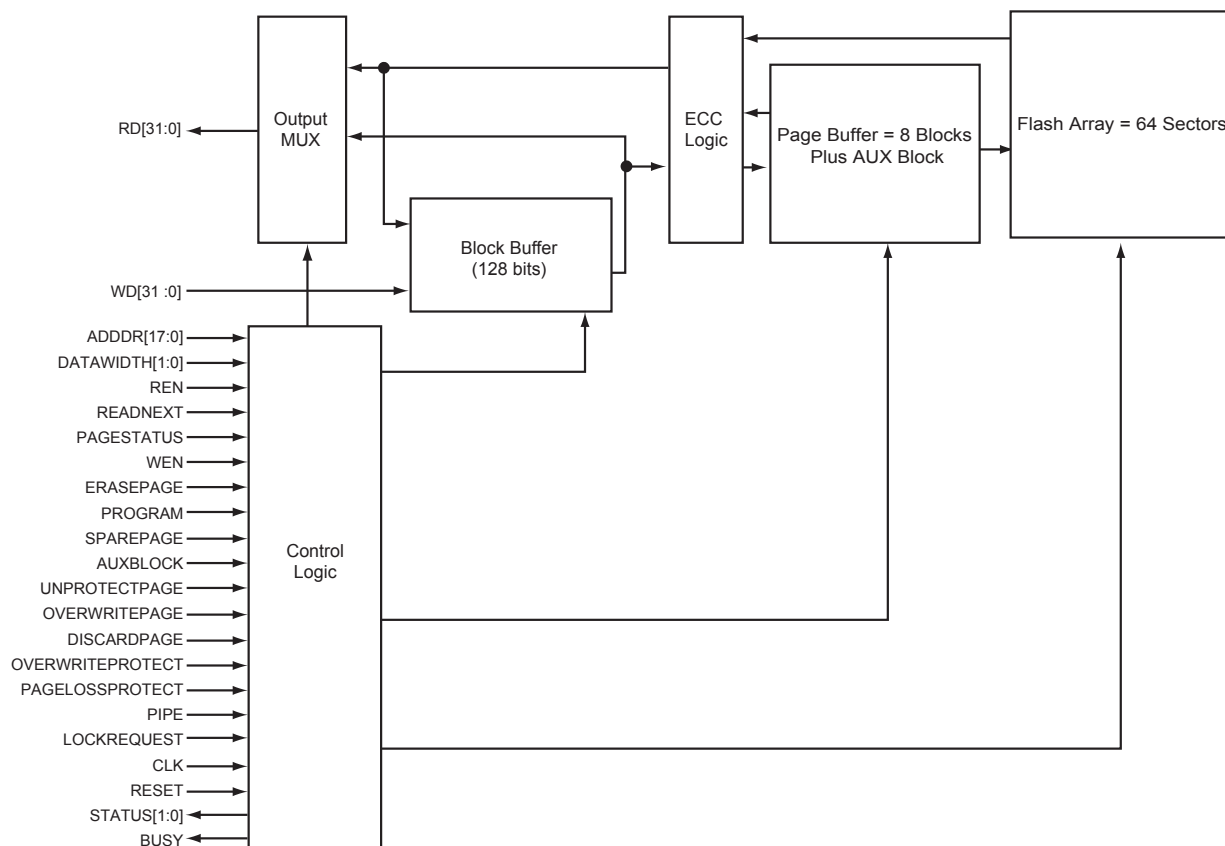


Figure 2-33 • Flash Memory Block Diagram

The logic consists of the following sub-blocks:

- **Flash Array**
Contains all stored data. The flash array contains 64 sectors, and each sector contains 33 pages of data.
- **Page Buffer**
A page-wide volatile register. A page contains 8 blocks of data and an AUX block.
- **Block Buffer**
Contains the contents of the last block accessed. A block contains 128 data bits.
- **ECC Logic**

The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in [Figure 2-40](#) and [Figure 2-41](#).

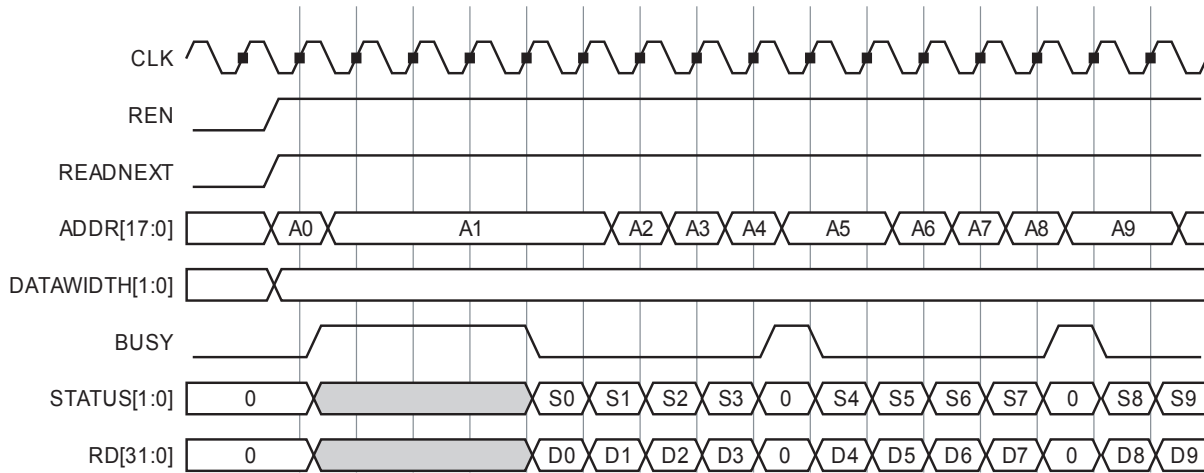


Figure 2-40 • Read Next Waveform (Non-Pipe Mode, 32-bit access)

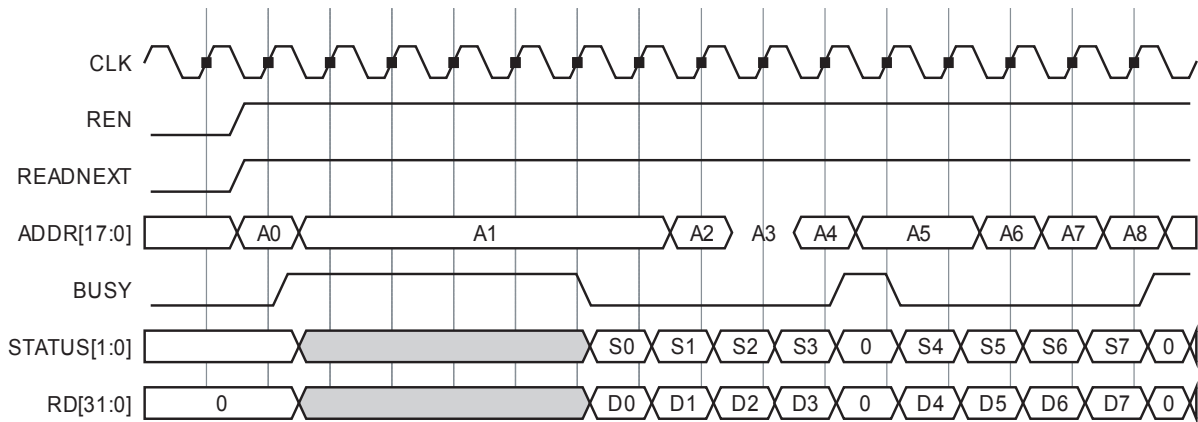


Figure 2-41 • Read Next WaveForm (Pipe Mode, 32-bit access)

Flash Memory Block Characteristics

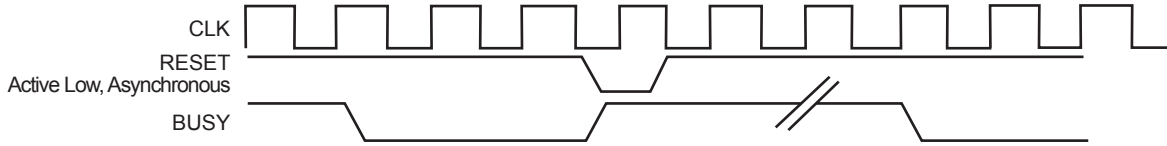


Figure 2-44 • Reset Timing Diagram

Table 2-25 • Flash Memory Block Timing
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{CLK2RD}	Clock-to-Q in 5-cycle read mode of the Read Data	7.99	9.10	10.70	ns
	Clock-to-Q in 6-cycle read mode of the Read Data	5.03	5.73	6.74	ns
t_{CLK2BUSY}	Clock-to-Q in 5-cycle read mode of BUSY	4.95	5.63	6.62	ns
	Clock-to-Q in 6-cycle read mode of BUSY	4.45	5.07	5.96	ns
$t_{\text{CLK2STATUS}}$	Clock-to-Status in 5-cycle read mode	11.24	12.81	15.06	ns
	Clock-to-Status in 6-cycle read mode	4.48	5.10	6.00	ns
t_{DSUNVM}	Data Input Setup time for the Control Logic	1.92	2.19	2.57	ns
t_{DHNVM}	Data Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{ASUNVM}	Address Input Setup time for the Control Logic	2.76	3.14	3.69	ns
t_{AHNVM}	Address Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{SUDWNVM}	Data Width Setup time for the Control Logic	1.85	2.11	2.48	ns
t_{HDDWNVM}	Data Width Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{SURENNVM}	Read Enable Setup time for the Control Logic	3.85	4.39	5.16	ns
t_{HDRENNVM}	Read Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
t_{SUWENNVN}	Write Enable Setup time for the Control Logic	2.37	2.69	3.17	ns
t_{HDWENNVN}	Write Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUPROGNVM}}$	Program Setup time for the Control Logic	2.16	2.46	2.89	ns
$t_{\text{HDPROGNVM}}$	Program Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUSPAREPAGE}}$	SparePage Setup time for the Control Logic	3.74	4.26	5.01	ns
$t_{\text{HDSAREPAGE}}$	SparePage Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{SUAUXBLK}	Auxiliary Block Setup Time for the Control Logic	3.74	4.26	5.00	ns
t_{HDAUXBLK}	Auxiliary Block Hold Time for the Control Logic	0.00	0.00	0.00	ns
t_{SURDNEXT}	ReadNext Setup Time for the Control Logic	2.17	2.47	2.90	ns
t_{HDRDNEXT}	ReadNext Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUERASEPG}}$	Erase Page Setup Time for the Control Logic	3.76	4.28	5.03	ns
$t_{\text{HDERASEPG}}$	Erase Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUUNPROTECTPG}}$	Unprotect Page Setup Time for the Control Logic	2.01	2.29	2.69	ns
$t_{\text{HDUNPROTECTPG}}$	Unprotect Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUDISCARDPG}}$	Discard Page Setup Time for the Control Logic	1.88	2.14	2.52	ns
$t_{\text{HDDISCARDPG}}$	Discard Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{\text{SUOVERWRPRO}}$	Overwrite Protect Setup Time for the Control Logic	1.64	1.86	2.19	ns
$t_{\text{HDOVERWRPRO}}$	Overwrite Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage-monitoring capabilities unique in the FPGA industry. The Analog Quad comprises three analog input pads— Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-66), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.

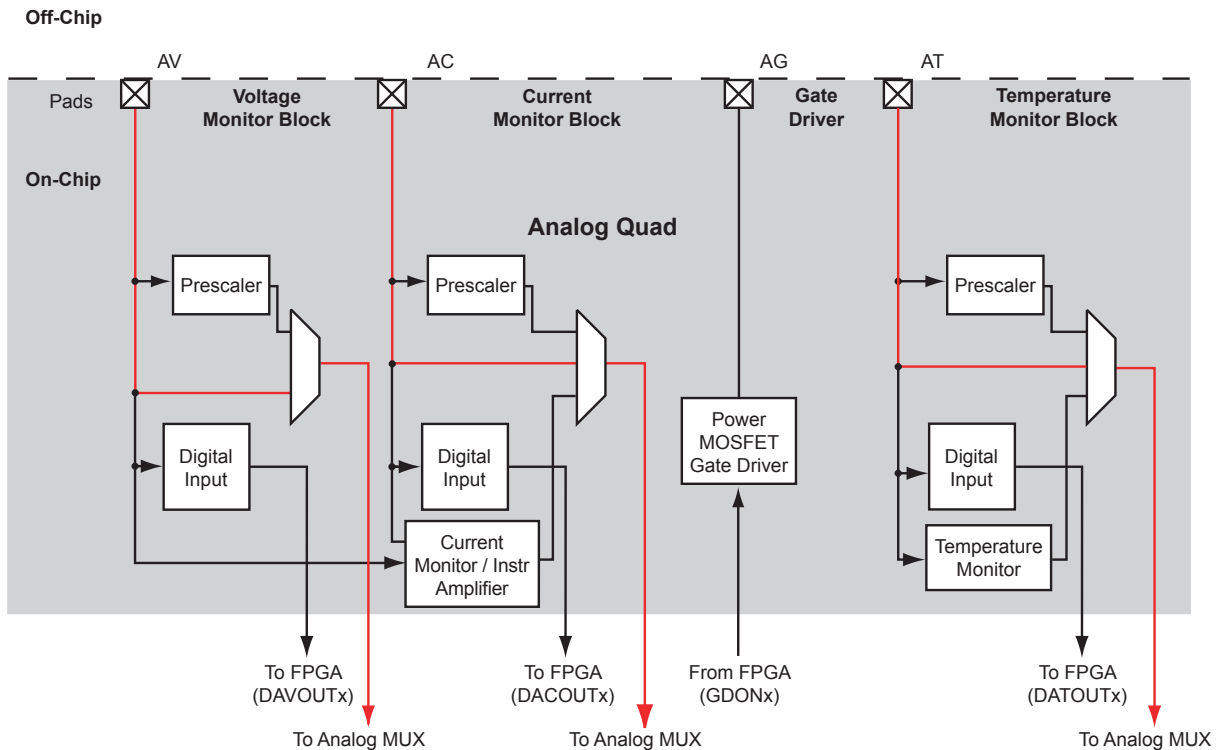


Figure 2-66 • Analog Quad Direct Connect

The Analog Quad offers a wide variety of prescaling options to enable the ADC to resolve the input signals. Figure 2-67 shows the path through the Analog Quad for a signal that is to be prescaled prior to conversion. The ADC internal reference voltage and the prescaler factors were selected to make both prescaling and postscaling of the signals easy binary calculations (refer to Table 2-57 on page 2-130 for details). When an analog input pad is configured with a prescaler, there will be a 1 M Ω resistor to ground. This occurs even when the device is in power-down mode. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, analog inputs are pulled down to ground through a 1 M Ω resistor. The gate driver output is floating (or tristated), and there is no extra current on VCC33A.

These scaling factors hold true whether the particular pad is configured to accept a positive or negative voltage. Note that whereas the AV and AC pads support the same prescaling factors, the AT pad supports a reduced set of prescaling factors and supports positive voltages only.

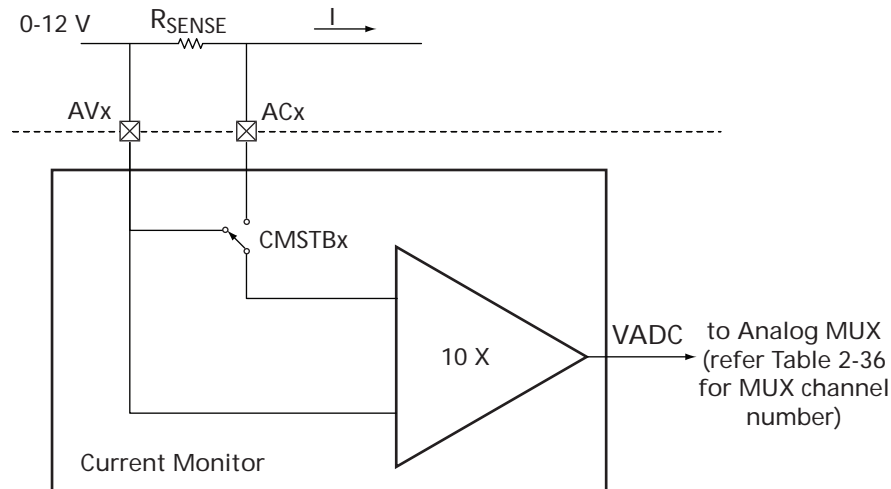


Figure 2-72 • Positive Current Monitor

Care must be taken when choosing the right resistor for current measurement application. Note that because of the 10× amplification, the maximum measurable difference between the AV and AC pads is $V_{AREF} / 10$. A larger AV-to-AC voltage drop will result in ADC saturation; that is, the digital code put out by the ADC will stay fixed at the full scale value. Therefore, the user must select the external sense resistor appropriately. Table 2-38 shows recommended resistor values for different current measurement ranges. When choosing resistor values for a system, there is a trade-off between measurement accuracy and power consumption. Choosing a large resistor will increase the voltage drop and hence increase accuracy of the measurement; however the larger voltage drop dissipates more power ($P = I^2 \times R$).

The Current Monitor is a unipolar system, meaning that the differential voltage swing must be from 0 V to $V_{AREF}/10$. Therefore, the Current Monitor only supports differential voltage where $|V_{AV} - V_{AC}|$ is greater than 0 V. This results in the requirement that the potential of the AV pad must be larger than the potential of the AC pad. This is straightforward for positive voltage systems. For a negative voltage system, it means that the AV pad must be "more negative" than the AC pad. This is shown in Figure 2-73.

In this case, both the AV pad and the AC pad are configured for negative operations and the output of the differential amplifier still falls between 0 V and V_{AREF} as required.

Table 2-37 • Recommended Resistor for Different Current Range Measurement

Current Range	Recommended Minimum Resistor Value (Ohms)
> 5 mA – 10 mA	10 – 20
> 10 mA – 20 mA	5 – 10
> 20 mA – 50 mA	2.5 – 5
> 50 mA – 100 mA	1 – 2
> 100 mA – 200 mA	0.5 – 1
> 200 mA – 500 mA	0.3 – 0.5
> 500 mA – 1 A	0.1 – 0.2
> 1 A – 2 A	0.05 – 0.1
> 2 A – 4 A	0.025 – 0.05
> 4 A – 8 A	0.0125 – 0.025
> 8 A – 12 A	0.00625 – 0.02

There are several popular ADC architectures, each with advantages and limitations. The analog-to-digital converter in Fusion devices is a switched-capacitor Successive Approximation Register (SAR) ADC. It supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (ksps). Built-in bandgap circuitry offers 1% internal voltage reference accuracy or an external reference voltage can be used.

As shown in [Figure 2-81](#), a SAR ADC contains N capacitors with binary-weighted values.

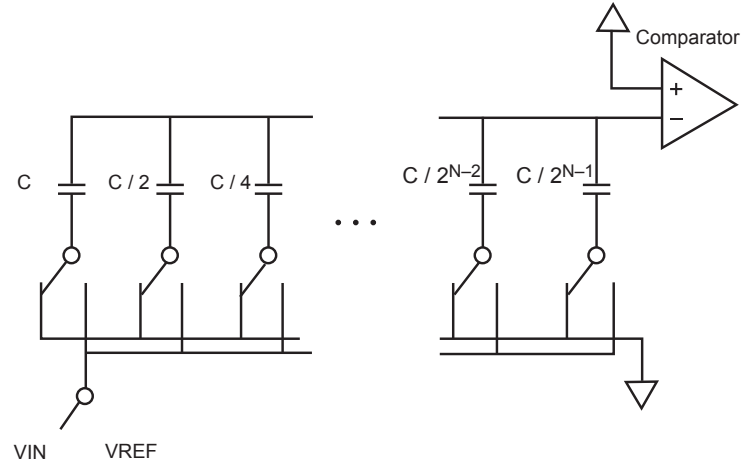


Figure 2-81 • Example SAR ADC Architecture

To begin a conversion, all of the capacitors are quickly discharged. Then VIN is applied to all the capacitors for a period of time (acquisition time) during which the capacitors are charged to a value very close to VIN. Then all of the capacitors are switched to ground, and thus $-VIN$ is applied across the comparator. Now the conversion process begins. First, C is switched to VREF. Because of the binary weighting of the capacitors, the voltage at the input of the comparator is then shown by [EQ 11](#).

$$\text{Voltage at input of comparator} = -VIN + VREF / 2$$

EQ 11

If VIN is greater than $VREF / 2$, the output of the comparator is 1; otherwise, the comparator output is 0. A register is clocked to retain this value as the MSB of the result. Next, if the MSB is 0, C is switched back to ground; otherwise, it remains connected to VREF, and C / 2 is connected to VREF. The result at the comparator input is now either $-VIN + VREF / 4$ or $-VIN + 3 VREF / 4$ (depending on the state of the MSB), and the comparator output now indicates the value of the next most significant bit. This bit is likewise registered, and the process continues for each subsequent bit until a conversion is completed. The conversion process requires some acquisition time plus N + 1 ADC clock cycles to complete.

INL – Integral Non-Linearity

INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the end points of the transfer function (Figure 2-85).

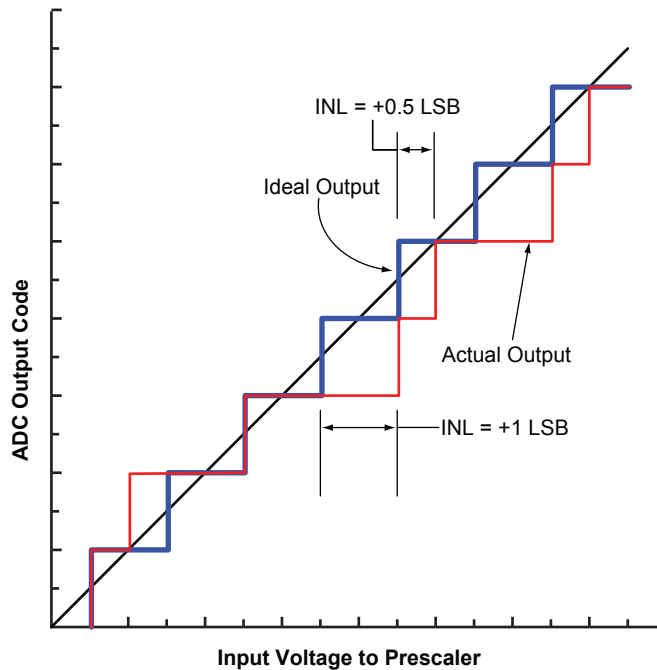


Figure 2-85 • Integral Non-Linearity (INL)

LSB – Least Significant Bit

In a binary number, the LSB is the least weighted bit in the group. Typically, the LSB is the furthest right bit. For an ADC, the weight of an LSB equals the full-scale voltage range of the converter divided by 2^N , where N is the converter's resolution.

EQ 13 shows the calculation for a 10-bit ADC with a unipolar full-scale voltage of 2.56 V:

$$1 \text{ LSB} = (2.56 \text{ V} / 2^{10}) = 2.5 \text{ mV}$$

EQ 13

No Missing Codes

An ADC has no missing codes if it produces all possible digital codes in response to a ramp signal applied to the analog input.

Table 2-50 • ADC Characteristics in Direct Input Mode
Commercial Temperature Range Conditions, $T_J = 85^{\circ}\text{C}$ (unless noted otherwise),
Typical: $V_{CC33A} = 3.3\text{ V}$, $V_{CC} = 1.5\text{ V}$

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Direct Input using Analog Pad AV, AC, AT						
VINADC	Input Voltage (Direct Input)	Refer to Table 3-2 on page 3-3				
CINADC	Input Capacitance	Channel not selected		7		pF
		Channel selected but not sampling		8		pF
		Channel selected and sampling		18		pF
ZINADC	Input Impedance	8-bit mode		2		kΩ
		10-bit mode		2		kΩ
		12-bit mode		2		kΩ
Analog Reference Voltage VAREF						
VAREF	Accuracy	T _J = 25°C	2.537	2.56	2.583	V
	Temperature Drift of Internal Reference			65		ppm / °C
	External Reference		2.527		VCC33A + 0.05	V
ADC Accuracy (using external reference) ^{1,2}						
DC Accuracy						
TUE	Total Unadjusted Error	8-bit mode	0.29			LSB
		10-bit mode	0.72			LSB
		12-bit mode	1.8			LSB
INL	Integral Non-Linearity	8-bit mode		0.20	0.25	LSB
		10-bit mode		0.32	0.43	LSB
		12-bit mode		1.71	1.80	LSB
DNL	Differential Non-Linearity (no missing code)	8-bit mode		0.20	0.24	LSB
		10-bit mode		0.60	0.65	LSB
		12-bit mode		2.40	2.48	LSB
	Offset Error	8-bit mode		0.01	0.17	LSB
		10-bit mode		0.05	0.20	LSB
		12-bit mode		0.20	0.40	LSB
	Gain Error	8-bit mode		0.0004	0.003	LSB
		10-bit mode		0.002	0.011	LSB
		12-bit mode		0.007	0.044	LSB
	Gain Error (with internal reference)	All modes		2		% FSR

Notes:

1. Accuracy of the external reference is $2.56\text{ V} \pm 4.6\text{ mV}$.
2. Data is based on characterization.
3. The sample rate is time-shared among active analog inputs.

Analog Quad ACM Description

Table 2-56 maps out the ACM space associated with configuration of the Analog Quads within the Analog Block. Table 2-56 shows the byte assignment within each quad and the function of each bit within each byte. Subsequent tables will explain each bit setting and how it corresponds to a particular configuration. After 3.3 V and 1.5 V are applied to Fusion, Analog Quad configuration registers are loaded with default settings until the initialization and configuration state machine changes them to user-defined settings.

Table 2-56 • Analog Quad ACM Byte Assignment

Byte	Bit	Signal (Bx)	Function	Default Setting
Byte 0 (AV)	0	B0[0]	Scaling factor control – prescaler	Highest voltage range
	1	B0[1]		
	2	B0[2]		
	3	B0[3]	Analog MUX select	Prescaler
	4	B0[4]	Current monitor switch	Off
	5	B0[5]	Direct analog input switch	Off
	6	B0[6]	Selects V-pad polarity	Positive
	7	B0[7]	Prescaler op amp mode	Power-down
Byte 1 (AC)	0	B1[0]	Scaling factor control – prescaler	Highest voltage range
	1	B1[1]		
	2	B1[2]		
	3	B1[3]	Analog MUX select	Prescaler
	4	B1[4]		
	5	B1[5]	Direct analog input switch	Off
	6	B1[6]	Selects C-pad polarity	Positive
	7	B1[7]	Prescaler op amp mode	Power-down
Byte 2 (AG)	0	B2[0]	Internal chip temperature monitor *	Off
	1	B2[1]	Spare	–
	2	B2[2]	Current drive control	Lowest current
	3	B2[3]		
	4	B2[4]	Spare	–
	5	B2[5]	Spare	–
	6	B2[6]	Selects G-pad polarity	Positive
	7	B2[7]	Selects low/high drive	Low drive
Byte 3 (AT)	0	B3[0]	Scaling factor control – prescaler	Highest voltage range
	1	B3[1]		
	2	B3[2]		
	3	B3[3]	Analog MUX select	Prescaler
	4	B3[4]		
	5	B3[5]	Direct analog input switch	Off
	6	B3[6]	–	–
	7	B3[7]	Prescaler op amp mode	Power-down

Note: *For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

Electrostatic Discharge (ESD) Protection

Fusion devices are tested per JEDEC Standard JESD22-A114-B.

Fusion devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to VCCI. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the Off state, except when transient voltage is significantly above VCCI or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to [Table 2-75](#) and [Table 2-76 on page 2-143](#) for more information about I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 2-75 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities

I/O Assignment	Clamp Diode		Hot Insertion		5 V Input Tolerance ¹		Input Buffer	Output Buffer
	Standard I/O	Advanced I/O	Standard I/O	Advanced I/O	Standard I/O	Advanced I/O		
3.3 V LVTTTL/LVCMOS	No	Yes	Yes	No	Yes ¹	Yes ¹	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	N/A	Yes	N/A	No	N/A	Yes ¹	Enabled/Disabled	
LVCMOS 2.5 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V	N/A	Yes	N/A	No	N/A	Yes ²	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
Differential, LVDS/BLVDS/M-LVDS/ LVPECL ³	N/A	Yes	N/A	No	N/A	No	Enabled/Disabled	

Notes:

1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.
2. Can be implemented with an external resistor and an internal clamp diode.
3. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.

Table 2-76 • Fusion Pro I/O – Hot-Swap and 5 V Input Tolerance Capabilities

I/O Assignment	Clamp Diode	Hot Insertion	5 V Input Tolerance	Input Buffer	Output Buffer
3.3 V LVTTTL/LVCMOS	No	Yes	Yes ¹	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes ¹	Enabled/Disabled	
LVCMOS 2.5 V ³	No	Yes	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V ³	Yes	No	Yes ²	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/BLVDS/M-LVDS/LVPECL ⁴	No	Yes	No	Enabled/Disabled	

Notes:

1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.
2. Can be implemented with an external resistor and an internal clamp diode.
3. In the [SmartGen](#), [FlashROM](#), [Flash Memory System Builder](#), and [Analog System Builder User Guide](#), select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V I/O standard.
4. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.

Output Enable Register

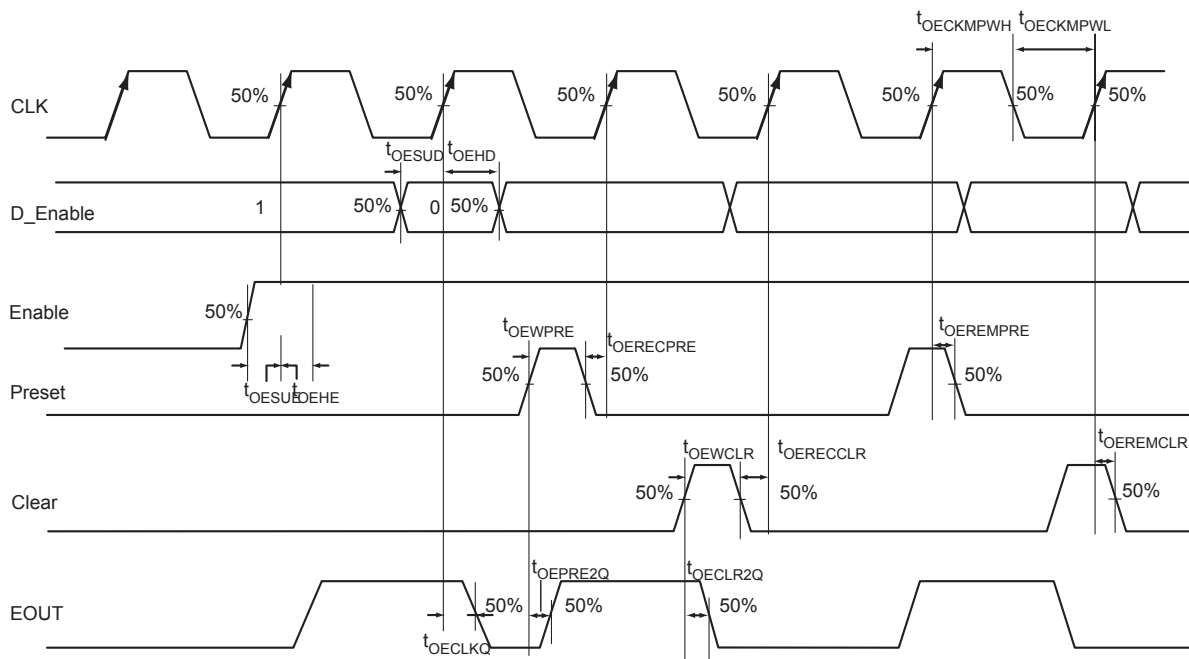


Figure 2-141 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-178 • Output Enable Register Propagation Delays

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.44	0.51	0.59	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{ja(\text{total})} = \frac{T_J - T_A}{P} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{3.00\text{ W}} = 10.00^\circ\text{C/W}$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(\text{TOTAL})} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

$$\theta_{JA} = 0.37^\circ\text{C/W}$$

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$$\theta_{SA} = \text{Thermal resistance of the heat sink in } ^\circ\text{C/W}$$

$$\theta_{SA} = \theta_{JA(\text{TOTAL})} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33^\circ\text{C/W} - 8.28^\circ\text{C/W} - 0.37^\circ\text{C/W} = 5.01^\circ\text{C/W}$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Microsemi FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 3-7 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V)

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.88	0.93	0.95	1.00	1.02	1.05
1.500	0.83	0.88	0.90	0.95	0.96	0.99
1.575	0.80	0.85	0.87	0.91	0.93	0.96

RAM Dynamic Contribution— P_{MEMORY}

Operating Mode

$$P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE-CLOCK})$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-17 on page 3-27.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-17 on page 3-27.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

Standby Mode and Sleep Mode

$$P_{MEMORY} = 0 \text{ W}$$

PLL/CCC Dynamic Contribution— P_{PLL}

Operating Mode

$$P_{PLL} = PAC13 * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Standby Mode and Sleep Mode

$$P_{PLL} = 0 \text{ W}$$

Nonvolatile Memory Dynamic Contribution— P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

$$P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * PAC15 * F_{READ-NVM} \text{ when } F_{READ-NVM} \leq 33 \text{ MHz,}$$

$$P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * (PAC16 + PAC17 * F_{READ-NVM} \text{ when } F_{READ-NVM} > 33 \text{ MHz}$$

$N_{NVM-BLOCKS}$ is the number of NVM blocks used in the design (2 in AFS600).

β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state).

$F_{READ-NVM}$ is the NVM read clock frequency.

Standby Mode and Sleep Mode

$$P_{NVM} = 0 \text{ W}$$

Crystal Oscillator Dynamic Contribution— $P_{XTL-OSC}$

Operating Mode

$$P_{XTL-OSC} = PAC18$$

Standby Mode

$$P_{XTL-OSC} = PAC18$$

Sleep Mode

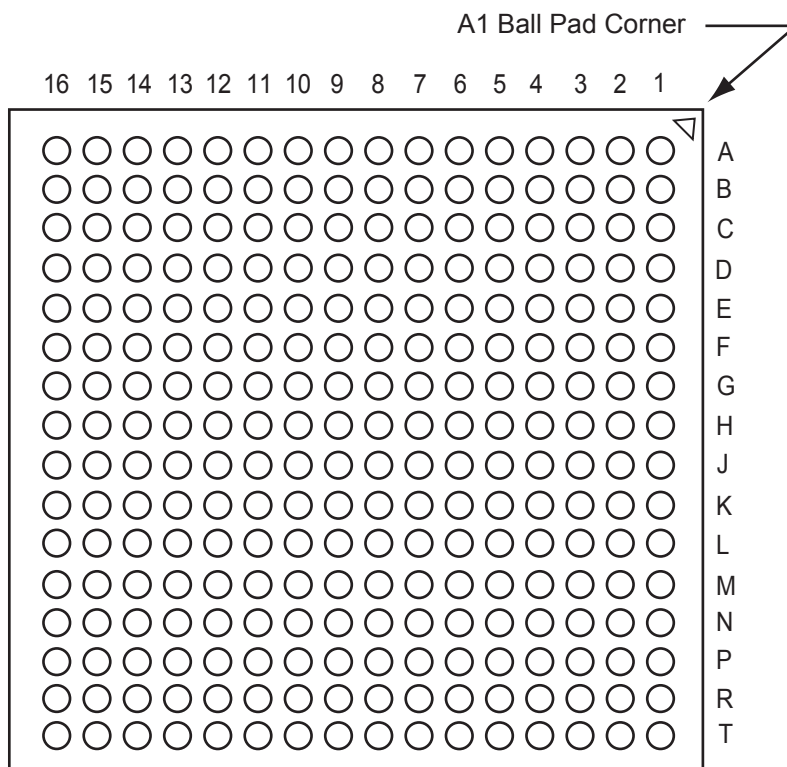
$$P_{XTL-OSC} = 0 \text{ W}$$

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.

PQ208		
Pin Number	AFS250 Function	AFS600 Function
147	GCC1/IO47PDB1V0	IO39NDB2V0
148	IO42NDB1V0	GCA2/IO39PDB2V0
149	GBC2/IO42PDB1V0	IO31NDB2V0
150	VCCIB1	GBB2/IO31PDB2V0
151	GND	IO30NDB2V0
152	VCC	GBA2/IO30PDB2V0
153	IO41NDB1V0	VCCIB2
154	GBB2/IO41PDB1V0	GNDQ
155	IO40NDB1V0	VCOMPLB
156	GBA2/IO40PDB1V0	VCCPLB
157	GBA1/IO39RSB0V0	VCCIB1
158	GBA0/IO38RSB0V0	GNDQ
159	GBB1/IO37RSB0V0	GBB1/IO27PPB1V1
160	GBB0/IO36RSB0V0	GBA1/IO28PPB1V1
161	GBC1/IO35RSB0V0	GBB0/IO27NPB1V1
162	VCCIB0	GBA0/IO28NPB1V1
163	GND	VCCIB1
164	VCC	GND
165	GBC0/IO34RSB0V0	VCC
166	IO33RSB0V0	GBC1/IO26PDB1V1
167	IO32RSB0V0	GBC0/IO26NDB1V1
168	IO31RSB0V0	IO24PPB1V1
169	IO30RSB0V0	IO23PPB1V1
170	IO29RSB0V0	IO24NPB1V1
171	IO28RSB0V0	IO23NPB1V1
172	IO27RSB0V0	IO22PPB1V0
173	IO26RSB0V0	IO21PPB1V0
174	IO25RSB0V0	IO22NPB1V0
175	VCCIB0	IO21NPB1V0
176	GND	IO20PSB1V0
177	VCC	IO19PSB1V0
178	IO24RSB0V0	IO14NSB0V1
179	IO23RSB0V0	IO12PDB0V1
180	IO22RSB0V0	IO12NDB0V1
181	IO21RSB0V0	VCCIB0
182	IO20RSB0V0	GND
183	IO19RSB0V0	VCC

PQ208		
Pin Number	AFS250 Function	AFS600 Function
184	IO18RSB0V0	IO10PPB0V1
185	IO17RSB0V0	IO09PPB0V1
186	IO16RSB0V0	IO10NPB0V1
187	IO15RSB0V0	IO09NPB0V1
188	VCCIB0	IO08PPB0V1
189	GND	IO07PPB0V1
190	VCC	IO08NPB0V1
191	IO14RSB0V0	IO07NPB0V1
192	IO13RSB0V0	IO06PPB0V0
193	IO12RSB0V0	IO05PPB0V0
194	IO11RSB0V0	IO06NPB0V0
195	IO10RSB0V0	IO04PPB0V0
196	IO09RSB0V0	IO05NPB0V0
197	IO08RSB0V0	IO04NPB0V0
198	IO07RSB0V0	GAC1/IO03PDB0V0
199	IO06RSB0V0	GAC0/IO03NDB0V0
200	GAC1/IO05RSB0V0	VCCIB0
201	VCCIB0	GND
202	GND	VCC
203	VCC	GAB1/IO02PDB0V0
204	GAC0/IO04RSB0V0	GAB0/IO02NDB0V0
205	GAB1/IO03RSB0V0	GAA1/IO01PDB0V0
206	GAB0/IO02RSB0V0	GAA0/IO01NDB0V0
207	GAA1/IO01RSB0V0	GNDQ
208	GAA0/IO00RSB0V0	VCCIB0

FG256



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/default.aspx>.

Revision	Changes	Page
Revision 2 (continued)	A note was added to Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro) stating that the user is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off (SAR 21773).	2-31
	VPUMP was incorrectly represented as VPP in several places. This was corrected to VPUMP in the "Standby and Sleep Mode Circuit Implementation" section and Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics (21963).	2-32, 3-10
	Additional information was added to the Flash Memory Block "Write Operation" section, including an explanation of the fact that a copy-page operation takes no less than 55 cycles (SAR 26338).	2-45
	The "FlashROM" section was revised to refer to Figure 2-46 • FlashROM Timing Diagram and Table 2-26 • FlashROM Access Time rather than stating 20 MHz as the maximum FlashROM access clock and 10 ns as the time interval for D0 to become valid or invalid (SAR 22105).	2-53, 2-54
	The following figures were deleted (SAR 29991). Reference was made to a new application note, <i>Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs</i> , which covers these cases in detail (SAR 34862). Figure 2-55 • Write Access after Write onto Same Address Figure 2-56 • Read Access after Write onto Same Address Figure 2-57 • Write Access after Read onto Same Address The port names in the SRAM "Timing Waveforms", "Timing Characteristics", SRAM tables, Figure 2-55 • RAM Reset . Applicable to both RAM4K9 and RAM512x18., and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35753).	2-63, 2-66, 2-65, 2-75
	In several places throughout the datasheet, GNDREF was corrected to ADCGNDREF (SAR 20783): Figure 2-64 • Analog Block Macro Table 2-36 • Analog Block Pin Description "ADC Operation" section	2-77 2-78 2-104
	The following note was added below Figure 2-78 • Timing Diagram for the Temperature Monitor Strobe Signal : When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 μ A sink into the Fusion device. (SAR 24796).	2-93
	The "Analog-to-Digital Converter Block" section was extensively revised, reorganizing the information and adding the "ADC Theory of Operation" section and "Acquisition Time or Sample Time Control" section. The "ADC Example" section was reworked and corrected (SAR 20577).	2-96
	Table 2-49 • Analog Channel Specifications was modified to include calibrated and uncalibrated values for offset (AFS090 and AFS250) for the external and internal temperature monitors. The "Offset" section was revised accordingly and now references Table 2-49 • Analog Channel Specifications (SARs 22647, 27015).	2-95, 2-117
	The "Intra-Conversion" section and "Injected Conversion" section had definitions incorrectly interchanged and have been corrected. Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram were also incorrectly interchanged and have been replaced correctly. Reference in the figure notes to EQ 10 has been corrected to EQ 23 (SAR 20547).	2-110, 2-113, 2-113