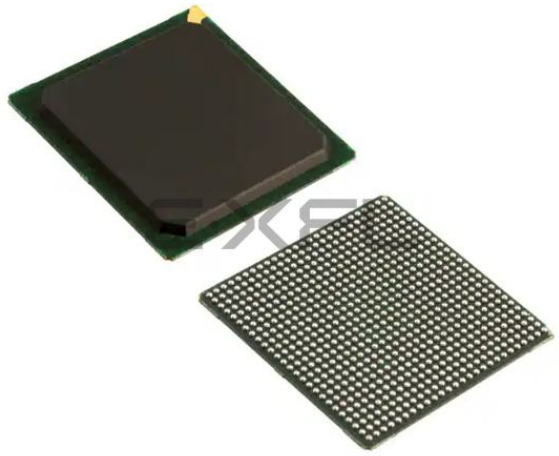

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	252
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-1fgg676

Temperature Grade Offerings

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
ARM Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500
Pigeon Point Devices			P1AFS600 [3]	P1AFS1500 [3]
MicroBlade Devices		U1AFS250 [4]	U1AFS600 [4]	U1AFS1500 [4]
QN108 [5]	C, I	–	–	–
QN180 [5]	C, I	C, I	–	–
PQ208	–	C, I	C, I	–
FG256	C, I	C, I	C, I	C, I
FG484	–	–	C, I	C, I
FG676	–	–	–	C, I

Notes:
1. *C = Commercial Temperature Range: 0°C to 85°C Junction*
2. *I = Industrial Temperature Range: –40°C to 100°C Junction*
3. *Pigeon Point devices are only offered in FG484 and FG256.*
4. *MicroBlade devices are only offered in FG256.*
5. *Package not available.*

Speed Grade and Temperature Grade Matrix

	Std.[1]	–1	–2[2]
C[3]	✓	✓	✓
I[4]	✓	✓	✓

Notes:
1. *MicroBlade devices are only offered in standard speed grade.*
2. *Pigeon Point devices are only offered in –2 speed grade.*
3. *C = Commercial Temperature Range: 0°C to 85°C Junction*
4. *I = Industrial Temperature Range: –40°C to 100°C Junction*

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/index.php?option=com_content&id=137&lang=en&view=article.

Cortex-M1, Pigeon Point, and MicroBlade Fusion Device Information

This datasheet provides information for all Fusion (AFS), Cortex-M1 (M1), Pigeon Point (P1), and MicroBlade (U1) devices. The remainder of the document will only list the Fusion (AFS) devices. Please apply relevant information to M1, P1, and U1 devices when appropriate. Please note the following:

- Cortex-M1 devices are offered in the same speed grades and packages as basic Fusion devices.
- Pigeon Point devices are only offered in –2 speed grade and FG484 and FG256 packages.
- MicroBlade devices are only offered in standard speed grade and the FG256 package.

The FlashPoint tool in the Fusion development software solutions, Libero SoC and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

Clock Resources

PLLs and Clock Conditioning Circuits (CCCs)

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. In the two larger family members, two of these CCCs also include a PLL; the smaller devices support one PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
  - 100 MHz on-chip RC oscillator
  - Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
  - 70 ps at 350 MHz
  - 90 ps at 100 MHz
  - 180 ps at 24 MHz
  - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 µs
- Low power consumption of 5 mW

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

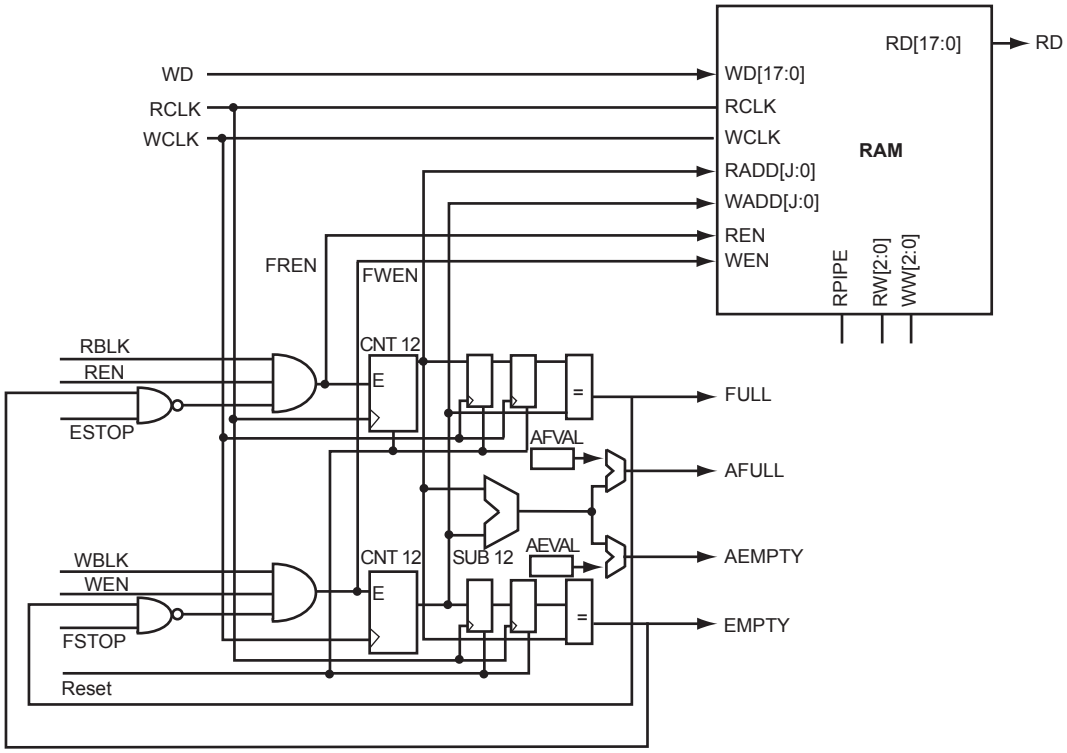


Figure 2-47 • **Fusion RAM Block with Embedded FIFO Controller**

Timing Characteristics

Table 2-35 • FIFO
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup time	1.34	1.52	1.79	ns
t_{ENH}	REN, WEN Hold time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold time	0.00	0.00	0.00	ns
t_{DS}	Input data (WD) Setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Terminology

Resolution

Resolution defines the smallest temperature change Fusion Temperature Monitor can resolve. For ADC configured as 8-bit mode, each LSB represents 4°C, and 1°C per LSB for 10-bit mode. With 12-bit mode, the Temperature Monitor can still only resolve 1°C due to Temperature Monitor design.

Offset

The Fusion Temperature Monitor has a systematic offset (Table 2-49 on page 2-117), excluding error due to board resistance and ideality factor of the external diode. Microsemi provides an IP block (CalibIP) that is required in order to mitigate the systematic temperature offset. For further details on CalibIP, refer to the "*Temperature*, *Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide*.

***Table 2-49* • Analog Channel Specifications (continued)**
Commercial Temperature Range Conditions, T_J = 85°C (unless noted otherwise),
Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Digital Input using Analog Pads AV, AC and AT						
VIND[2,3]	Input Voltage	Refer to Table 3-2 on page 3-3				
VHYSDIN	Hysteresis			0.3		V
VIHDIN	Input High			1.2		V
VILDIN	Input Low			0.9		V
VMPWDIN	Minimum Pulse With		50			ns
F_{DIN}	Maximum Frequency				10	MHz
ISTBDIN	Input Leakage Current			2		µA
IDYNDIN	Dynamic Current			20		µA
t_{INDIN}	Input Delay			10		ns
Gate Driver Output Using Analog Pad AG						
VG	Voltage Range	Refer to Table 3-2 on page 3-3				
IG	Output Current Drive	High Current Mode[6] at 1.0 V			±20	mA
		Low Current Mode: ±1 µA	0.8	1.0	1.3	µA
		Low Current Mode: ±3 µA	2.0	2.7	3.3	µA
		Low Current Mode: ± 10 µA	7.4	9.0	11.5	µA
		Low Current Mode: ± 30 µA	21.0	27.0	32.0	µA
IOFFG	Maximum Off Current				100	nA
F_G	Maximum switching rate	High Current Mode[6] at 1.0 V, 1 kΩ resistive load		1.3		MHz
		Low Current Mode: ±1 µA, 3 MΩ resistive load		3		KHz
		Low Current Mode: ±3 µA, 1 MΩ resistive load		7		KHz
		Low Current Mode: ±10 µA, 300 kΩ resistive load		25		KHz
		Low Current Mode: ±30 µA, 105 kΩ resistive load		78		KHz

Notes:

1. *VRSM is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.*
3. *VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User Guide.

***Table 2-73* • Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os; All I/O Bank Types (maximum drive strength and high slew selected)**

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
LVPECL	300 MHz

User I/O Naming Convention

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).

n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-22 on page 2-25 shows the three input pins per clock source MUX at CCC location m.

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.

x = P (Positive) or N (Negative) for differential pairs, or R (Regular – single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as an LVPECL pair.

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.

V = Reference voltage

z = Minibank number

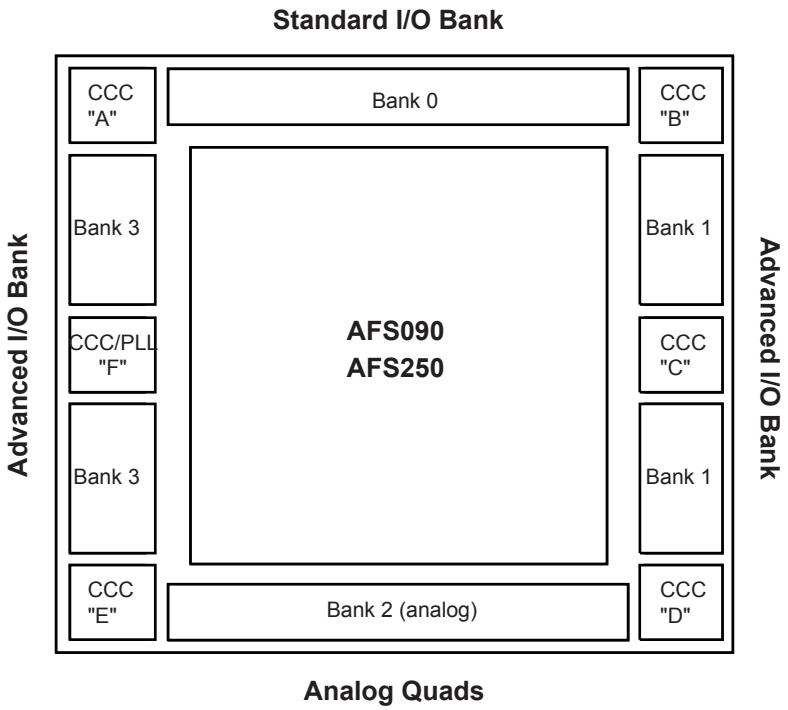


***Figure 2-113* • Naming Conventions of Fusion Devices with Three Digital I/O Banks**

Table 2-96 • I/O Output Buffer Maximum Resistances [1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	17 mA	27	31
SSTL2 (II)	21 mA	13	15
SSTL3 (I)	16 mA	44	69
SSTL3 (II)	24 mA	18	32
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$

Table 2-115 • 2.5 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	–1	0.56	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	–2	0.49	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
8 mA	Std.	0.66	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	–1	0.56	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	–2	0.49	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	–1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	–2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
16 mA	Std.	0.66	3.35	0.04	1.31	0.43	3.41	3.06	3.36	3.55	5.65	5.30	ns
	–1	0.56	2.85	0.04	1.11	0.36	2.90	2.60	2.86	3.02	4.81	4.51	ns
	–2	0.49	2.50	0.03	0.98	0.32	2.55	2.29	2.51	2.65	4.22	3.96	ns
24 mA	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	–1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	–2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-116 • 2.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	–1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	–2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
4 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	–1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	–2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
6 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	–1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	–2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns
8 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	–1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	–2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF **Analog Reference Ground**

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA **Ground (analog)**

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ **Ground (analog quiet)**

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM **Flash Memory Ground**

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC **Oscillator Ground**

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A **Analog Power Supply (1.5 V)**

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N **Negative 3.3 V Output**

This is the –3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to ground.

VCC33PMP **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM **Flash Memory Block Power Supply (1.5 V)**

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC **Oscillator Power Supply (3.3 V)**

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33 pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

Table 3-1 • **Absolute Maximum Ratings (continued)**

Symbol	Parameter	Commercial	Industrial	Units
AV, AC	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.6	–11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	–0.4 to 12.6	–0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.4 to 3.75	–0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range)	–11.0 to 0.4	–11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range)	–3.75 to 0.4	–3.75 to 0.4	V
	Analog input (direct input to ADC)	–0.4 to 3.75	–0.4 to 3.75	V
	Digital input	–0.4 to 12.6	–0.4 to 12.0	V
AG	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.6	–11.0 to 12.0	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)	–0.4 to 12.6	–0.4 to 12.0	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)	–11.0 to 0.4	–11.0 to 0.4	V
	High Current Mode [3]	–11.0 to 12.6	–11.0 to 12.0	V
AT	Unpowered, ADC reset asserted or unconfigured	–0.4 to 16.0	–0.4 to 15.0	V
	Analog input (+16 V, 4 V prescaler range)	–0.4 to 16.0	–0.4 to 15.0	V
	Analog input (direct input to ADC)	–0.4 to 3.75	–0.4 to 3.75	V
	Digital input	–0.4 to 16.0	–0.4 to 15.0	V
T_{STG} [4]	Storage temperature	–65 to +150		°C
T_J [4]	Junction temperature	+125		°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-4.*
2. *Analog data not valid beyond 3.65 V.*
3. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
4. *For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.*

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • **AFS1500 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min.	Typ.	Max.	Unit
ICC[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		20	40	mA
			T_J = 85°C		32	65	mA
			T_J = 100°C		59	120	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
ICC33[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		10.7	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.31	2	mA
			T_J = 85°C		0.35	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.9	3.6	mA
			T_J = 85°C		2.9	4	mA
			T_J = 100°C		3.3	6	mA
		Sleep mode[6], VCC33 = 3.63 V	T_J = 25°C		17	19	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
ICCI[3]	I/O quiescent current	Operational standby[4], Standby mode, and Sleep Mode[6], VCCIx = 3.63 V	T_J = 25°C		417	649	µA
			T_J = 85°C		417	649	µA
			T_J = 100°C		417	649	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

PLL/CCC Contribution—P_{PLL}

PLL is not used in this application.

P_{PLL} = 0 W

Nonvolatile Memory—P_{NVM}

Nonvolatile memory is not used in this application.

P_{NVM} = 0 W

Crystal Oscillator—$P_{XTL-OSC}$

The application utilizes standby mode. The crystal oscillator is assumed to be active.

Operating Mode

$P_{XTL-OSC}$ = PAC18

$P_{XTL-OSC}$ = 0.63 mW

Standby Mode

$P_{XTL-OSC}$ = PAC18

$P_{XTL-OSC}$ = 0.63 mW

Sleep Mode

$P_{XTL-OSC}$ = 0 W

RC Oscillator—P_{RC-OSC}

Operating Mode

P_{RC-OSC} = PAC19

P_{RC-OSC} = 3.30 mW

Standby Mode and Sleep Mode

P_{RC-OSC} = 0 W

Analog System—P_{AB}

Number of Quads used: N_{QUADS} = 4

Operating Mode

P_{AB} = PAC20

P_{AB} = 3.00 mW

Standby Mode and Sleep Mode

P_{AB} = 0 W

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL-OSC} + P_{RC-OSC} + P_{AB}$

P_{DYN} = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P_{DYN} = 143.06 mW

Standby Mode

$P_{DYN} = P_{XTL-OSC}$

P_{DYN} = 0.63 mW

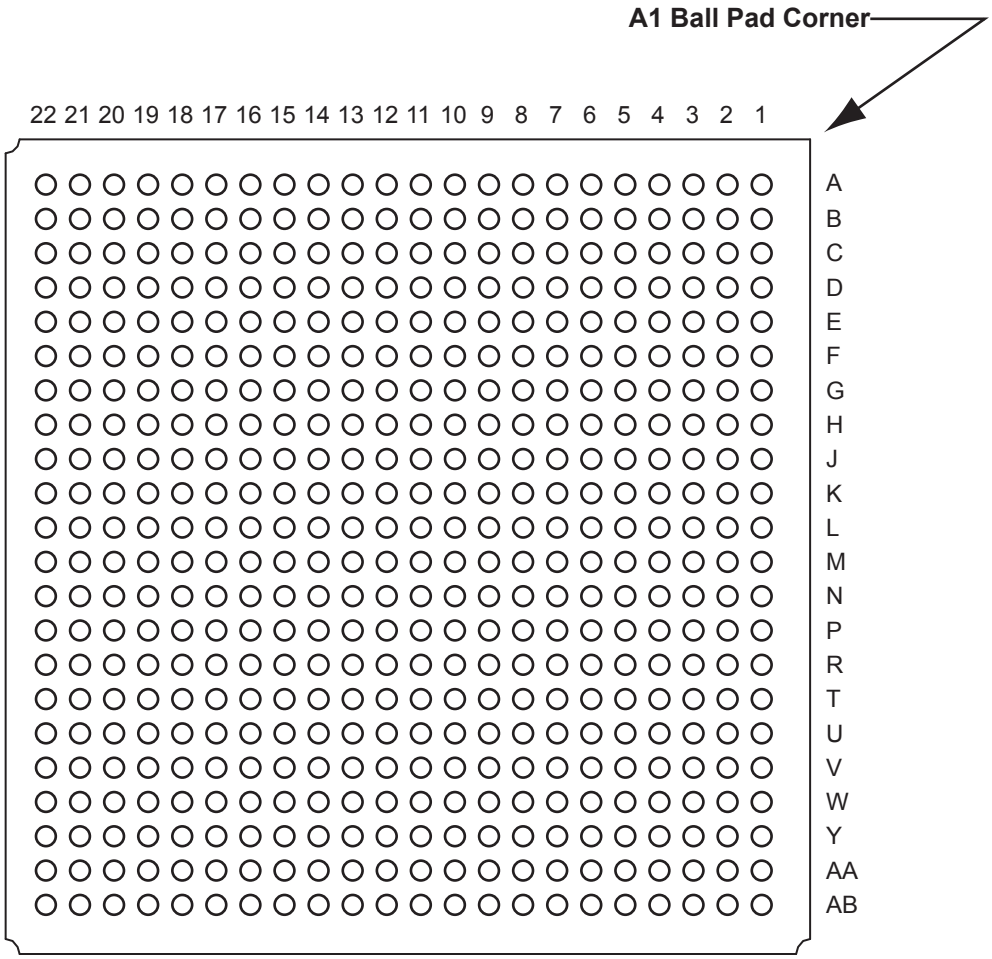
Sleep Mode

P_{DYN} = 0 W

PQ208		
Pin Number	AFS250 Function	AFS600 Function
1	VCCPLA	VCCPLA
2	VCOMPLA	VCOMPLA
3	GNDQ	GAA2/IO85PDB4V0
4	VCCIB3	IO85NDB4V0
5	GAA2/IO76PDB3V0	GAB2/IO84PDB4V0
6	IO76NDB3V0	IO84NDB4V0
7	GAB2/IO75PDB3V0	GAC2/IO83PDB4V0
8	IO75NDB3V0	IO83NDB4V0
9	NC	IO77PDB4V0
10	NC	IO77NDB4V0
11	VCC	IO76PDB4V0
12	GND	IO76NDB4V0
13	VCCIB3	VCC
14	IO72PDB3V0	GND
15	IO72NDB3V0	VCCIB4
16	GFA2/IO71PDB3V0	GFA2/IO75PDB4V0
17	IO71NDB3V0	IO75NDB4V0
18	GFB2/IO70PDB3V0	GFC2/IO73PDB4V0
19	IO70NDB3V0	IO73NDB4V0
20	GFC2/IO69PDB3V0	VCCOSC
21	IO69NDB3V0	XTAL1
22	VCC	XTAL2
23	GND	GNDOSC
24	VCCIB3	GFC1/IO72PDB4V0
25	GFC1/IO68PDB3V0	GFC0/IO72NDB4V0
26	GFC0/IO68NDB3V0	GFB1/IO71PDB4V0
27	GFB1/IO67PDB3V0	GFB0/IO71NDB4V0
28	GFB0/IO67NDB3V0	GFA1/IO70PDB4V0
29	VCCOSC	GFA0/IO70NDB4V0
30	XTAL1	IO69PDB4V0
31	XTAL2	IO69NDB4V0
32	GNDOSC	VCC
33	GEB1/IO62PDB3V0	GND
34	GEB0/IO62NDB3V0	VCCIB4
35	GEA1/IO61PDB3V0	GEC1/IO63PDB4V0
36	GEA0/IO61NDB3V0	GEC0/IO63NDB4V0
37	GEC2/IO60PDB3V0	GEB1/IO62PDB4V0

PQ208		
Pin Number	AFS250 Function	AFS600 Function
38	IO60NDB3V0	GEB0/IO62NDB4V0
39	GND	GEA1/IO61PDB4V0
40	VCCIB3	GEA0/IO61NDB4V0
41	GEB2/IO59PDB3V0	GEC2/IO60PDB4V0
42	IO59NDB3V0	IO60NDB4V0
43	GEA2/IO58PDB3V0	VCCIB4
44	IO58NDB3V0	GNDQ
45	VCC	VCC
45	VCC	VCC
46	VCCNVM	VCCNVM
47	GNDNVM	GNDNVM
48	GND	GND
49	VCC15A	VCC15A
50	PCAP	PCAP
51	NCAP	NCAP
52	VCC33PMP	VCC33PMP
53	VCC33N	VCC33N
54	GNDA	GNDA
55	GNDAQ	GNDAQ
56	NC	AV0
57	NC	AC0
58	NC	AG0
59	NC	AT0
60	NC	ATRTN0
61	NC	AT1
62	NC	AG1
63	NC	AC1
64	NC	AV1
65	AV0	AV2
66	AC0	AC2
67	AG0	AG2
68	AT0	AT2
69	ATRTN0	ATRTN1
70	AT1	AT3
71	AG1	AG3
72	AC1	AC3
73	AV1	AV3

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

FG484		
Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND
A2	VCC	NC
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0
A6	IO07NDB0V1	IO07NDB0V1
A7	IO07PDB0V1	IO07PDB0V1
A8	IO10PDB0V1	IO09PDB0V1
A9	IO14NDB0V1	IO13NDB0V2
A10	IO14PDB0V1	IO13PDB0V2
A11	IO17PDB1V0	IO24PDB1V0
A12	IO18PDB1V0	IO26PDB1V0
A13	IO19NDB1V0	IO27NDB1V1
A14	IO19PDB1V0	IO27PDB1V1
A15	IO24NDB1V1	IO35NDB1V2
A16	IO24PDB1V1	IO35PDB1V2
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A19	IO29NDB1V1	IO43NDB1V2
A20	IO29PDB1V1	IO43PDB1V2
A21	VCC	NC
A22	GND	GND
AA1	VCC	NC
AA2	GND	GND
AA3	VCCIB4	VCCIB4
AA4	VCCIB4	VCCIB4
AA5	PCAP	PCAP
AA6	AG0	AG0
AA7	GNDA	GNDA
AA8	AG1	AG1
AA9	AG2	AG2
AA10	GNDA	GNDA
AA11	AG3	AG3
AA12	AG6	AG6
AA13	GNDA	GNDA

FG484		
Pin Number	AFS600 Function	AFS1500 Function
AA14	AG7	AG7
AA15	AG8	AG8
AA16	GNDA	GNDA
AA17	AG9	AG9
AA18	VAREF	VAREF
AA19	VCCIB2	VCCIB2
AA20	PTEM	PTEM
AA21	GND	GND
AA22	VCC	NC
AB1	GND	GND
AB2	VCC	NC
AB3	NC	IO94NSB4V0
AB4	GND	GND
AB5	VCC33N	VCC33N
AB6	AT0	AT0
AB7	ATRTN0	ATRTN0
AB8	AT1	AT1
AB9	AT2	AT2
AB10	ATRTN1	ATRTN1
AB11	AT3	AT3
AB12	AT6	AT6
AB13	ATRTN3	ATRTN3
AB14	AT7	AT7
AB15	AT8	AT8
AB16	ATRTN4	ATRTN4
AB17	AT9	AT9
AB18	VCC33A	VCC33A
AB19	GND	GND
AB20	NC	IO76NPB2V0
AB21	VCC	NC
AB22	GND	GND
B1	VCC	NC
B2	GND	GND
B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
B4	GND	GND

FG676	
Pin Number	AFS1500 Function
C9	IO07PDB0V1
C10	IO09PDB0V1
C11	IO13NDB0V2
C12	IO13PDB0V2
C13	IO24PDB1V0
C14	IO26PDB1V0
C15	IO27NDB1V1
C16	IO27PDB1V1
C17	IO35NDB1V2
C18	IO35PDB1V2
C19	GBC0/IO40NDB1V2
C20	GBA0/IO42NDB1V2
C21	IO43NDB1V2
C22	IO43PDB1V2
C23	NC
C24	GND
C25	NC
C26	NC
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO01NDB0V0
D6	GND
D7	IO04NDB0V0
D8	IO04PDB0V0
D9	GND
D10	IO09NDB0V1
D11	IO11PDB0V1
D12	GND
D13	IO24NDB1V0
D14	IO26NDB1V0
D15	GND
D16	IO31NDB1V1
D17	IO31PDB1V1
D18	GND

FG676	
Pin Number	AFS1500 Function
D19	GBC1/IO40PDB1V2
D20	GBA1/IO42PDB1V2
D21	GND
D22	VCCPLB
D23	GND
D24	NC
D25	NC
D26	NC
E1	GND
E2	IO122NPB4V0
E3	IO121PDB4V0
E4	IO122PPB4V0
E5	IO00NDB0V0
E6	IO00PDB0V0
E7	VCCIB0
E8	IO05NDB0V1
E9	IO05PDB0V1
E10	VCCIB0
E11	IO11NDB0V1
E12	IO14PDB0V2
E13	VCCIB0
E14	VCCIB1
E15	IO29NDB1V1
E16	IO29PDB1V1
E17	VCCIB1
E18	IO37NDB1V2
E19	GBB0/IO41NDB1V2
E20	VCCIB1
E21	VCOMPLB
E22	GBA2/IO44PDB2V0
E23	IO48PPB2V0
E24	GBB2/IO45PDB2V0
E25	NC
E26	GND
F1	NC
F2	VCCIB4

FG676	
Pin Number	AFS1500 Function
F3	IO121NDB4V0
F4	GND
F5	IO123NDB4V0
F6	GAC2/IO123PDB4V0
F7	GAA2/IO125PDB4V0
F8	GAC0/IO03NDB0V0
F9	GAC1/IO03PDB0V0
F10	IO10NDB0V1
F11	IO10PDB0V1
F12	IO14NDB0V2
F13	IO23NDB1V0
F14	IO23PDB1V0
F15	IO32NPB1V1
F16	IO34NDB1V1
F17	IO34PDB1V1
F18	IO37PDB1V2
F19	GBB1/IO41PDB1V2
F20	VCCIB2
F21	IO47PPB2V0
F22	IO44NDB2V0
F23	GND
F24	IO45NDB2V0
F25	VCCIB2
F26	NC
G1	NC
G2	IO119PPB4V0
G3	IO120NDB4V0
G4	IO120PDB4V0
G5	VCCIB4
G6	GAB2/IO124PDB4V0
G7	IO125NDB4V0
G8	GND
G9	VCCIB0
G10	IO08NDB0V1
G11	IO08PDB0V1
G12	GND

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