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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-2fg484

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1 – Fusion Device Family Overview

Introduction

The Fusion mixed signal FPGA satisfies the demand from system architects for a device that simplifies design and unleashes their creativity. As the world's first mixed signal programmable logic family, Fusion integrates mixed signal analog, flash memory, and FPGA fabric in a monolithic device. Fusion devices enable designers to quickly move from concept to completed design and then deliver feature-rich systems to market. This new technology takes advantage of the unique properties of Microsemi flash-based FPGAs, including a high-isolation, triple-well process and the ability to support high-voltage transistors to meet the demanding requirements of mixed signal system design.

Fusion mixed signal FPGAs bring the benefits of programmable logic to many application areas, including power management, smart battery charging, clock generation and management, and motor control. Until now, these applications have only been implemented with costly and space-consuming discrete analog components or mixed signal ASIC solutions. Fusion mixed signal FPGAs present new capabilities for system development by allowing designers to integrate a wide range of functionality into a single device, while at the same time offering the flexibility of upgrades late in the manufacturing process or after the device is in the field. Fusion devices provide an excellent alternative to costly and

time-consuming mixed signal ASIC designs. In addition, when used in conjunction with the ARM Cortex-M1 processor, Fusion technology represents the definitive mixed signal FPGA platform.

Flash-based Fusion devices are Instant On. As soon as system power is applied and within normal operating specifications, Fusion devices are working. Fusion devices have a 128-bit flash-based lock and industry-leading AES decryption, used to secure programmed intellectual property (IP) and configuration data. Fusion devices are the most comprehensive single-chip analog and digital programmable logic solution available today.

To support this new ground-breaking technology, Microsemi has developed a series of major tool innovations to help maximize designer productivity. Implemented as extensions to the popular Microsemi Libero[®] System-on-Chip (SoC) software, these new tools allow designers to easily instantiate and configure peripherals within a design, establish links between peripherals, create or import building blocks or reference designs, and perform hardware verification. This tool suite will also add comprehensive hardware/software debug capability as well as a suite of utilities to simplify development of embedded soft-processor-based solutions.

General Description

The Fusion family, based on the highly successful ProASIC[®]3 and ProASIC3E flash FPGA architecture, has been designed as a high-performance, programmable, mixed signal platform. By combining an advanced flash FPGA core with flash memory blocks and analog peripherals, Fusion devices dramatically simplify system design and, as a result, dramatically reduce overall system cost and board space.

The state-of-the-art flash memory technology offers high-density integrated flash memory blocks, enabling savings in cost, power, and board area relative to external flash solutions, while providing increased flexibility and performance. The flash memory blocks and integrated analog peripherals enable true mixed-mode programmable logic designs. Two examples are using an on-chip soft processor to implement a fully functional flash MCU and using high-speed FPGA logic to offer system and power supervisory capabilities. Instant On, and capable of operating from a single 3.3 V supply, the Fusion family is ideally suited for system management and control applications.

The devices in the Fusion family are categorized by FPGA core density. Each family member contains many peripherals, including flash memory blocks, an analog-to-digital-converter (ADC), high-drive outputs, both RC and crystal oscillators, and a real-time counter (RTC). This provides the user with a high level of flexibility and integration to support a wide variety of mixed signal applications. The flash memory block capacity ranges from 2 Mbits to 8 Mbits. The integrated 12-bit ADC supports up to 30 independently configurable input channels.



Timing Characteristics

Table 2-1 • Combinatorial Cell Propagation DelaysCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	Units
INV	Y = !A	t _{PD}	0.40	0.46	0.54	ns
AND2	$Y = A \cdot B$	t _{PD}	0.47	0.54	0.63	ns
NAND2	$Y = !(A \cdot B)$	t _{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t _{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t _{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t _{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t _{PD}	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	t _{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t _{PD}	0.51	0.58	0.68	ns
AND3	$Y = A \cdot B \cdot C$	t _{PD}	0.56	0.64	0.75	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library (Figure 2-5). For more details, refer to the *IGLOO*, *ProASIC3*, *SmartFusion and Fusion Macro Library Guide*.



Figure 2-5 • Sample of Sequential Cells







Signal Name	Width	Direction	Function						
XTL_EN*	1		Enables the	Enables the crystal. Active high.					
XTL_MODE*	2		Settings for	Settings for the crystal clock for different frequency.					
			Value	Modes Frequency Range					
			b'00	RC network	32 KHz to 4 MHz				
			b'01	Low gain	32 to 200 KHz				
			b'10	Medium gain	0.20 to 2.0 MHz				
			b'11	High gain	2.0 to 20.0 MHz				
SELMODE	1	IN	Selects the source of XTL_MODE and also enables the XTL_EN. Connect from RTCXTLSEL from AB.						
			0 For normal operation or sleep mode, XTL_EN depends on FPGA_EN, XTL_MODE depends on MODE						
			1 For Standby mode, XTL_EN is enabled, XTL_MODE depends on RTC_MODE						
RTC_MODE[1:0]	2	IN	Settings for the crystal clock for different frequency ranges. XTL_MODE uses RTC_MODE when SELMODE is '1'.						
MODE[1:0]	2	IN	Settings for the crystal clock for different frequency ranges. XTL_MODE uses MODE when SELMODE is '0'. In Standby, MODE inputs will be 0's.						
FPGA_EN*	1	IN	0 when 1.5	0 when 1.5 V is not present for VCC 1 when 1.5 V is present for VCC					
XTL	1	IN	Crystal Clock source						
CLKOUT	1	OUT	Crystal Cloo	Crystal Clock output					

Table 2-10 • XTLOSC Signals Descriptions

Note: *Internal signal—does not exist in macro.



The following signals are used to configure the FIFO4K18 memory element.

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-33).

TADIE 2-33 · ASDECLINALIO SELLINUS IOI WWWIZ.VI

WW2, WW1, WW0	RW2, RW1, RW0	D×W
000	000	4k×1
001	001	2k×2
010	010	1k×4
011	011	512×9
100	100	256×18
101, 110, 111	101, 110, 111	Reserved

WBLK and RBLK

These signals are active low and will enable the respective ports when Low. When the RBLK signal is High, the corresponding port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A Low on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins Low, the FULL and AFULL pins Low, and the EMPTY and AEMPTY pins High (Table 2-34).

Table 2-34 • Input Data Signal Usage for Different Aspect Ratios

D×W	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	-

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-34).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-34).





Figure 2-57 • FIFO Read







	VAREF		
	ADCGNDREF		
	AV0	DAVOUT0	
	AC0	DACOUT0	
	ΔΤΟ		
	•	DAIOUIU	
	• • •		
	AV9	DAVOUT9	
	AC9	DACOU19	
	AT9	DATOUT9	
	ATRETURN01		
	•	AG0	
	Å TRETURN9	AG1	
	DENAV0	•	
		<u>م</u>	
		A09	
	DENAIU		
	•		
	DENAV0		
	DENAC0		
	DENAT0		
	CMSTB0		
	•		
	ĊSMTB9		
	GDONO		
	CDON0		
	GDON9		
	IMSTBO		
	•		
	TMSTB9		
	MODE[3:0]	BUSY	
	TVC[7:0]	CALIBRATE	
	STC[7:0]	DATAVALID	
	CHNUMBER[4:0]	SAMPLE	
	TMSTINT	RESULTI11:01	
	ADCSTART	RTCMATCH	
	PWRDWN	RICXILSEL	
	ADCRESET	RTCPSMMATCH	
	RTCCLK		
	SYSCLK		
	ACMIVEN	ACMRDATA[7:0]	
<u> </u>	ACMRESET		
	ACMWDATA		
	ACMADDR		
	ACMCLK		
	AE	3	

Figure 2-64 • Analog Block Macro

Table 2-36 describes each pin in the Analog Block. Each function within the Analog Block will be explained in detail in the following sections.

Table 2-36 • Analog Block Pin Description

Signal Name	Number of Bits	Direction	Function	Location of Details
VAREF	1	Input/Output	Voltage reference for ADC	ADC
ADCGNDREF	1	Input	External ground reference	ADC
MODE[3:0]	4	Input	ADC operating mode	ADC
SYSCLK	1	Input	External system clock	
TVC[7:0]	8	Input	Clock divide control	ADC
STC[7:0]	8	Input	Sample time control	ADC
ADCSTART	1	Input	Start of conversion	ADC
PWRDWN	1	Input	ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin.	ADC
ADCRESET	1	Input	ADC resets and disables Analog Quad – active high	ADC
BUSY	1	Output	1 – Running conversion	ADC
CALIBRATE	1	Output	1 – Power-up calibration	ADC
DATAVALID	1	Output	1 – Valid conversion result	ADC
RESULT[11:0]	12	Output	Conversion result	ADC
TMSTBINT	1	Input	Internal temp. monitor strobe	ADC
SAMPLE	1	Output	 1 – An analog signal is actively being sampled (stays high during signal acquisition only) 0 – No analog signal is being sampled 	ADC
VAREFSEL	1	Input	0 = Output internal voltage reference (2.56 V) to VAREF 1 = Input external voltage reference	ADC
	_		from VAREF and ADCGNDREF	
CHNUMBER[4:0]	5	Input	Analog input channel select	Input multiplexer
ACMCLK	1	Input	ACM clock	ACM
ACMWEN	1	Input	ACM write enable – active high	ACM
ACMRESET	1	Input	ACM reset – active low	ACM
ACMWDATA[7:0]	8	Input	ACM write data	ACM
ACMRDATA[7:0]	8	Output	ACM read data	ACM
ACMADDR[7:0]	8	Input	ACM address	ACM
CMSTB0 to CMSTB9	10	Input	Current monitor strobe – 1 per quad, active high	Analog Quad



Typical scaling factors are given in Table 2-57 on page 2-130, and the gain error (which contributes to the minimum and maximum) is in Table 2-49 on page 2-117.





Terminology

BW – Bandwidth

BW is a range of frequencies that a Channel can handle.

Channel

A channel is define as an analog input configured as one of the Prescaler range shown in Table 2-57 on page 2-130. The channel includes the Prescaler circuit and the ADC.

Channel Gain

Channel Gain is a measured of the deviation of the actual slope from the ideal slope. The slope is measured from the 20% and 80% point.

Gain =
$$rac{ ext{Gain}_{ ext{actual}}}{ ext{Gain}_{ ext{ideal}}}$$

EQ 1

Channel Gain Error

Channel Gain Error is a deviation from the ideal slope of the transfer function. The Prescaler Gain Error is expressed as the percent difference between the actual and ideal, as shown in EQ 2.

$$\text{Error}_{\text{Gain}} = (1-\text{Gain}) \times 100\%$$

EQ 2



Gain Error

The gain error of an ADC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale (%FSR). Gain error is the full-scale error minus the offset error (Figure 2-84).



Figure 2-84 • Gain Error

Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

Timing Characteristics

Table 2-55 • Analog Configuration Multiplexer (ACM) TimingCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{CLKQACM}	Clock-to-Q of the ACM	19.73	22.48	26.42	ns
t _{SUDACM}	Data Setup time for the ACM	4.39	5.00	5.88	ns
t _{HDACM}	Data Hold time for the ACM	0.00	0.00	0.00	ns
t _{SUAACM}	Address Setup time for the ACM	4.73	5.38	6.33	ns
t _{HAACM}	Address Hold time for the ACM	0.00	0.00	0.00	ns
t _{SUEACM}	Enable Setup time for the ACM	3.93	4.48	5.27	ns
t _{HEACM}	Enable Hold time for the ACM	0.00	0.00	0.00	ns
t _{MPWARACM}	Asynchronous Reset Minimum Pulse Width for the ACM	10.00	10.00	10.00	ns
t _{REMARACM}	Asynchronous Reset Removal time for the ACM	12.98	14.79	17.38	ns
t _{RECARACM}	Asynchronous Reset Recovery time for the ACM	12.98	14.79	17.38	ns
t _{MPWCLKACM}	Clock Minimum Pulse Width for the ACM	45.00	45.00	45.00	ns
t _{FMAXCLKACM}	lock Maximum Frequency for the ACM	10.00	10.00	10.00	MHz

I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-84 and Table 2-85 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

Table 2-84 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)*	RES PULL	OUT_LOAD (output only)	COMBINE REGISTER
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3
PCI (3.3 V)			3		3	3
PCI-X (3.3 V)	3		3		3	3
LVDS, BLVDS, M-LVDS			3			3
LVPECL						3

Note: * This feature does not apply to the standard I/O banks, which are the north I/O banks of AFS090 and AFS250 devices





Figure 2-118 • Tristate Output Buffer Timing Model and Delays (example)



Table 2-96 • I/O Output Buffer Maximum Resistances ¹ (continued)

Standard	Drive Strength	R _{PULL-DOWN} (ohms) ²	R _{PULL-UP} (ohms) ³				
Applicable to Standard I/O Banks							
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300				
	4 mA	100	300				
	6 mA	50	150				
	8 mA	50	150				
2.5 V LVCMOS	2 mA	100	200				
	4 mA	100	200				
	6 mA	50	100				
	8 mA	50	100				
1.8 V LVCMOS	2 mA	200	225				
	4 mA	100	112				
1.5 V LVCMOS	2 mA	200	224				

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.

2. R_(PULL-DOWN-MAX) = VOLspec / I_{OLspec}

3. R_(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec

Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	R _{(WEAK I} (oh	PULL-UP) ms)	R _{(WEAK PUI} (ohr	LL-DOWN) ² ns)
VCCI	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

R_(WEAK PULL-UP-MAX) = (VCCImax – VOHspec) / I_{WEAK PULL-UP-MIN}
 R_(WEAK PULL-DOWN-MAX) = VOLspec / I_{WEAK PULL-DOWN-MIN}



Table 2-105 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/Os

Drive	Speed						^τ ΕΟU							11
Strength	Grade	TDOUT	τ _{DP}	τ _{DIN}	τ _{ΡΥ}	τ _{PYS}	Т	۲ZL	τzΗ	ιLZ	τ _{HZ}	τ _{ZLS}	τ _{zhs}	Units
4 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	-1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	-2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	-1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	-2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	-1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	-2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	-1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	-2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	-1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	-2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Table 2-121 • 1.8 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Applicable to Pro I/Os

Drive	Speed													
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	-1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	-2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	-1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	-2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
8 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	-1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	-2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
12 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	-1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	-2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	-1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	-2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-169 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.075	1.325	Cross point	_

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-170 • LVDS

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Pro I/Os

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	0.66	2.10	0.04	1.82	ns
-1	0.56	1.79	0.04	1.55	ns
-2	0.49	1.57	0.03	1.36	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations can contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus, since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-135. The input and output buffer delays are available in the LVDS section in Table 2-171.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case industrial operating conditions at the farthest receiver: $R_S = 60 \Omega$ and $R_T = 70 \Omega$, given $Z_0 = 50 \Omega$ (2") and $Z_{stub} = 50 \Omega$ (~1.5").



Figure 2-135 • BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers



Output Register





Timing Characteristics

Table 2-177 • Output Data Register Propagation DelaysCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
tosud	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t _{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
tosue	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t _{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t _{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t _{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t _{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
t _{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Total Static Power Consumption—PSTAT

Number of Quads used: $N_{QUADS} = 4$ Number of NVM blocks available (AFS600): $N_{NVM-BLOCKS} = 2$ Number of input pins used: $N_{INPUTS} = 30$ Number of output pins used: $N_{OUTPUTS} = 40$

Operating Mode

 $\mathsf{P}_{\mathsf{STAT}} = \mathsf{PDC1} + (\mathsf{N}_{\mathsf{NVM-BLOCKS}} * \mathsf{PDC4}) + \mathsf{PDC5} + (\mathsf{N}_{\mathsf{QUADS}} * \mathsf{PDC6}) + (\mathsf{N}_{\mathsf{INPUTS}} * \mathsf{PDC7}) + (\mathsf{N}_{\mathsf{OUTPUTS}} * \mathsf{PDC8})$

P_{STAT} = 7.50 mW + (2 * 1.19 mW) + 8.25 mW + (4 * 3.30 mW) + (30 * 0.00) + (40 * 0.00)

P_{STAT} = 31.33 mW

Standby Mode

P_{STAT} = PDC2

 P_{STAT} = 0.03 mW

Sleep Mode

 $P_{STAT} = PDC3$

 $P_{STAT} = 0.03 \text{ mW}$

Total Power Consumption—PTOTAL

In operating mode, the total power consumption of the device is 174.39 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{TOTAL} = 143.06 mW + 31.33 mW

P_{TOTAL} = 174.39 mW

In standby mode, the total power consumption of the device is limited to 0.66 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

 $P_{TOTAL} = 0.03 \text{ mW} + 0.63 \text{ mW}$

 $P_{TOTAL} = 0.66 \text{ mW}$

In sleep mode, the total power consumption of the device drops as low as 0.03 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$ $P_{TOTAL} = 0.03 \text{ mW}$



Datasheet Information

Revision	Changes	Page
Advance v1.0 (January 2008)	All Timing Characteristics tables were updated. For the Differential I/O Standards, the Standard I/O support tables are new.	N/A
	Table 2-3 • Array Coordinates was updated to change the max x and y values	2-9
	Table 2-12 • Fusion CCC/PLL Specification was updated.	2-31
	A note was added to Table 2-16 · RTC ACM Memory Map.	2-37
	A reference to the Peripheral's User's Guide was added to the "Voltage Regulator Power Supply Monitor (VRPSM)" section.	2-42
	In Table 2-25 • Flash Memory Block Timing, the commercial conditions were updated.	2-55
	In Table 2-26 • FlashROM Access Time, the commercial conditions were missing and have been added below the title of the table.	2-58
	In Table 2-36 • Analog Block Pin Description, the function description was updated for the ADCRESET.	2-82
	In the "Voltage Monitor" section, the following sentence originally had \pm 10% and it was changed to +10%.	2-86
	The Analog Quad inputs are tolerant up to 12 V + 10%.	
	In addition, this statement was deleted from the datasheet:	
	Each I/O will draw power when connected to power (3 mA at 3 V).	0.00
	The "Terminology" section is new.	2-88
	The "Current Monitor" section was significantly updated. Figure 2-72 • Timing Diagram for Current Monitor Strobe to Figure 2-74 • Negative Current Monitor and Table 2-37 • Recommended Resistor for Different Current Range Measurement are new.	2-90
	The "ADC Description" section was updated to add the "Terminology" section.	2-93
	In the "Gate Driver" section, 25 mA was changed to 20 mA and 1.5 MHz was changed to 1.3 MHz. In addition, the following sentence was deleted: The maximum AG pad switching frequency is 1.25 MHz.	2-94
	The "Temperature Monitor" section was updated to rewrite most of the text and add Figure 2-78, Figure 2-79, and Table 2-38 • Temperature Data Format.	2-96
	In Table 2-38 • Temperature Data Format, the temperature K column was changed for 85°C from 538 to 358.	2-98
	In Table 2-45 • ADC Interface Timing, "Typical-Case" was changed to "Worst-Case."	2-110
	The "ADC Interface Timing" section is new.	2-110
	Table 2-46 • Analog Channel Specifications was updated.	2-118
	The "V _{CC15A} Analog Power Supply (1.5 V)" section was updated.	2-224
	The "V _{CCPLA/B} PLL Supply Voltage" section is new.	2-225
	In "V $_{\rm CCNVM}$ Flash Memory Block Power Supply (1.5 V)" section, supply was changed to supply input.	2-224
	The "V_{CCPLAVB} PLL Supply Voltage" pin description was updated to include the following statement:	2-225
	Actel recommends tying VCCPLX to VCC and using proper filtering circuits to decouple V_{CC} noise from PLL.	
	The "V _{COMPLA/B} Ground for West and East PLL" section was updated.	2-225

Fusion Family of Mixed Signal FPGAs

Revision	Changes	Page					
Advance v0.6 (continued)	The "Analog-to-Digital Converter Block" section was updated with the following statement: "All results are MSB justified in the ADC."						
	The information about the ADCSTART signal was updated in the "ADC Description" section.						
	Table 2-46 · Analog Channel Specifications was updated.						
	Table 2-47 · ADC Characteristics in Direct Input Mode was updated.	2-121					
	Table 2-51 • ACM Address Decode Table for Analog Quad was updated.	2-127					
	In Table 2-53 • Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated.						
	The "Introduction" section was updated to include information about digital inputs, outputs, and bibufs.						
	In Table 2-69 • Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features:						
	Single-ended receiver						
	Voltage-reterenced differential receiver						
	The "liker I/O Naming Convention" section was undeted to include "V/" and "r"	2 150					
	descriptions	2-159					
	The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw.	2-224					
	The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw.	2-224					
	The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and V_{CCI} pins within a given I/O bank.	2-185					
	The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used.	2-228					
	The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used.	2-228					
	The "PTEM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used.	2-228					
	The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090.	3-8					