Microchip Technology - M1AFS1500-2FG676 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	252
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-2fg676

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Temperature Grade Offerings

Fusion Devices	**AFS090**	**AFS250**	**AFS600**	**AFS1500**
ARM Cortex-M1 Devices	▨	**M1AFS250**	**M1AFS600**	**M1AFS1500**
Pigeon Point Devices	▨	▨	**P1AFS600** [3]	**P1AFS1500** [3]
MicroBlade Devices	▨	**U1AFS250** [4]	**U1AFS600** [4]	**U1AFS1500** [4]
QN108 [5]	C, I	–	–	–
QN180 [5]	C, I	C, I	–	–
PQ208	–	C, I	C, I	–
FG256	C, I	C, I	C, I	C, I
FG484	–	–	C, I	C, I
FG676	–	–	–	C, I

Notes:
1. *C = Commercial Temperature Range: 0°C to 85°C Junction*
2. *I = Industrial Temperature Range: –40°C to 100°C Junction*
3. *Pigeon Point devices are only offered in FG484 and FG256.*
4. *MicroBlade devices are only offered in FG256.*
5. *Package not available.*

Speed Grade and Temperature Grade Matrix

	Std.[1]	**–1**	**–2**[2]
C[3]	✓	✓	✓
I[4]	✓	✓	✓

Notes:
1. *MicroBlade devices are only offered in standard speed grade.*
2. *Pigeon Point devices are only offered in –2 speed grade.*
3. *C = Commercial Temperature Range: 0°C to 85°C Junction*
4. *I = Industrial Temperature Range: –40°C to 100°C Junction*

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/index.php?option=com_content&id=137&lang=en&view=article.

Cortex-M1, Pigeon Point, and MicroBlade Fusion Device Information

This datasheet provides information for all Fusion (AFS), Cortex-M1 (M1), Pigeon Point (P1), and MicroBlade (U1) devices. The remainder of the document will only list the Fusion (AFS) devices. Please apply relevant information to M1, P1, and U1 devices when appropriate. Please note the following:

- Cortex-M1 devices are offered in the same speed grades and packages as basic Fusion devices.
- Pigeon Point devices are only offered in –2 speed grade and FG484 and FG256 packages.
- MicroBlade devices are only offered in standard speed grade and the FG256 package.

Global Clocking

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 KHz to 20 MHz)
- Ceramic (500 KHz to 8 MHz)
- RC (32.768 KHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Digital I/Os with Advanced I/O Standards

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

The I/Os are organized into banks, with four or five banks per device. The configuration of these banks determines the I/O standards supported. The banks along the east and west sides of the device support the full range of I/O standards (single-ended and differential). The south bank supports the Analog Quads (analog I/O). In the family's two smaller devices, the north bank supports multiple single-ended digital I/O standards. In the family’s larger devices, the north bank is divided into two banks of digital Pro I/Os, supporting a wide variety of single-ended, differential, and voltage-referenced I/O standards.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following applications:

- Single-Data-Rate (SDR) applications
- Double-Data-Rate (DDR) applications—DDR LVDS I/O for chip-to-chip communications
- Fusion banks support LVPECL, LVDS, BLVDS, and M-LVDS with 20 multi-drop points.

VersaTiles

The Fusion core consists of VersaTiles, which are also used in the successful ProASIC3 family. The Fusion VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set and optional enable

Refer to Figure 1-2 for the VersaTile configuration arrangement.

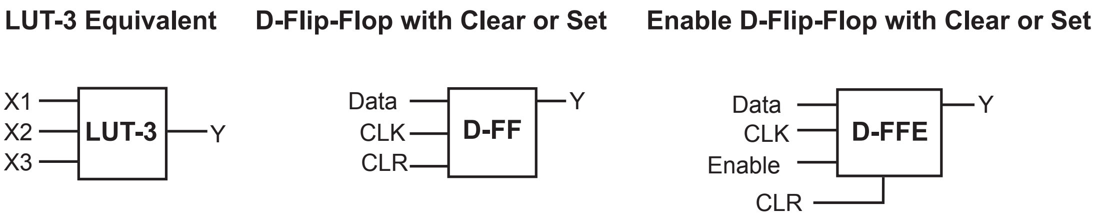


Figure 1-2 • **VersaTile Configurations**

2 – Device Architecture

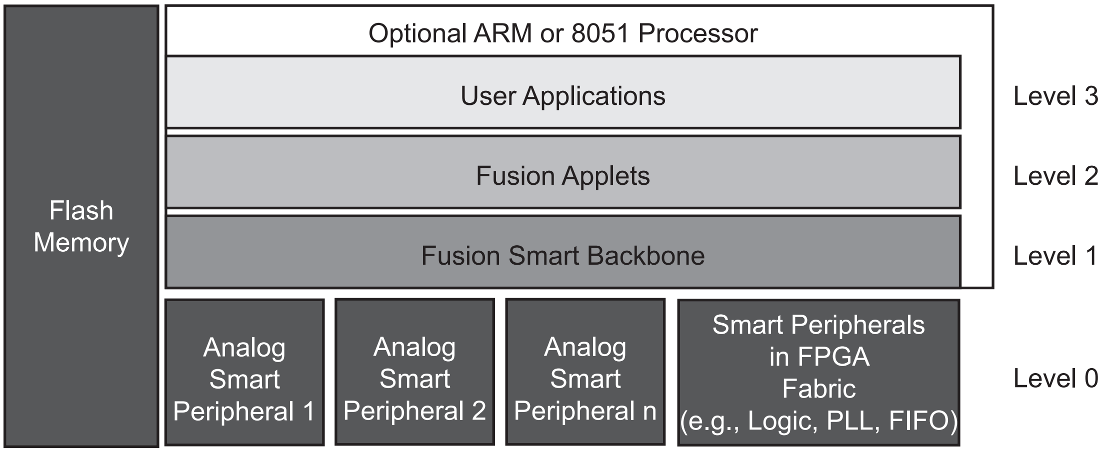
Fusion Stack Architecture

To manage the unprecedented level of integration in Fusion devices, Microsemi developed the Fusion technology stack (Figure 2-1). This layered model offers a flexible design environment, enabling design at very high and very low levels of abstraction. Fusion peripherals include hard analog IP and hard and soft digital IP. Peripherals communicate across the FPGA fabric via a layer of soft gates—the Fusion backbone. Much more than a common bus interface, this Fusion backbone integrates a micro-sequencer within the FPGA fabric and configures the individual peripherals and supports low-level processing of peripheral data. Fusion applets are application building blocks that can control and respond to peripherals and other system signals. Applets can be rapidly combined to create large applications. The technology is scalable across devices, families, design types, and user expertise, and supports a well-defined interface for external IP and tool integration.

At the lowest level, Level 0, are Fusion peripherals. These are configurable functional blocks that can be hardwired structures such as a PLL or analog input channel, or soft (FPGA gate) blocks such as a UART or two-wire serial interface. The Fusion peripherals are configurable and support a standard interface to facilitate communication and implementation.

Connecting and controlling access to the peripherals is the Fusion backbone, Level 1. The backbone is a soft-gate structure, scalable to any number of peripherals. The backbone is a bus and much more; it manages peripheral configuration to ensure proper operation. Leveraging the common peripheral interface and a low-level state machine, the backbone efficiently offloads peripheral management from the system design. The backbone can set and clear flags based upon peripheral behavior and can define performance criteria. The flexibility of the stack enables a designer to configure the silicon, directly bypassing the backbone if that level of control is desired.

One step up from the backbone is the Fusion applet, Level 2. The applet is an application building block that implements a specific function in FPGA gates. It can react to stimuli and board-level events coming through the backbone or from other sources, and responds to these stimuli by accessing and manipulating peripherals via the backbone or initiating some other action. An applet controls or responds to the peripheral(s). Applets can be easily imported or exported from the design environment. The applet structure is open and well-defined, enabling users to import applets from Microsemi, system developers, third parties, and user groups.



Note: Levels 1, 2, and 3 are implemented in FPGA logic gates.

Figure 2-1 • **Fusion Architecture Stack**

Clocking Resources

The Fusion family has a robust collection of clocking peripherals, as shown in the block diagram in Figure 2-16. These on-chip resources enable the creation, manipulation, and distribution of many clock signals. The Fusion integrated RC oscillator produces a 100 MHz clock source with no external components. For systems requiring more precise clock signals, the Fusion family supports an on-chip crystal oscillator circuit. The integrated PLLs in each Fusion device can use the RC oscillator, crystal oscillator, or another on-chip clock signal as a source. These PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay). Utilizing the CCC found in the popular ProASIC3 family, Fusion incorporates six CCC blocks. The CCCs allow access to Fusion global and local clock distribution nets, as described in the "Global Resources (VersaNets)" section on page 2-11.

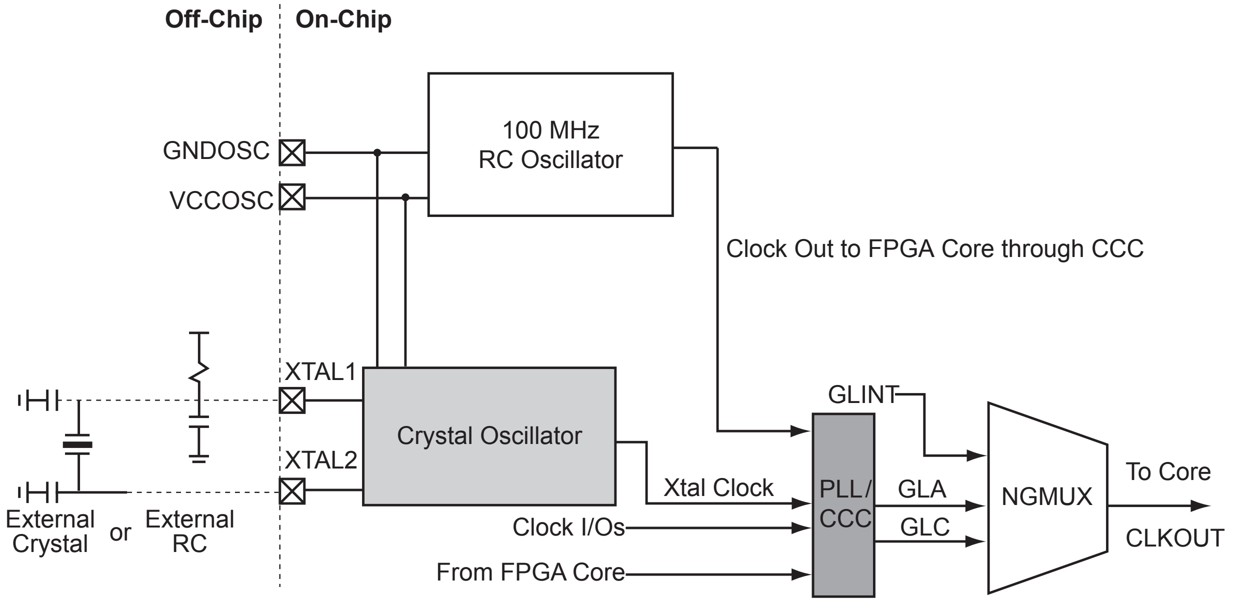


Figure 2-16 • **Fusion Clocking Options**

No-Glitch MUX (NGMUX)

Positioned downstream from the PLL/CCC blocks, the NGMUX provides a special switching sequence between two asynchronous clock domains that prevents generating any unwanted narrow clock pulses. The NGMUX is used to switch the source of a global between three different clock sources. Allowable inputs are either two PLL/CCC outputs or a PLL/CCC output and a regular net, as shown in Figure 2-24. The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). These are set by SmartGen during design but can also be changed by dynamically reconfiguring the PLL. The GLMUXSEL[1:0] bits control which clock source is passed through the NGMUX to the global network (GL). See Table 2-13.

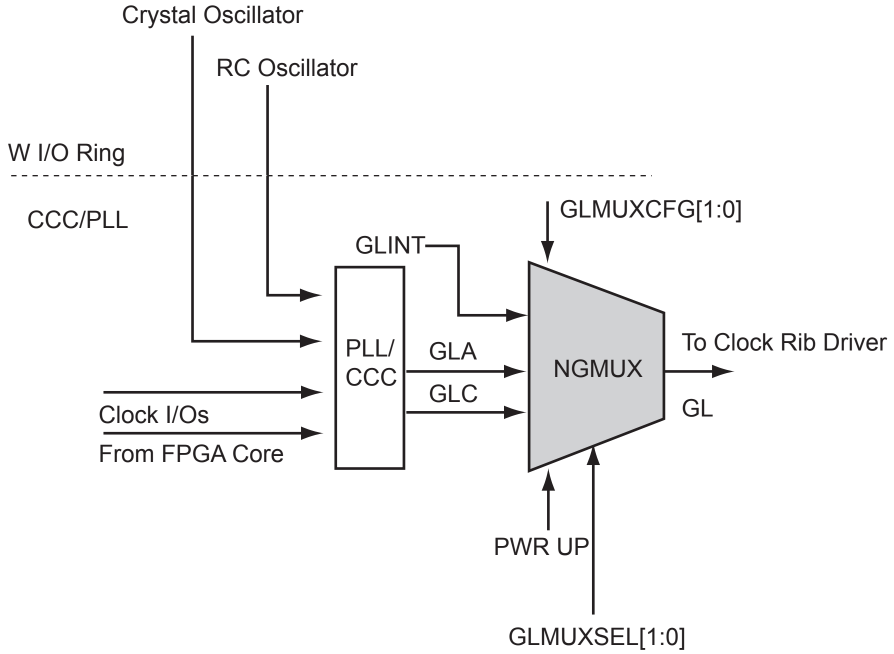


Figure 2-24 • **NGMUX**

Table 2-13 **• NGMUX Configuration and Selection Table**

GLMUXCFG[1:0]	GLMUXSEL[1:0]		Selected Input Signal	MUX Type
00	X	0	GLA	2-to-1 GLMUX
	X	1	GLC	
01	X	0	GLA	2-to-1 GLMUX
	X	1	GLINT	

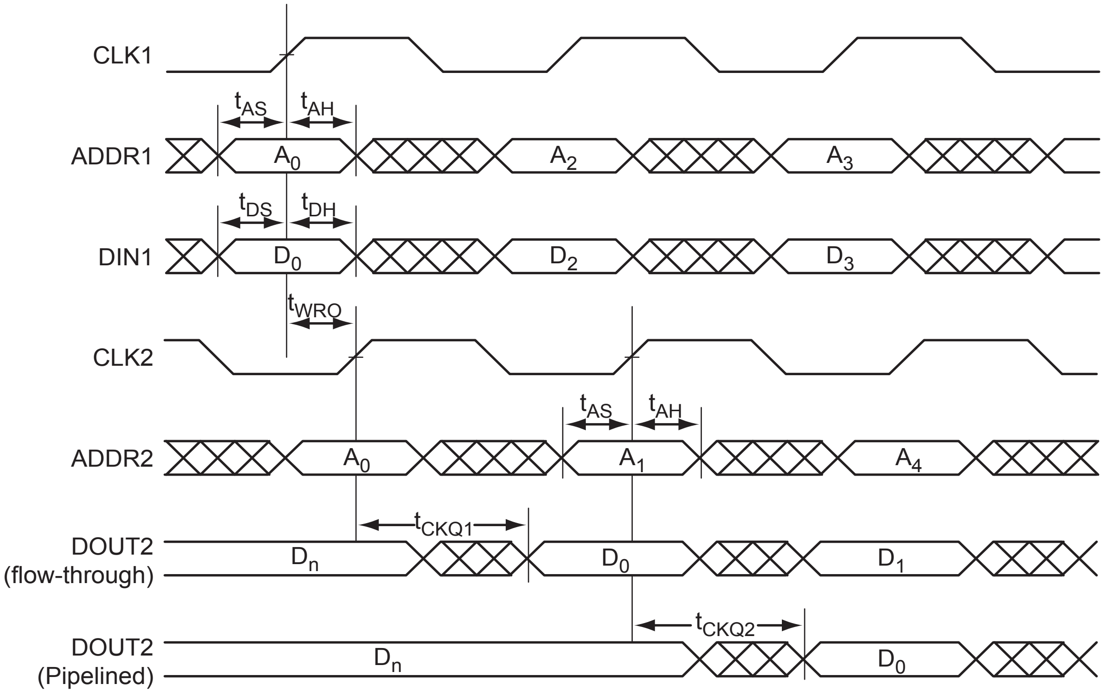


Figure 2-54 **• One Port Write / Other Port Read Same**

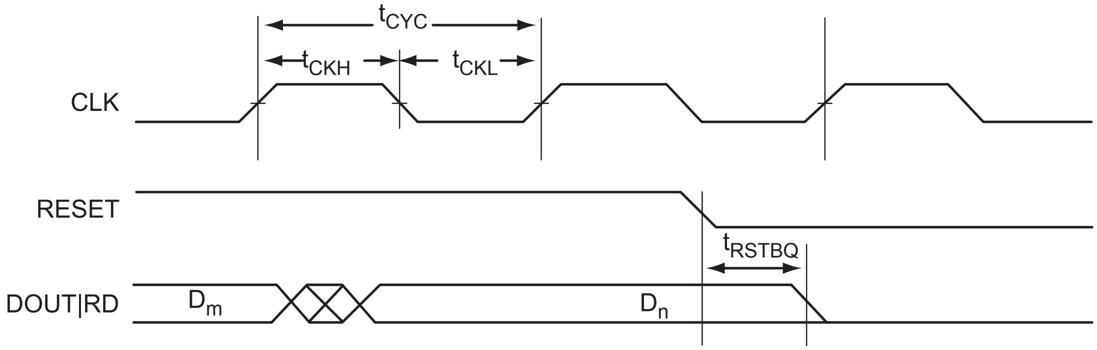


Figure 2-55 **• RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

Temperature Monitor

The final pin in the Analog Quad is the Analog Temperature (AT) pin. The AT pin is used to implement an accurate temperature monitor in conjunction with an external diode-connected bipolar transistor (Figure 2-76). For improved temperature measurement accuracy, it is important to use the ATRTN pin for the return path of the current sourced by the AT pin. Each ATRTN pin is shared between two adjacent Analog Quads. Additionally, if not used for temperature monitoring, the AT pin can provide functionality similar to that of the AV pad. However, in this mode only positive voltages can be applied to the AT pin, and only two prescaler factors are available (16 V and 4 V ranges—refer to Table 2-57 on page 2-130).

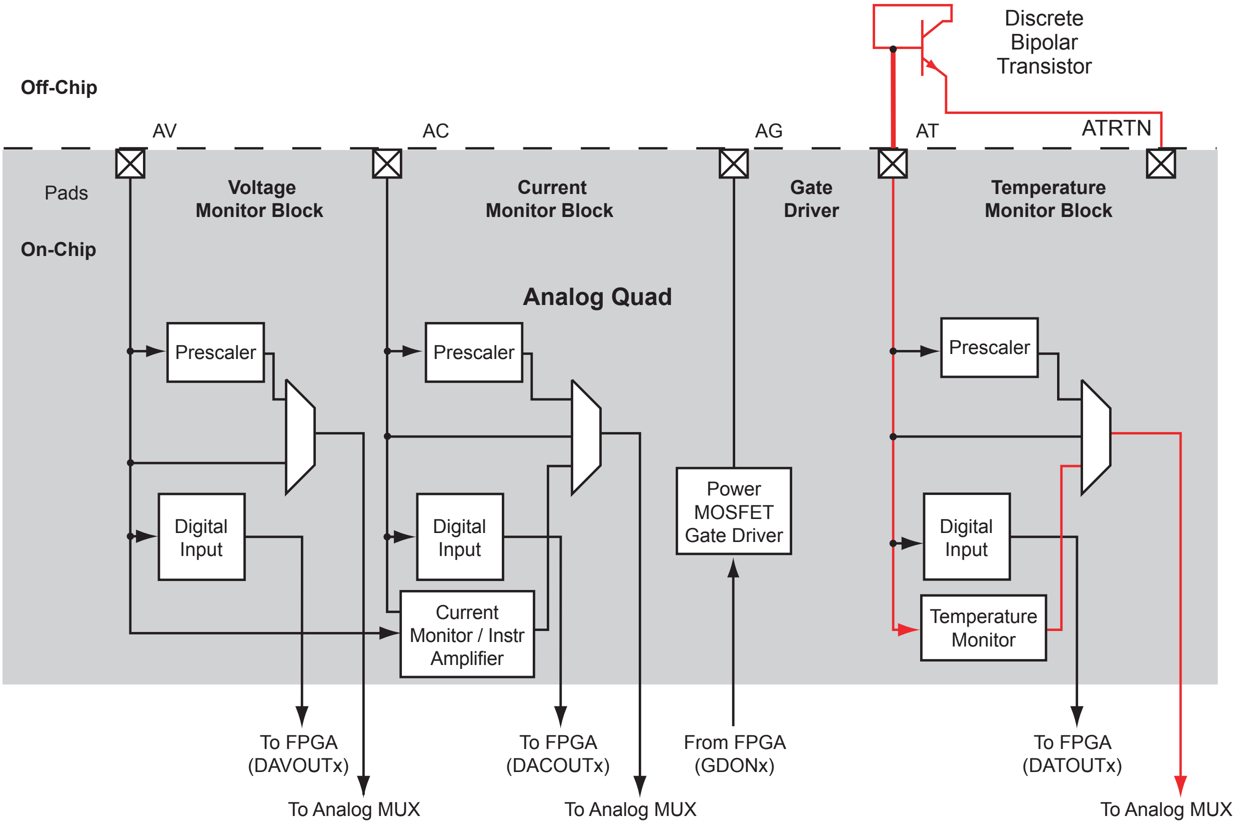
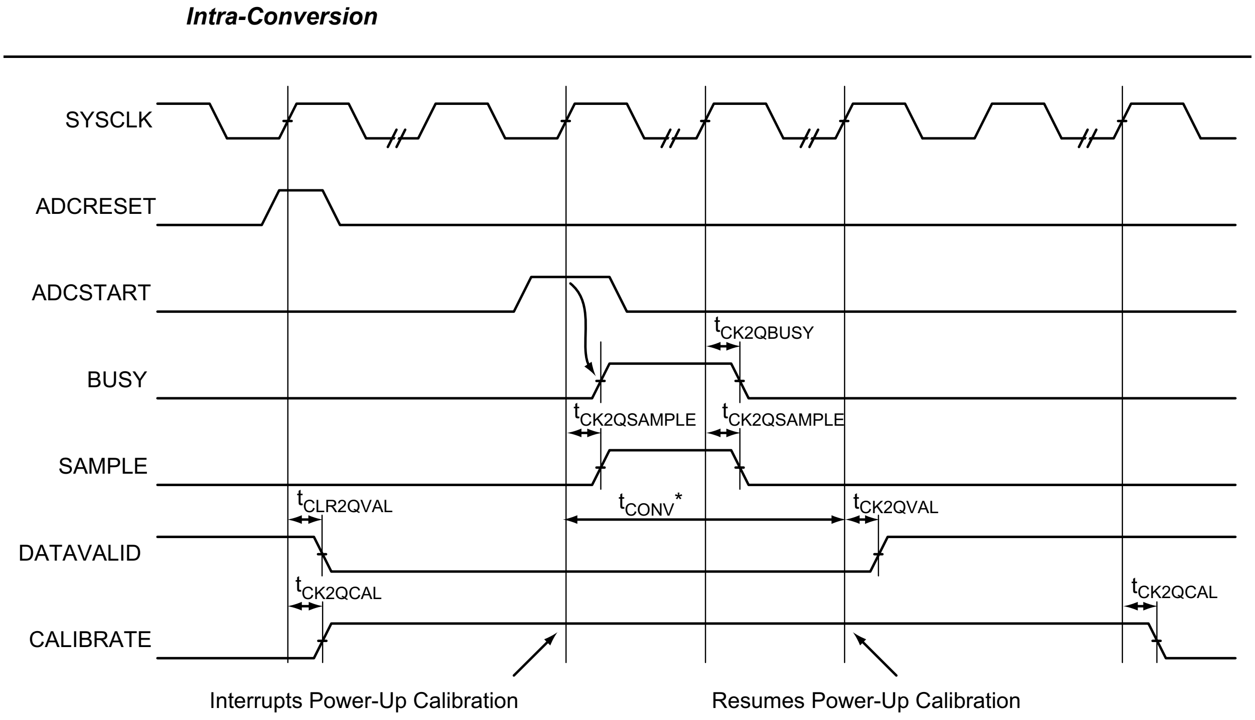
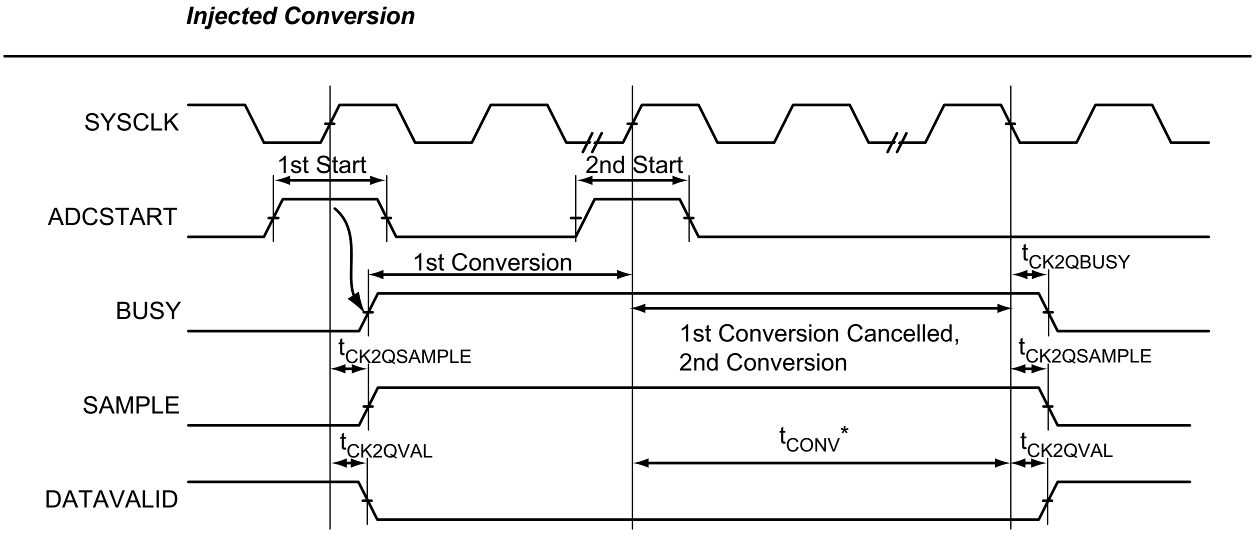


Figure 2-76 • Temperature Monitor Quad



Note: *t_{CONV} represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV}.

Figure 2-92 • Intra-Conversion Timing Diagram



Note: *See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.

Figure 2-93 • Injected Conversion Timing Diagram

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-147 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**μA[4]**	**μA[4]**
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

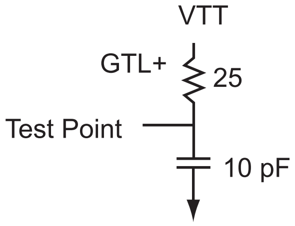


Figure 2-127 • AC Loading

Table 2-148 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-149 • 2.5 V GTL+
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
–1	0.56	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
–2	0.49	1.65	0.03	1.13	0.32	1.68	1.57			3.35	4.34	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-159* • Minimum and Maximum DC Input and Output Levels**

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

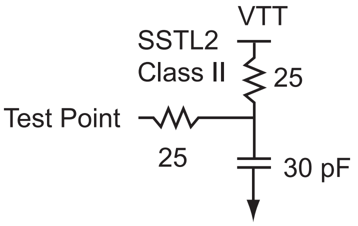


***Figure 2-131* • AC Loading**

***Table 2-160* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

***Table 2-161* • SSTL 2 Class II**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	4.01	ns
–1	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	3.41	ns
–2	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	2.99	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Differential I/O Characteristics

Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-134. The building blocks of the LVDS transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

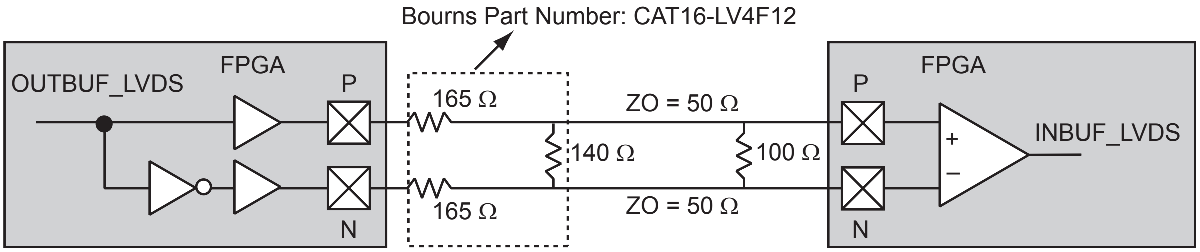


Figure 2-134 • LVDS Circuit Diagram and Board-Level Implementation

Table 2-168 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Input High Voltage	1.25	1.425	1.6	V
IOL [1]	Output Low Voltage	0.65	0.91	1.16	mA
IOH [1]	Output High Voltage	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIL [2,3]	Input Low Voltage			10	µA
IIH [2,4]	Input High Voltage			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

Notes:

1. *IOL/IOH defined by VODIFF/(Resistor Network)*
2. *Currents are measured at 85°C junction temperature.*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings[1] (continued)

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52
Applicable to Standard I/O Banks				
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	431.08
2.5 V LVCMOS	35	2.5	–	247.36
1.8 V LVCMOS	35	1.8	–	128.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	89.46

Notes:

1. *Dynamic power consumption is given for standard load and software-default drive strength and output slew.*
2. *PDC8 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*

Methodology

Total Power Consumption—P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Operating Mode

$P_{STAT} = PDC1 + (N_{NVM\text{-}BLOCKS} * PDC4) + PDC5 + (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLS} * PDC9)$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = PDC2$

Sleep Mode

$P_{STAT} = PDC3$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

Sleep Mode

$P_{DYN} = 0$ W

Global Clock Dynamic Contribution—P_{CLOCK}

Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Sleep Mode

$P_{CLOCK} = 0$ W

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

Operating Mode

$P_{S\text{-}CELL} = 0\ W$

$P_{C\text{-}CELL} = 0\ W$

$P_{NET} = 0\ W$

$P_{LOGIC} = 0\ W$

I/O Input and Output Buffer Contribution—$P_{I/O}$

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

$F_{CLK} = 50\ MHz$

Number of input pins used: $N_{INPUTS} = 30$

Number of output pins used: $N_{OUTPUTS} = 40$

Estimated I/O buffer toggle rate: $\alpha_2 = 0.1$ (10%)

Estimated IO buffer enable rate: $\beta_1 = 1$ (100%)

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$

$P_{INPUTS} = 30 * (0.1 / 2) * 0.01739 * 50$

$P_{INPUTS} = 1.30\ mW$

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$

$P_{OUTPUTS} = 40 * (0.1 / 2) * 1 * 0.4747 * 50$

$P_{OUTPUTS} = 47.47\ mW$

$P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$

$P_{I/O} = 1.30\ mW + 47.47\ mW$

$P_{I/O} = 48.77\ mW$

Standby Mode and Sleep Mode

$P_{INPUTS} = 0\ W$

$P_{OUTPUTS} = 0\ W$

$P_{I/O} = 0\ W$

RAM Contribution—P_{MEMORY}

Frequency of Read Clock: $F_{READ\text{-}CLOCK} = 10\ MHz$

Frequency of Write Clock: $F_{WRITE\text{-}CLOCK} = 10\ MHz$

Number of RAM blocks: $N_{BLOCKS} = 20$

Estimated RAM Read Enable Rate: $\beta_2 = 0.125$ (12.5%)

Estimated RAM Write Enable Rate: $\beta_3 = 0.125$ (12.5%)

Operating Mode

$P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE\text{-}CLOCK})$

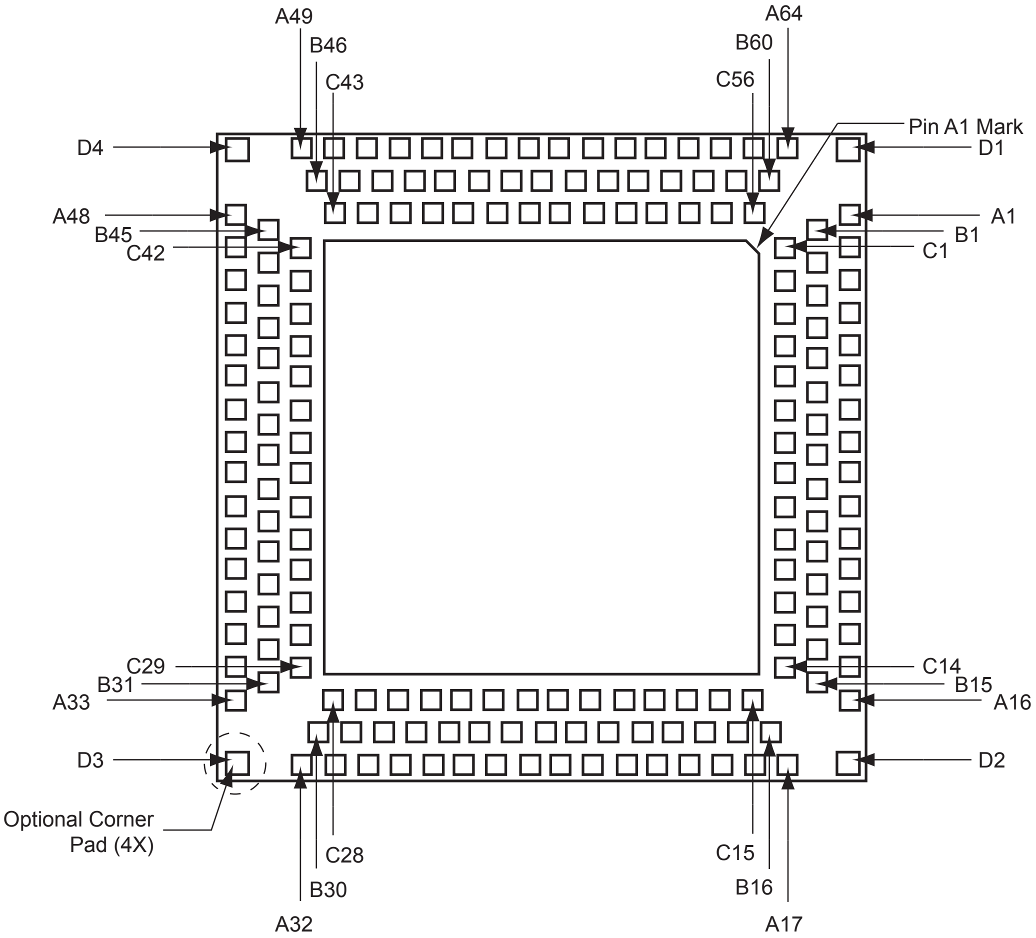
$P_{MEMORY} = (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10)$

$P_{MEMORY} = 1.38\ mW$

Standby Mode and Sleep Mode

$P_{MEMORY} = 0\ W$

QN180



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

FG484		
Pin Number	**AFS600 Function**	**AFS1500 Function**
V3	VCCIB4	VCCIB4
V4	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
V5	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
V6	GND	GND
V7	VCC33PMP	VCC33PMP
V8	NC	NC
V9	VCC33A	VCC33A
V10	AG4	AG4
V11	AT4	AT4
V12	ATRTN2	ATRTN2
V13	AT5	AT5
V14	VCC33A	VCC33A
V15	NC	NC
V16	VCC33A	VCC33A
V17	GND	GND
V18	TMS	TMS
V19	VJTAG	VJTAG
V20	VCCIB2	VCCIB2
V21	TRST	TRST
V22	TDO	TDO
W1	NC	IO93PDB4V0
W2	GND	GND
W3	NC	IO93NDB4V0
W4	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
W5	IO59NDB4V0	IO86NDB4V0
W6	AV0	AV0
W7	GNDA	GNDA
W8	AV1	AV1
W9	AV2	AV2
W10	GNDA	GNDA
W11	AV3	AV3
W12	AV6	AV6
W13	GNDA	GNDA
W14	AV7	AV7
W15	AV8	AV8

FG484		
Pin Number	**AFS600 Function**	**AFS1500 Function**
W16	GNDA	GNDA
W17	AV9	AV9
W18	VCCIB2	VCCIB2
W19	NC	IO68PPB2V0
W20	TCK	TCK
W21	GND	GND
W22	NC	IO76PPB2V0
Y1	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
Y2	IO60NDB4V0	IO87NDB4V0
Y3	GEA2/IO58PDB4V0	GEA2/IO85PDB4V0
Y4	IO58NDB4V0	IO85NDB4V0
Y5	NCAP	NCAP
Y6	AC0	AC0
Y7	VCC33A	VCC33A
Y8	AC1	AC1
Y9	AC2	AC2
Y10	VCC33A	VCC33A
Y11	AC3	AC3
Y12	AC6	AC6
Y13	VCC33A	VCC33A
Y14	AC7	AC7
Y15	AC8	AC8
Y16	VCC33A	VCC33A
Y17	AC9	AC9
Y18	ADCGNDREF	ADCGNDREF
Y19	PTBASE	PTBASE
Y20	GNDNVM	GNDNVM
Y21	VCCNVM	VCCNVM
Y22	VPUMP	VPUMP

FG676	
Pin Number	**AFS1500 Function**
L17	VCCIB2
L18	GCB2/IO60PDB2V0
L19	IO58NDB2V0
L20	IO57NDB2V0
L21	IO59NDB2V0
L22	GCC2/IO61PDB2V0
L23	IO55PPB2V0
L24	IO56PDB2V0
L25	IO55NPB2V0
L26	GND
M1	NC
M2	VCCIB4
M3	GFC2/IO108PDB4V0
M4	GND
M5	IO109NDB4V0
M6	IO110NDB4V0
M7	GND
M8	IO104NDB4V0
M9	IO111NDB4V0
M10	GND
M11	VCC
M12	GND
M13	VCC
M14	GND
M15	VCC
M16	GND
M17	GND
M18	IO60NDB2V0
M19	IO58PDB2V0
M20	GND
M21	IO68NPB2V0
M22	IO61NDB2V0
M23	GND
M24	IO56NDB2V0
M25	VCCIB2
M26	IO65PDB2V0

FG676	
Pin Number	**AFS1500 Function**
N1	NC
N2	NC
N3	IO108NDB4V0
N4	VCCOSC
N5	VCCIB4
N6	XTAL2
N7	GFC1/IO107PDB4V0
N8	VCCIB4
N9	GFB1/IO106PDB4V0
N10	VCCIB4
N11	GND
N12	VCC
N13	GND
N14	VCC
N15	GND
N16	VCC
N17	VCCIB2
N18	IO70PDB2V0
N19	VCCIB2
N20	IO69PDB2V0
N21	GCA1/IO64PDB2V0
N22	VCCIB2
N23	GCC0/IO62NDB2V0
N24	GCC1/IO62PDB2V0
N25	IO66PDB2V0
N26	IO65NDB2V0
P1	NC
P2	NC
P3	IO103PDB4V0
P4	XTAL1
P5	VCCIB4
P6	GNDOSC
P7	GFC0/IO107NDB4V0
P8	VCCIB4
P9	GFB0/IO106NDB4V0
P10	VCCIB4

FG676	
Pin Number	**AFS1500 Function**
P11	VCC
P12	GND
P13	VCC
P14	GND
P15	VCC
P16	GND
P17	VCCIB2
P18	IO70NDB2V0
P19	VCCIB2
P20	IO69NDB2V0
P21	GCA0/IO64NDB2V0
P22	VCCIB2
P23	GCB0/IO63NDB2V0
P24	GCB1/IO63PDB2V0
P25	IO66NDB2V0
P26	IO67PDB2V0
R1	NC
R2	VCCIB4
R3	IO103NDB4V0
R4	GND
R5	IO101PDB4V0
R6	IO100NPB4V0
R7	GND
R8	IO99PDB4V0
R9	IO97PDB4V0
R10	GND
R11	GND
R12	VCC
R13	GND
R14	VCC
R15	GND
R16	VCC
R17	GND
R18	GDB2/IO83PDB2V0
R19	IO78PDB2V0
R20	GND

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

Revision	Changes	Page
Revision 6 (March 2014)	Note added for the discontinuance of QN108 and QN180 packages to the "Package I/Os: Single-/Double-Ended (Analog)" table and the "Temperature Grade Offerings" table (SAR 55113, PDN 1306).	II and IV
	Updated details about page programming time in the "Program Operation" section (SAR 49291).	2-46
	ADC_START changed to ADCSTART in the "ADC Operation" section (SAR 44104).	2-104
Revision 5 (January 2014)	Calibrated offset values (AFS090, AFS250) of the external temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 51464).	2-117
	Specifications for the internal temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 50870).	2-117
Revision 4 (January 2013)	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43177).	III
	The note in Table 2-12 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42563).	2-28
	Table 2-49 • Analog Channel Specifications was modified to update the uncalibrated offset values (AFS250) of the external and internal temperature monitors (SAR 43134).	2-117
	In Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3), changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 20812).	2-130
	The values for the Speed Grade (-1 and Std.) for FDDRIMAX (Table 2-180 • Input DDR Propagation Delays) and values for the Speed Grade (-2 and Std.) for FDDOMAX (Table 2-182 • Output DDR Propagation Delays) had been inadvertently interchanged. This has been rectified (SAR 38514).	2-220, 2-222
	Added description about what happens if a user connects VAREF to an external 3.3 V on their board to the "VAREF Analog Reference Voltage" section (SAR 35188).	2-225
	Added a note to Table 3-2 • Recommended Operating Conditions1 (SAR 43429): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	3-3
	Added the Package Thermal details for AFS600-PQ208 and AFS250-PQ208 to Table 3-6 • Package Thermal Resistance (SAR 37816). Deleted the Die Size column from the table (SAR 43503).	3-7
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 42495). Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 3 (August 2012)	Microblade U1AFS250 and U1AFS1500 devices were added to the product tables.	I – IV
	A sentence pertaining to the analog I/Os was added to the "Specifying I/O States During Programming" section (SAR 34831).	1-9

Revision	Changes	Page
Revision 3 (continued)	The "RC Oscillator" section was revised to correct a sentence that did not differentiate accuracy for commercial and industrial temperature ranges, which is given in Table 2-9 • Electrical Characteristics of RC Oscillator (SAR 33722).	2-19
	Figure 2-57 • FIFO Read and Figure 2-58 • FIFO Write are new (SAR 34840).	2-72
	The first paragraph of the "Offset" section was removed; it was intended to be replaced by the paragraph following it (SAR 22647).	2-95
	IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions (SAR 39813).	2-164
	The drive strength, IOL, and IOH for 3.3 V GTL and 2.5 V GTL were changed from 25 mA to 20 mA in the following tables (SAR 37373): Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings Table 2-96 • I/O Output Buffer Maximum Resistances 1 Table 2-138 • Minimum and Maximum DC Input and Output Levels Table 2-141 • Minimum and Maximum DC Input and Output Levels	2-164 2-167 2-169 2-199 2-200
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34800): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-181
	Corrected the inadvertent error in maximum values for LVPECL VIH and VIL and revised them to "3.6" in Table 2-171 • Minimum and Maximum DC Input and Output Levels, making these consistent with Table 3-1 • Absolute Maximum Ratings, and Table 3-4 • Overshoot and Undershoot Limits 1 (SAR 37687).	2-211
	The maximum frequency for global clock parameter was removed from Table 2-5 • AFS1500 Global Resource Timing through Table 2-8 • AFS090 Global Resource Timing because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36955).	2-16 to 2-17
Revision 2 (March 2012)	The phrase "without debug" was removed from the "Soft ARM Cortex-M1 Fusion Devices (M1)" section (SAR 21390).	I
	The "In-System Programming (ISP) and Security" section, "Security" section, "Flash Advantages" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34679).	I, 1-2, 2-228
	The Y security option and Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34721).	III
	The "Specifying I/O States During Programming" section is new (SAR 34693).	1-9
	The following information was added before Figure 2-17 • XTLOSC Macro: In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating (SAR 24119).	2-20
	Table 2-12 • Fusion CCC/PLL Specification was updated. A note was added indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34814).	2-28