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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 252 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-2fg676i |

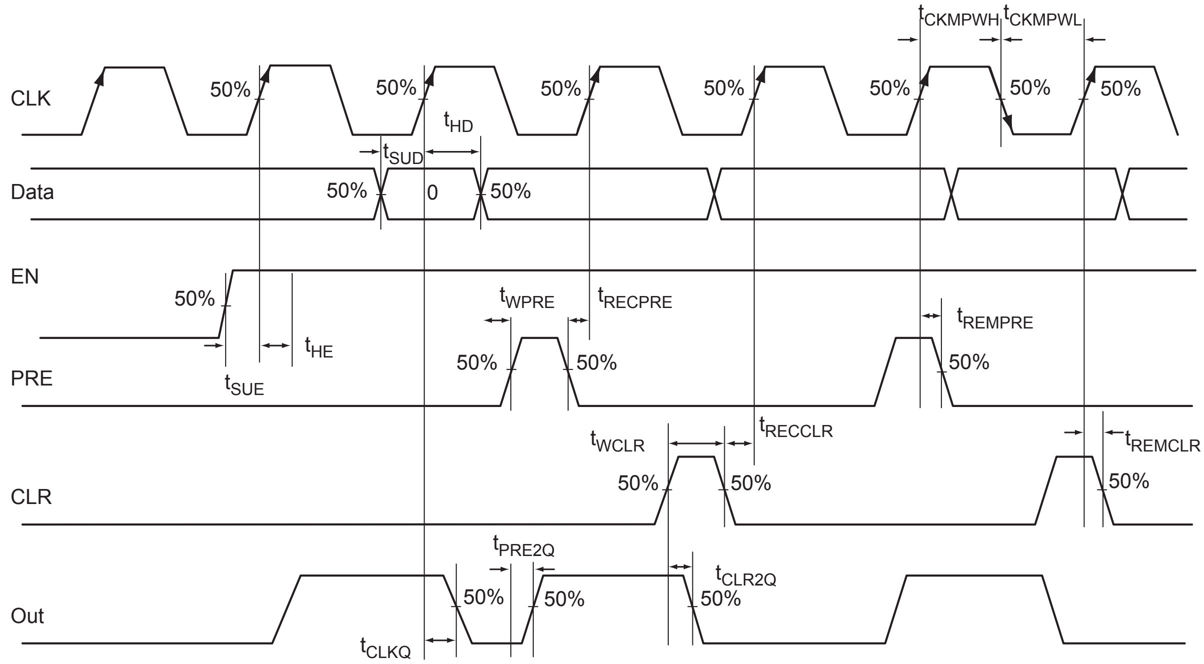



***Figure 2-6 •*** **Sequential Timing Model and Waveforms**

### *Sequential Timing Characteristics*

***Table 2-2 •*** **Register Delays**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.37 | 0.43 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.41 | 0.48 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

## Crystal Oscillator

The Crystal Oscillator (XTLOSC) is source that generates the clock from an external crystal. The output of XTLOSC CLKOUT signal can be selected as an input to the PLL. Refer to the "Clock Conditioning Circuits" section for more details. The XTLOSC can operate in normal operations and Standby mode (RTC is running and 1.5 V is not present).

In normal operation, the internal FPGA_EN signal is '1' as long as 1.5 V is present for VCC. As such, the internal enable signal, XTL_EN, for Crystal Oscillator is enabled since FPGA_EN is asserted. The XTL_MODE has the option of using MODE or RTC_MODE, depending on SELMODE.

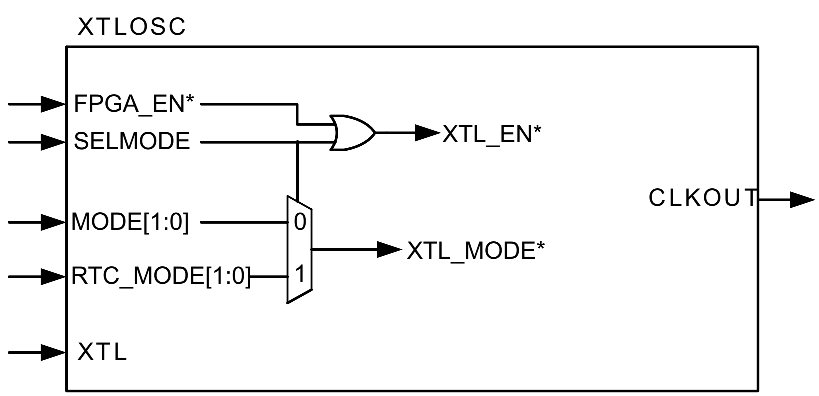
During Standby, 1.5 V is not available, as such, and FPGA_EN is '0'. SELMODE must be asserted in order for XTL_EN to be enabled; hence XTL_MODE relies on RTC_MODE. SELMODE and RTC_MODE must be connected to RTCXTLSEL and RTCXTLMODE from the AB respectively for correct operation during Standby (refer to the "Real-Time Counter System" section on page 2-31 for a detailed description).

The Crystal Oscillator can be configured in one of four modes:

- RC network, 32 KHz to 4 MHz
- Low gain, 32 to 200 KHz
- Medium gain, 0.20 to 2.0 MHz
- High gain, 2.0 to 20.0 MHz

In RC network mode, the XTAL1 pin is connected to an RC circuit, as shown in Figure 2-16 on page 2-18. The XTAL2 pin should be left floating. The RC value can be chosen based on Figure 2-18 for any desired frequency between 32 KHz and 4 MHz. The RC network mode can also accommodate an external clock source on XTAL1 instead of an RC circuit.

In Low gain, Medium gain, and High gain, an external crystal component or ceramic resonator can be added onto XTAL1 and XTAL2, as shown in Figure 2-16 on page 2-18. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.




*Note: *Internal signal—does not exist in macro.*

***Figure 2-17* • XTLOSC Macro**

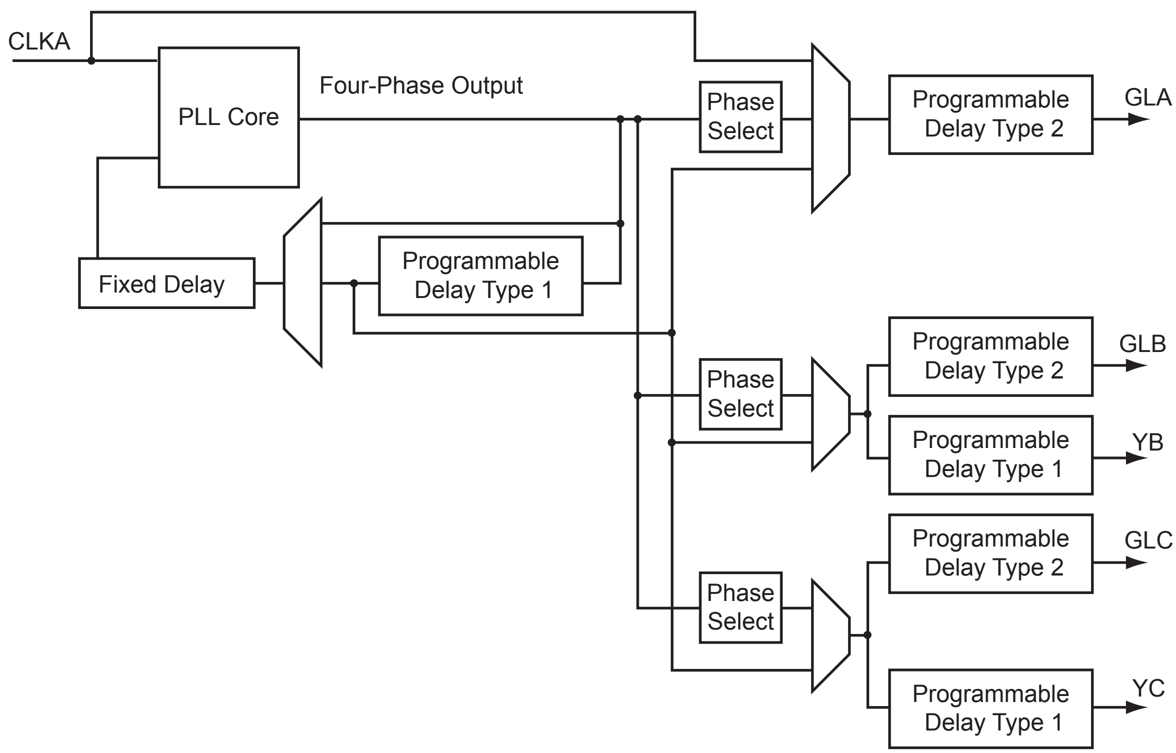
## CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

### CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.




*Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.*

***Figure 2-23* • PLL Block**

Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

### Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-35 on page 2-45 illustrates the multiple Write operations.

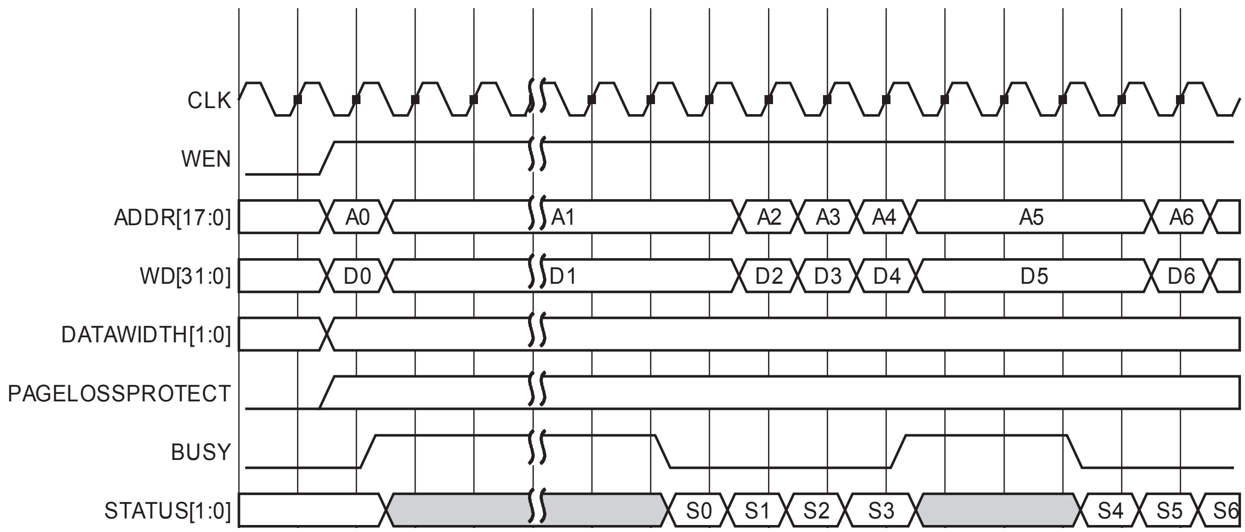



***Figure 2-35 •*** **FB Write Waveform**

When a Write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. A Copy Page operation takes no less than 55 cycles and could take more if a Write or Unprotect Page operation is started while the NVM is busy pre-fetching a block. The basic operation is to read a block from the array into the block register (5 cycles) and then write the block register to the page buffer (1 cycle) and if necessary, when the copy is complete, reading the block being written from the page buffer into the block buffer (1 cycle). A page contains 9 blocks, so 9 blocks multiplied by 6 cycles to read/write each block, plus 1 is 55 cycles total. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates that an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky"; it is unchanged until another operation is started.

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

1. Attempting to write a page that is Overwrite Protected (STATUS = '01'). The write is not performed.
2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = '11'). The write is not performed.

## Timing Characteristics

***Table 2-31* • RAM4K9**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| $t_{BKH}$ | BL hold time | 0.02 | 0.02 | 0.02 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 1.79 | 2.03 | 2.39 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 2.36 | 2.68 | 3.15 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{C2CWWH}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum frequency | 310 | 272 | 231 | MHz |

*Notes:*

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-32 • RAM512X18**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.09 | 0.10 | 0.12 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.06 | 0.07 | 0.08 | ns |
| $t_{DS}$ | Input data (WD) setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (WD) hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on RD (output retained) | 2.16 | 2.46 | 2.89 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on RD (pipelined) | 0.90 | 1.02 | 1.20 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.50 | 0.43 | 0.38 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge | 0.59 | 0.50 | 0.44 | ns |
| $t_{RSTBQ}$[1] | RESET Low to data out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to data out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum frequency | 310 | 272 | 231 | MHz |

*Notes:*

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to* *Table 3-7 on page 3-9**.*

## Analog-to-Digital Converter Block

At the heart of the Fusion analog system is a programmable Successive Approximation Register (SAR) ADC. The ADC can support 8-, 10-, or 12-bit modes of operation. In 12-bit mode, the ADC can resolve 500 ksps. All results are MSB-justified in the ADC. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 2-79. The ADC offers multiple self-calibrating modes to ensure consistent high performance both at power-up and during runtime.

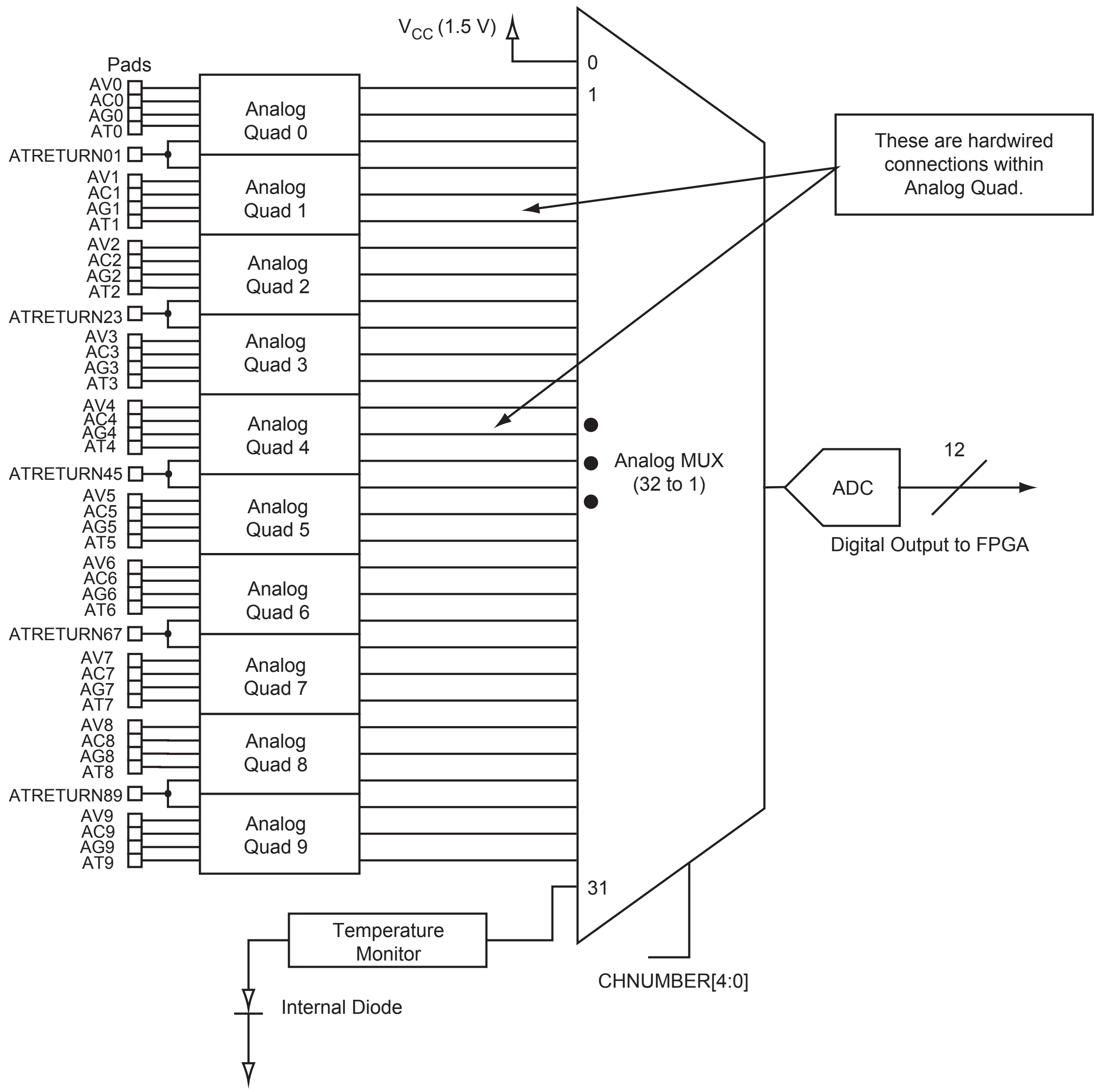



*Figure 2-79* • **ADC Block Diagram**

*Table 2-40* • **Analog MUX Channels (continued)**

| Analog MUX Channel | Signal | Analog Quad Number |
|---|---|---|
| 16 | AV5 | Analog Quad 5 |
| 17 | AC5 | |
| 18 | AT5 | |
| 19 | AV6 | Analog Quad 6 |
| 20 | AC6 | |
| 21 | AT6 | |
| 22 | AV7 | Analog Quad 7 |
| 23 | AC7 | |
| 24 | AT7 | |
| 25 | AV8 | Analog Quad 8 |
| 26 | AC8 | |
| 27 | AT8 | |
| 28 | AV9 | Analog Quad 9 |
| 29 | AC9 | |
| 30 | AT9 | |
| 31 | Internal temperature monitor | |

The ADC can be powered down independently of the FPGA core, as an additional control or for power-saving considerations, via the PWRDWN pin of the Analog Block. The PWRDWN pin controls only the comparators in the ADC.

### ADC Modes

The Fusion ADC can be configured to operate in 8-, 10-, or 12-bit modes, power-down after conversion, and dynamic calibration. This is controlled by MODE[3:0], as defined in Table 2-41 on page 2-106.

The output of the ADC is the RESULT[11:0] signal. In 8-bit mode, the Most Significant 8 Bits RESULT[11:4] are used as the ADC value and the Least Significant 4 Bits RESULT[3:0] are logical '0's. In 10-bit mode, RESULT[11:2] are used the ADC value and RESULT[1:0] are logical 0s.

*Table 2-41* • **Mode Bits Function**

| Name | Bits | Function |
|---|---|---|
| MODE | 3 | 0 – Internal calibration after every conversion; two ADCCLK cycles are used after the conversion.<br>1 – No calibration after every conversion |
| MODE | 2 | 0 – Power-down after conversion<br>1 – No Power-down after conversion |
| MODE | 1:0 | 00 – 10-bit<br>01 – 12-bit<br>10 – 8-bit<br>11 – Unused |

Refer to Table 2-46 on page 2-109 and the "Acquisition Time or Sample Time Control" section on page 2-107

$$t_{sample} = (2 + STC) \times t_{ADCCLK}$$

*EQ 20*

STC: Sample Time Control value (0–255)

$t_{SAMPLE}$ is the sample time

***Table 2-46*** **• STC Bits Function**

| Name | Bits | Function |
|---|---|---|
| STC | [7:0] | Sample time control |

Sample time is computed based on the period of ADCCLK.

### Distribution Phase

The second phase is called the distribution phase. During distribution phase, the ADC computes the equivalent digital value from the value stored in the input capacitor. In this phase, the output signal SAMPLE goes back to '0', indicating the sample is completed; but the BUSY signal remains '1', indicating the ADC is still busy for distribution. The distribution time depends strictly on the number of bits. If the ADC is configured as a 10-bit ADC, then 10 ADCCLK cycles are needed. EQ 8 describes the distribution time.

$$t_{distrib} = N \times t_{ADCCLK}$$

*EQ 21*

N: Number of bits

### Post-Calibration Phase

The last phase is the post-calibration phase. This is an optional phase. The post-calibration phase takes two ADCCLK cycles. The output BUSY signal will remain '1' until the post-calibration phase is completed. If the post-calibration phase is skipped, then the BUSY signal goes to '0' after distribution phase. As soon as BUSY signal goes to '0', the DATAVALID signal goes to '1', indicating the digital result is available on the RESULT output signals. DATAVAILD will remain '1' until the next ADCSTART is asserted. Microsemi recommends enabling post-calibration to compensate for drift and temperature-dependent effects. This ensures that the ADC remains consistent over time and with temperature. The post-calibration phase is enabled by bit 3 of the Mode register. EQ 9 describes the post-calibration time.

$$t_{post\text{-}cal} = MODE[3] \times (2 \times t_{ADCCLK})$$

*EQ 22*

MODE[3]: Bit 3 of the Mode register, described in Table 2-41 on page 2-106.

The calculation for the conversion time for the ADC is summarized in EQ 23.

$$t_{conv} = t_{sync\_read} + t_{sample} + t_{distrib} + t_{post\text{-}cal} + t_{sync\_write}$$

*EQ 23*

$t_{conv}$: conversion time

$t_{sync\_read}$: maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, $t_{SYSCLK}$.

$t_{sample}$: Sample time

$t_{distrib}$: Distribution time

$t_{post\text{-}cal}$: Post-calibration time

$t_{sync\_write}$: Maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, $t_{SYSCLK}$.

## Analog System Characteristics

***Table 2-49* • Analog Channel Specifications**
**Commercial Temperature Range Conditions, $T_J$ = 85°C (unless noted otherwise),**
**Typical: VCC33A = 3.3 V, VCC = 1.5 V**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Voltage Monitor Using Analog Pads AV, AC and AT (using prescaler)** | | | | | | |
| | Input Voltage (Prescaler) | Refer to Table 3-2 on page 3-3 | | | | |
| VINAP | Uncalibrated Gain and Offset Errors | Refer to Table 2-51 on page 2-122 | | | | |
| | Calibrated Gain and Offset Errors | Refer to Table 2-52 on page 2-123 | | | | |
| | Bandwidth1 | | | | 100 | KHz |
| | Input Resistance | Refer to Table 3-3 on page 3-4 | | | | |
| | Scaling Factor | Prescaler modes (Table 2-57 on page 2-130) | | | | |
| | Sample Time | | 10 | | | µs |
| **Current Monitor Using Analog Pads AV and AC** | | | | | | |
| VRSM[1] | Maximum Differential Input Voltage | | | | VAREF / 10 | mV |
| | Resolution | Refer to "Current Monitor" section | | | | |
| | Common Mode Range | | | | – 10.5 to +12 | V |
| CMRR | Common Mode Rejection Ratio | DC – 1 KHz | | 60 | | dB |
| | | 1 KHz - 10 KHz | | 50 | | dB |
| | | > 10 KHz | | 30 | | dB |
| $t_{CMSHI}$ | Strobe High time | | ADC conv. time | | 200 | µs |
| $t_{CMSHI}$ | Strobe Low time | | 5 | | | µs |
| $t_{CMSHI}$ | Settling time | | 0.02 | | | µs |
| | Accuracy | Input differential voltage > 50 mV | | | –2 –(0.05 x VRSM) to +2 + (0.05 x VRSM) | mV |

*Notes:*

1. *VRSM is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.*
3. *VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User Guide.

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 kΩ (or lower) output drive resistance at hot insertion, and 1 kΩ (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

1. Grounds
2. Powers, I/Os, other pins

## Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks and standard I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If Standard I/O banks are used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the standard I/O buffers do not have built-in I/O clamp diodes.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull down resistor and driven in the opposite direction. A small static current is induced on each IO pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Please refer to Table 2-95 on page 2-169, Table 2-96 on page 2-169, and Table 2-97 on page 2-171 for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTL 3.3 V, pull-up resistor is ~45 kΩ and the resulting current is equal to 3.3 V / 45 kΩ = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven low
- Input buffers with pull-down, driven high
- Bidirectional buffers with pull-up, driven low
- Bidirectional buffers with pull-down, driven high
- Output buffers with pull-up, driven low
- Output buffers with pull-down, driven high
- Tristate buffers with pull-up, driven low
- Tristate buffers with pull-down, driven high

## Electrostatic Discharge (ESD) Protection

Fusion devices are tested per JEDEC Standard JESD22-A114-B.

Fusion devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to VCCI. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the Off state, except when transient voltage is significantly above VCCI or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 2-75 and Table 2-76 on page 2-143 for more information about I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

***Table 2-75*** **• Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities**

| I/O Assignment | Clamp Diode | | Hot Insertion | | 5 V Input Tolerance [1] | | Input Buffer | Output Buffer |
|---|---|---|---|---|---|---|---|---|
| | Standard I/O | Advanced I/O | Standard I/O | Advanced I/O | Standard I/O | Advanced I/O | | |
| 3.3 V LVTTL/LVCMOS | No | Yes | Yes | No | Yes[1] | Yes[1] | Enabled/Disabled | |
| 3.3 V PCI, 3.3 V PCI-X | N/A | Yes | N/A | No | N/A | Yes[1] | Enabled/Disabled | |
| LVCMOS 2.5 V | No | Yes | Yes | No | No | No | Enabled/Disabled | |
| LVCMOS 2.5 V / 5.0 V | N/A | Yes | N/A | No | N/A | Yes[2] | Enabled/Disabled | |
| LVCMOS 1.8 V | No | Yes | Yes | No | No | No | Enabled/Disabled | |
| LVCMOS 1.5 V | No | Yes | Yes | No | No | No | Enabled/Disabled | |
| Differential, LVDS/BLVDS/M-LVDS/ LVPECL [3] | N/A | Yes | N/A | No | N/A | No | Enabled/Disabled | |

*Notes:*

1. *Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.*
2. *Can be implemented with an external resistor and an internal clamp diode.*
3. *Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.*

***Table 2-76*** **• Fusion Pro I/O – Hot-Swap and 5 V Input Tolerance Capabilities**

| I/O Assignment | Clamp Diode | Hot Insertion | 5 V Input Tolerance | Input Buffer | Output Buffer |
|---|---|---|---|---|---|
| 3.3 V LVTTL/LVCMOS | No | Yes | Yes[1] | Enabled/Disabled | |
| 3.3 V PCI, 3.3 V PCI-X | Yes | No | Yes[1] | Enabled/Disabled | |
| LVCMOS 2.5 V [3] | No | Yes | No | Enabled/Disabled | |
| LVCMOS 2.5 V / 5.0 V [3] | Yes | No | Yes[2] | Enabled/Disabled | |
| LVCMOS 1.8 V | No | Yes | No | Enabled/Disabled | |
| LVCMOS 1.5 V | No | Yes | No | Enabled/Disabled | |
| Voltage-Referenced Input Buffer | No | Yes | No | Enabled/Disabled | |
| Differential, LVDS/BLVDS/M-LVDS/LVPECL[4] | No | Yes | No | Enabled/Disabled | |

*Notes:*

1. *Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.*
2. *Can be implemented with an external resistor and an internal clamp diode.*
3. *In the SmartGen, FlashROM, Flash Memory System Builder, and Analog System Builder User Guide, select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V I/O standard.*
4. *Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.*

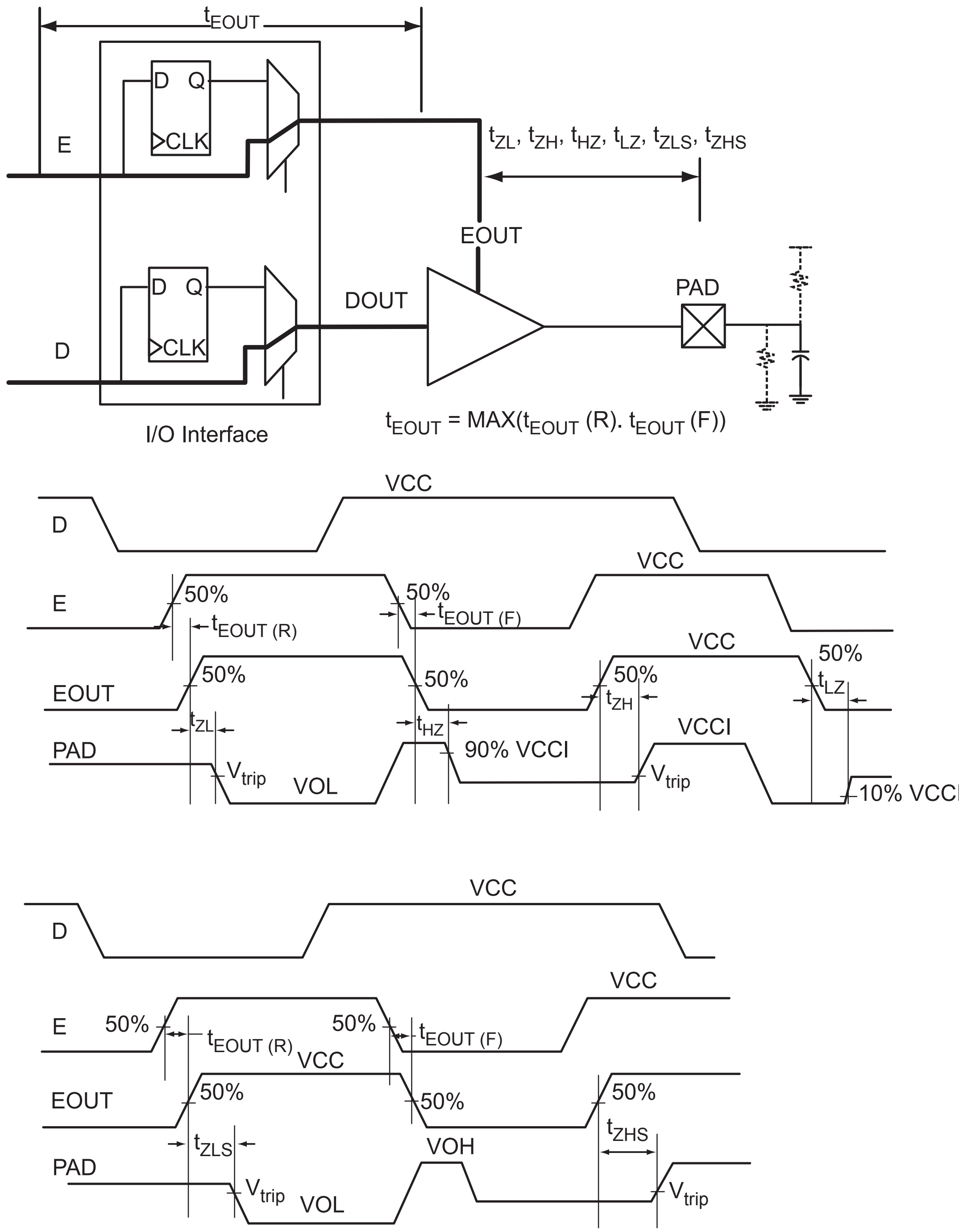



*Figure 2-118* • **Tristate Output Buffer Timing Model and Delays (example)**

***Table 2-98* • I/O Short Currents IOSH/IOSL**

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|---|---|---|---|
| **Applicable to Pro I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 4 mA | 25 | 27 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 2.5 V LVCMOS | 4 mA | 16 | 18 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |
| **Applicable to Advanced I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |

*Note:* *$T_J$ = 100°C

### 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

**Table 2-110 • Minimum and Maximum DC Input and Output Levels**

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | μA[4] | μA[4] |
| **Applicable to Pro I/O Banks** | | | | | | | | | | | | |
| 4 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 8 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |
| 16 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 10 | 10 |
| 24 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 10 | 10 |
| **Applicable to Advanced I/O Banks** | | | | | | | | | | | | |
| 2 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 10 | 10 |
| 4 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 6 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 10 | 10 |
| 8 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |
| 16 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 10 | 10 |
| 24 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 10 | 10 |
| **Applicable to Standard I/O Banks** | | | | | | | | | | | | |
| 2 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 10 | 10 |
| 4 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 6 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 10 | 10 |
| 8 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

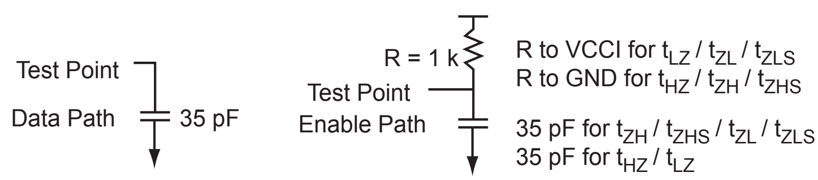



**Figure 2-120 • AC Loading**

**Table 2-111 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 2.5 | 1.2 | – | 35 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

## Input Register

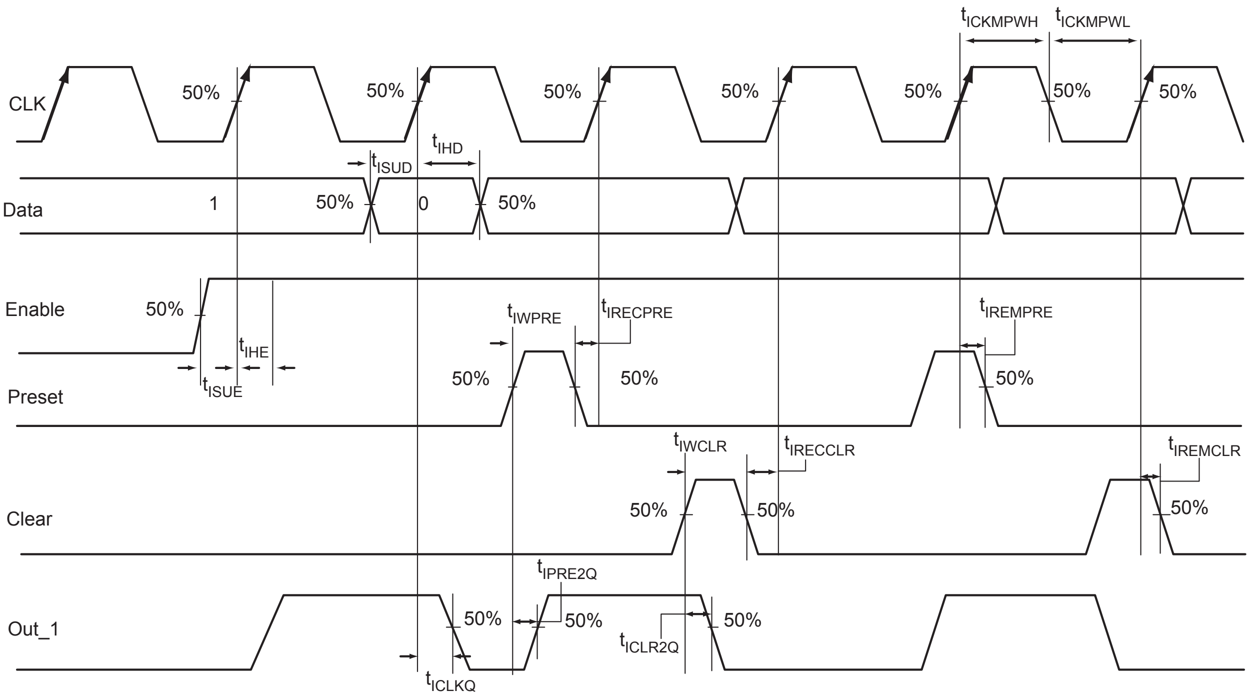



***Figure 2-139*** **• Input Register Timing Diagram**

### *Timing Characteristics*

***Table 2-176*** **• Input Data Register Propagation Delays**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.24 | 0.27 | 0.32 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.26 | 0.30 | 0.35 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 0.37 | 0.42 | 0.50 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.32 | 0.37 | 0.43 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### Theta-JA

Junction-to-ambient thermal resistance ($\theta_{JA}$) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

*EQ 4*

where

$\theta_{JA}$ = 19.00°C/W (taken from Table 3-6 on page 3-7).

$T_A$ = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{19.00°C/W} = 1.3\text{ W}$$

*EQ 5*

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

### Theta-JB

Junction-to-board thermal resistance ($\theta_{JB}$) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

### Theta-JC

Junction-to-case thermal resistance ($\theta_{JC}$) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

### Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent $T_a$ and $T_j$ are given as follows:

$T_J$ = 100.00°C

$T_A$ = 70.00°C

From the datasheet:

$\theta_{JA}$ = 17.00°C/W

$\theta_{JC}$ = 8.28°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\text{ W}} = 1.76\text{ W}$$

*EQ 6*

**Table 3-8 • AFS1500 Quiescent Supply Current Characteristics (continued)**

| Parameter | Description | Conditions | Temp. | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| IJTAG | JTAG I/O quiescent current | Operational standby[4], VJTAG = 3.63 V | $T_J$ = 25°C | | 80 | 100 | µA |
| | | | $T_J$ = 85°C | | 80 | 100 | µA |
| | | | $T_J$ = 100°C | | 80 | 100 | µA |
| | | Standby mode[5] or Sleep mode[6], VJTAG = 0 V | | | 0 | 0 | µA |
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | $T_J$ = 25°C | | 39 | 80 | µA |
| | | | $T_J$ = 85°C | | 40 | 80 | µA |
| | | | $T_J$ = 100°C | | 40 | 80 | µA |
| | | Standby mode[5] or Sleep mode[6], VPUMP = 0 V | | | 0 | 0 | µA |
| ICCNVM | Embedded NVM current | Reset asserted, $V_{CCNVM}$ = 1.575 V | $T_J$ = 25°C | | 50 | 150 | µA |
| | | | $T_J$ =85°C | | 50 | 150 | µA |
| | | | $T_J$ = 100°C | | 50 | 150 | µA |
| ICCPLL | 1.5 V PLL quiescent current | Operational standby , VCCPLL = 1.575 V | $T_J$ = 25°C | | 130 | 200 | µA |
| | | | $T_J$ = 85°C | | 130 | 200 | µA |
| | | | $T_J$ = 100°C | | 130 | 200 | µA |

*Notes:*

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

***Table 3-11*** **• AFS090 Quiescent Supply Current Characteristics**

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ICC[1] | 1.5 V quiescent current | Operational standby[4], VCC = 1.575 V | $T_J$ = 25°C | | 5 | 7.5 | mA |
| | | | $T_J$ = 85°C | | 6.5 | 20 | mA |
| | | | $T_J$ = 100°C | | 14 | 48 | mA |
| | | Standby mode[5] or Sleep mode[6], $V_{CC}$ = 0 V | | | 0 | 0 | µA |
| ICC33[2] | 3.3 V analog supplies current | Operational standby[4], VCC33 = 3.63 V | $T_J$ = 25°C | | 9.8 | 12 | mA |
| | | | $T_J$ = 85°C | | 9.8 | 12 | mA |
| | | | $T_J$ = 100°C | | 10.7 | 15 | mA |
| | | Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V | $T_J$ = 25°C | | 0.30 | 2 | mA |
| | | | $T_J$ = 85°C | | 0.30 | 2 | mA |
| | | | $T_J$ = 100°C | | 0.45 | 2 | mA |
| | | Standby mode[5], VCC33 = 3.63 V | $T_J$ = 25°C | | 2.9 | 2.9 | mA |
| | | | $T_J$ = 85°C | | 2.9 | 3.0 | mA |
| | | | $T_J$ = 100°C | | 3.5 | 6 | mA |
| | | Sleep mode[6], VCC33 = 3.63 V | $T_J$ = 25°C | | 17 | 18 | µA |
| | | | $T_J$ = 85°C | | 18 | 20 | µA |
| | | | $T_J$ = 100°C | | 24 | 25 | µA |
| ICCI[3] | I/O quiescent current | Operational standby[6], VCCIx = 3.63 V | $T_J$ = 25°C | | 260 | 437 | µA |
| | | | $T_J$ = 85°C | | 260 | 437 | µA |
| | | | $T_J$ = 100°C | | 260 | 437 | µA |
| IJTAG | JTAG I/O quiescent current | Operational standby[4], VJTAG = 3.63 V | $T_J$ = 25°C | | 80 | 100 | µA |
| | | | $T_J$ = 85°C | | 80 | 100 | µA |
| | | | $T_J$ = 100°C | | 80 | 100 | µA |
| | | Standby mode[5] or Sleep mode[6], VJTAG = 0 V | | | 0 | 0 | µA |
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | $T_J$ = 25°C | | 37 | 80 | µA |
| | | | $T_J$ = 85°C | | 37 | 80 | µA |
| | | | $T_J$ = 100°C | | 80 | 100 | µA |
| | | Standby mode[5] or Sleep mode[6], VPUMP = 0 V | | | 0 | 0 | µA |

*Notes:*

1. *ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, and ICCI2.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

| FG256 | | | | |
|---|---|---|---|---|
| **Pin Number** | **AFS090 Function** | **AFS250 Function** | **AFS600 Function** | **AFS1500 Function** |
| A1 | GND | GND | GND | GND |
| A2 | VCCIB0 | VCCIB0 | VCCIB0 | VCCIB0 |
| A3 | GAB0/IO02RSB0V0 | GAA0/IO00RSB0V0 | GAA0/IO01NDB0V0 | GAA0/IO01NDB0V0 |
| A4 | GAB1/IO03RSB0V0 | GAA1/IO01RSB0V0 | GAA1/IO01PDB0V0 | GAA1/IO01PDB0V0 |
| A5 | GND | GND | GND | GND |
| A6 | IO07RSB0V0 | IO11RSB0V0 | IO10PDB0V1 | IO07PDB0V1 |
| A7 | IO10RSB0V0 | IO14RSB0V0 | IO12PDB0V1 | IO13PDB0V2 |
| A8 | IO11RSB0V0 | IO15RSB0V0 | IO12NDB0V1 | IO13NDB0V2 |
| A9 | IO16RSB0V0 | IO24RSB0V0 | IO22NDB1V0 | IO24NDB1V0 |
| A10 | IO17RSB0V0 | IO25RSB0V0 | IO22PDB1V0 | IO24PDB1V0 |
| A11 | IO18RSB0V0 | IO26RSB0V0 | IO24NDB1V1 | IO29NDB1V1 |
| A12 | GND | GND | GND | GND |
| A13 | GBC0/IO25RSB0V0 | GBA0/IO38RSB0V0 | GBA0/IO28NDB1V1 | GBA0/IO42NDB1V2 |
| A14 | GBA0/IO29RSB0V0 | IO32RSB0V0 | IO29NDB1V1 | IO43NDB1V2 |
| A15 | VCCIB0 | VCCIB0 | VCCIB1 | VCCIB1 |
| A16 | GND | GND | GND | GND |
| B1 | VCOMPLA | VCOMPLA | VCOMPLA | VCOMPLA |
| B2 | VCCPLA | VCCPLA | VCCPLA | VCCPLA |
| B3 | GAA0/IO00RSB0V0 | IO07RSB0V0 | IO00NDB0V0 | IO00NDB0V0 |
| B4 | GAA1/IO01RSB0V0 | IO06RSB0V0 | IO00PDB0V0 | IO00PDB0V0 |
| B5 | NC | GAB1/IO03RSB0V0 | GAB1/IO02PPB0V0 | GAB1/IO02PPB0V0 |
| B6 | IO06RSB0V0 | IO10RSB0V0 | IO10NDB0V1 | IO07NDB0V1 |
| B7 | VCCIB0 | VCCIB0 | VCCIB0 | VCCIB0 |
| B8 | IO12RSB0V0 | IO16RSB0V0 | IO18NDB1V0 | IO22NDB1V0 |
| B9 | IO13RSB0V0 | IO17RSB0V0 | IO18PDB1V0 | IO22PDB1V0 |
| B10 | VCCIB0 | VCCIB0 | VCCIB1 | VCCIB1 |
| B11 | IO19RSB0V0 | IO27RSB0V0 | IO24PDB1V1 | IO29PDB1V1 |
| B12 | GBB0/IO27RSB0V0 | GBC0/IO34RSB0V0 | GBC0/IO26NPB1V1 | GBC0/IO40NPB1V2 |
| B13 | GBC1/IO26RSB0V0 | GBA1/IO39RSB0V0 | GBA1/IO28PDB1V1 | GBA1/IO42PDB1V2 |
| B14 | GBA1/IO30RSB0V0 | IO33RSB0V0 | IO29PDB1V1 | IO43PDB1V2 |
| B15 | NC | NC | VCCPLB | VCCPLB |
| B16 | NC | NC | VCOMPLB | VCOMPLB |
| C1 | VCCIB3 | V**CCI**B3 | VCCIB4 | VCCIB4 |
| C2 | GND | GND | GND | GND |
| C3 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| C4 | NC | NC | VCCIB0 | VCCIB0 |
| C5 | VCCIB0 | VCCIB0 | VCCIB0 | VCCIB0 |
| C6 | GAC1/IO05RSB0V0 | GAC1/IO05RSB0V0 | GAC1/IO03PDB0V0 | GAC1/IO03PDB0V0 |