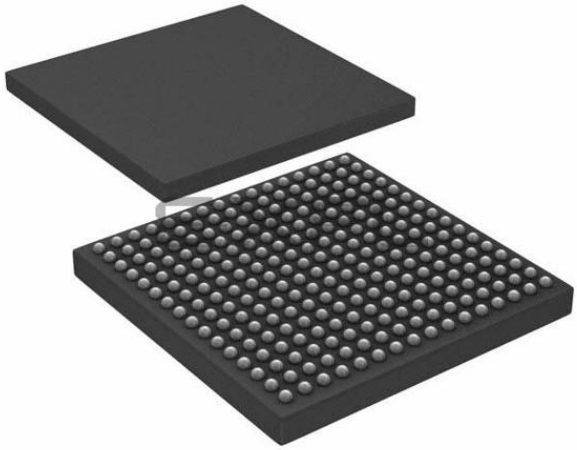

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 119 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-fg256i |

### VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, Table 2-7, and Table 2-8 on page 2-17 present minimum and maximum global clock delays within the device Minimum and maximum delays are measured with minimum and maximum loading, respectively.

#### Timing Characteristics

**Table 2-5 • AFS1500 Global Resource Timing**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.53 | 1.75 | 1.74 | 1.99 | 2.05 | 2.34 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.53 | 1.79 | 1.75 | 2.04 | 2.05 | 2.40 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | | | | | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-6 • AFS600 Global Resource Timing**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.27 | 1.49 | 1.44 | 1.70 | 1.69 | 2.00 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.26 | 1.54 | 1.44 | 1.75 | 1.69 | 2.06 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | | | | | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.27 | | 0.31 | | 0.36 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

## Crystal Oscillator

The Crystal Oscillator (XTLOSC) is source that generates the clock from an external crystal. The output of XTLOSC CLKOUT signal can be selected as an input to the PLL. Refer to the "Clock Conditioning Circuits" section for more details. The XTLOSC can operate in normal operations and Standby mode (RTC is running and 1.5 V is not present).

In normal operation, the internal FPGA_EN signal is '1' as long as 1.5 V is present for VCC. As such, the internal enable signal, XTL_EN, for Crystal Oscillator is enabled since FPGA_EN is asserted. The XTL_MODE has the option of using MODE or RTC_MODE, depending on SELMODE.

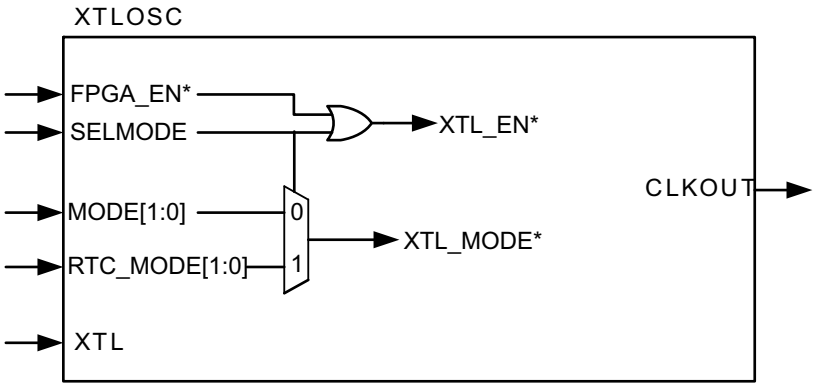
During Standby, 1.5 V is not available, as such, and FPGA_EN is '0'. SELMODE must be asserted in order for XTL_EN to be enabled; hence XTL_MODE relies on RTC_MODE. SELMODE and RTC_MODE must be connected to RTCXTLSEL and RTCXTLMODE from the AB respectively for correct operation during Standby (refer to the "Real-Time Counter System" section on page 2-31 for a detailed description).

The Crystal Oscillator can be configured in one of four modes:

- RC network, 32 KHz to 4 MHz
- Low gain, 32 to 200 KHz
- Medium gain, 0.20 to 2.0 MHz
- High gain, 2.0 to 20.0 MHz

In RC network mode, the XTAL1 pin is connected to an RC circuit, as shown in Figure 2-16 on page 2-18. The XTAL2 pin should be left floating. The RC value can be chosen based on Figure 2-18 for any desired frequency between 32 KHz and 4 MHz. The RC network mode can also accommodate an external clock source on XTAL1 instead of an RC circuit.

In Low gain, Medium gain, and High gain, an external crystal component or ceramic resonator can be added onto XTAL1 and XTAL2, as shown in Figure 2-16 on page 2-18. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.




*Note: *Internal signal—does not exist in macro.*

***Figure 2-17 •*** **XTLOSC Macro**

## Flash Memory Block Characteristics

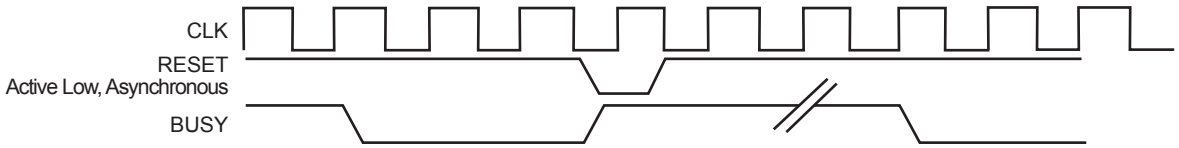



***Figure 2-44 •*** **Reset Timing Diagram**

***Table 2-25 •*** **Flash Memory Block Timing**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{CLK2RD}$ | Clock-to-Q in 5-cycle read mode of the Read Data | 7.99 | 9.10 | 10.70 | ns |
| | Clock-to-Q in 6-cycle read mode of the Read Data | 5.03 | 5.73 | 6.74 | ns |
| $t_{CLK2BUSY}$ | Clock-to-Q in 5-cycle read mode of BUSY | 4.95 | 5.63 | 6.62 | ns |
| | Clock-to-Q in 6-cycle read mode of BUSY | 4.45 | 5.07 | 5.96 | ns |
| $t_{CLK2STATUS}$ | Clock-to-Status in 5-cycle read mode | 11.24 | 12.81 | 15.06 | ns |
| | Clock-to-Status in 6-cycle read mode | 4.48 | 5.10 | 6.00 | ns |
| $t_{DSUNVM}$ | Data Input Setup time for the Control Logic | 1.92 | 2.19 | 2.57 | ns |
| $t_{DHNVM}$ | Data Input Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{ASUNVM}$ | Address Input Setup time for the Control Logic | 2.76 | 3.14 | 3.69 | ns |
| $t_{AHNVM}$ | Address Input Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUDWNVM}$ | Data Width Setup time for the Control Logic | 1.85 | 2.11 | 2.48 | ns |
| $t_{HDDWNVM}$ | Data Width Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SURENNVM}$ | Read Enable Setup time for the Control Logic | 3.85 | 4.39 | 5.16 | ns |
| $t_{HDRENNVM}$ | Read Enable Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUWENNVM}$ | Write Enable Setup time for the Control Logic | 2.37 | 2.69 | 3.17 | ns |
| $t_{HDWENNVM}$ | Write Enable Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUPROGNVM}$ | Program Setup time for the Control Logic | 2.16 | 2.46 | 2.89 | ns |
| $t_{HDPROGNVM}$ | Program Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUSPAREPAGE}$ | SparePage Setup time for the Control Logic | 3.74 | 4.26 | 5.01 | ns |
| $t_{HDSPAREPAGE}$ | SparePage Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUAUXBLK}$ | Auxiliary Block Setup Time for the Control Logic | 3.74 | 4.26 | 5.00 | ns |
| $t_{HDAUXBLK}$ | Auxiliary Block Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SURDNEXT}$ | ReadNext Setup Time for the Control Logic | 2.17 | 2.47 | 2.90 | ns |
| $t_{HDRDNEXT}$ | ReadNext Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUERASEPG}$ | Erase Page Setup Time for the Control Logic | 3.76 | 4.28 | 5.03 | ns |
| $t_{HDERASEPG}$ | Erase Page Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUUNPROTECTPG}$ | Unprotect Page Setup Time for the Control Logic | 2.01 | 2.29 | 2.69 | ns |
| $t_{HDUNPROTECTPG}$ | Unprotect Page Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUDISCARDPG}$ | Discard Page Setup Time for the Control Logic | 1.88 | 2.14 | 2.52 | ns |
| $t_{HDDISCARDPG}$ | Discard Page Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUOVERWRPRO}$ | Overwrite Protect Setup Time for the Control Logic | 1.64 | 1.86 | 2.19 | ns |
| $t_{HDOVERWRPRO}$ | Overwrite Protect Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |

The following signals are used to configure the RAM4K9 memory element.

### WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-27).

**Table 2-27 • Allowable Aspect Ratio Settings for WIDTHA[1:0]**

| WIDTHA1, WIDTHA0 | WIDTHB1, WIDTHB0 | D×W |
|---|---|---|
| 00 | 00 | 4k×1 |
| 01 | 01 | 2k×2 |
| 10 | 10 | 1k×4 |
| 11 | 11 | 512×9 |
| *Note: The aspect ratio settings are constant and cannot be changed on the fly.* | | |

### BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the corresponding port's outputs hold the previous value.

### WENA and WENB

These signals switch the RAM between read and write mode for the respective ports. A Low on these signals indicates a write operation, and a High indicates a read.

### CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

### PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A Low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A High indicates a pipelined, read and data appears on the corresponding output in the next clock cycle.

### WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A Low on these signals makes the output retain data from the previous read. A High indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

### RESET

This active low signal resets the output to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

### ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-28).

**Table 2-28 • Address Pins Unused/Used for Various Supported Bus Widths**

| D×W | ADDRx | |
|---|---|---|
| | Unused | Used |
| 4k×1 | None | [11:0] |
| 2k×2 | [11] | [10:0] |
| 1k×4 | [11:10] | [9:0] |
| 512×9 | [11:9] | [8:0] |

*Note: The "x" in ADDRx implies A or B.*

### DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-29).

### DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-29). The output data on unused pins is undefined.

***Table 2-29* • Unused/Used Input and Output Data Pins for Various Supported Bus Widths**

| D×W | DINx/DOUTx | |
|---|---|---|
| | **Unused** | **Used** |
| 4k×1 | [8:1] | [0] |
| 2k×2 | [8:2] | [1:0] |
| 1k×4 | [8:4] | [3:0] |
| 512×9 | None | [8:0] |

*Note: The "x" in DINx and DOUTx implies A or B.*

## RAM512X18 Description

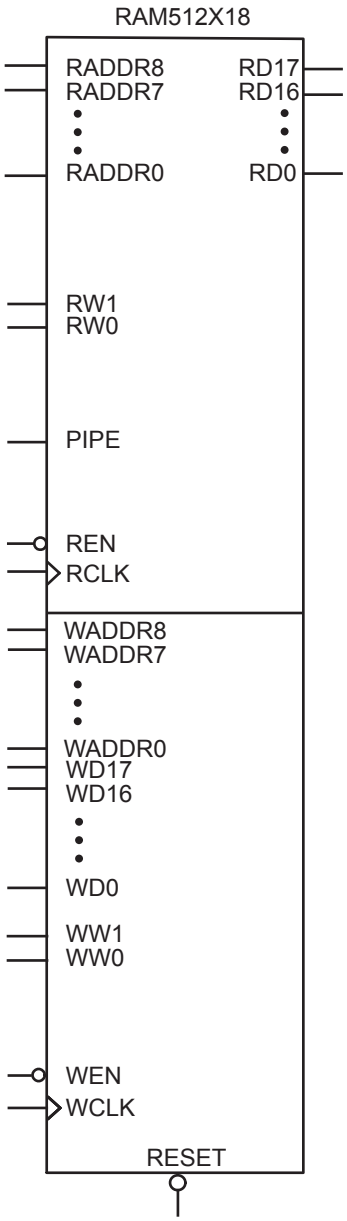



***Figure 2-49 •*** **RAM512X18**

Table 2-36 describes each pin in the Analog Block. Each function within the Analog Block will be explained in detail in the following sections.

***Table 2-36* • Analog Block Pin Description**

| Signal Name | Number of Bits | Direction | Function | Location of Details |
|---|---|---|---|---|
| VAREF | 1 | Input/Output | Voltage reference for ADC | ADC |
| ADCGNDREF | 1 | Input | External ground reference | ADC |
| MODE[3:0] | 4 | Input | ADC operating mode | ADC |
| SYSCLK | 1 | Input | External system clock | |
| TVC[7:0] | 8 | Input | Clock divide control | ADC |
| STC[7:0] | 8 | Input | Sample time control | ADC |
| ADCSTART | 1 | Input | Start of conversion | ADC |
| PWRDWN | 1 | Input | ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin. | ADC |
| ADCRESET | 1 | Input | ADC resets and disables Analog Quad – active high | ADC |
| BUSY | 1 | Output | 1 – Running conversion | ADC |
| CALIBRATE | 1 | Output | 1 – Power-up calibration | ADC |
| DATAVALID | 1 | Output | 1 – Valid conversion result | ADC |
| RESULT[11:0] | 12 | Output | Conversion result | ADC |
| TMSTBINT | 1 | Input | Internal temp. monitor strobe | ADC |
| SAMPLE | 1 | Output | 1 – An analog signal is actively being sampled (stays high during signal acquisition only)<br>0 – No analog signal is being sampled | ADC |
| VAREFSEL | 1 | Input | 0 = Output internal voltage reference (2.56 V) to VAREF<br>1 = Input external voltage reference from VAREF and ADCGNDREF | ADC |
| CHNUMBER[4:0] | 5 | Input | Analog input channel select | Input multiplexer |
| ACMCLK | 1 | Input | ACM clock | ACM |
| ACMWEN | 1 | Input | ACM write enable – active high | ACM |
| ACMRESET | 1 | Input | ACM reset – active low | ACM |
| ACMWDATA[7:0] | 8 | Input | ACM write data | ACM |
| ACMRDATA[7:0] | 8 | Output | ACM read data | ACM |
| ACMADDR[7:0] | 8 | Input | ACM address | ACM |
| CMSTB0 to CMSTB9 | 10 | Input | Current monitor strobe – 1 per quad, active high | Analog Quad |

Table 2-61 details the settings available to either power down or enable the prescaler associated with the analog inputs AV, AC, and AT.

***Table 2-61* • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

| Control Lines Bx[7] | Prescaler Op Amp |
|---|---|
| 0 | Power-down |
| 1 | Operational |

Table 2-62 details the settings available to enable the Current Monitor Block associated with the AC pin.

***Table 2-62* • Current Monitor Input Switch Control Truth Table—AV (x = 0)**

| Control Lines B0[4] | Current Monitor Input Switch |
|---|---|
| 0 | Off |
| 1 | On |

Table 2-63 details the settings available to configure the drive strength of the gate drive when not in high-drive mode.

***Table 2-63* • Low-Drive Gate Driver Current Truth Table (AG)**

| Control Lines B2[3] | Control Lines B2[2] | Current (µA) |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 3 |
| 1 | 0 | 10 |
| 1 | 1 | 30 |

Table 2-64 details the settings available to set the polarity of the gate driver (either p-channel- or n-channel-type devices).

***Table 2-64* • Gate Driver Polarity Truth Table (AG)**

| Control Lines B2[6] | Gate Driver Polarity |
|---|---|
| 0 | Positive |
| 1 | Negative |

Table 2-65 details the settings available to turn on the Gate Driver and set whether high-drive mode is on or off.

***Table 2-65* • Gate Driver Control Truth Table (AG)**

| Control Lines B2[7] | GDON | Gate Driver |
|---|---|---|
| 0 | 0 | Off |
| 0 | 1 | Low drive on |
| 1 | 0 | Off |
| 1 | 1 | High drive on |

Table 2-66 details the settings available to turn on and off the chip internal temperature monitor.

Note: For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

***Table 2-66* • Internal Temperature Monitor Control Truth Table**

| Control Lines B2[0] | PDTMB | Chip Internal Temperature Monitor |
|---|---|---|
| 0 | 0 | Off |
| 1 | 1 | On |

Temporary overshoots are allowed according to Table 3-4 on page 3-4.

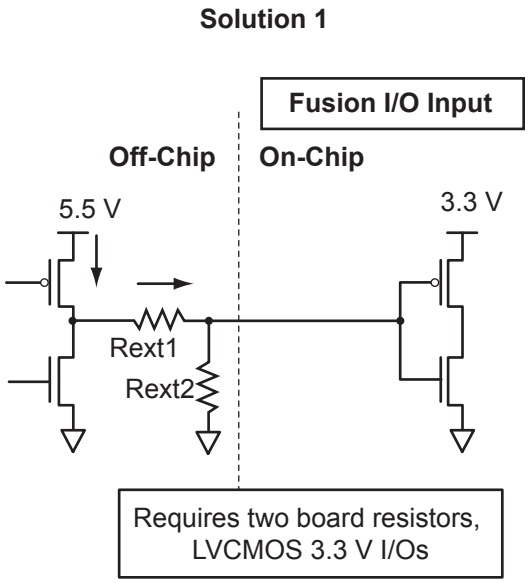



***Figure 2-103 •*** **Solution 1**

## *Solution 2*

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-4. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-104. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

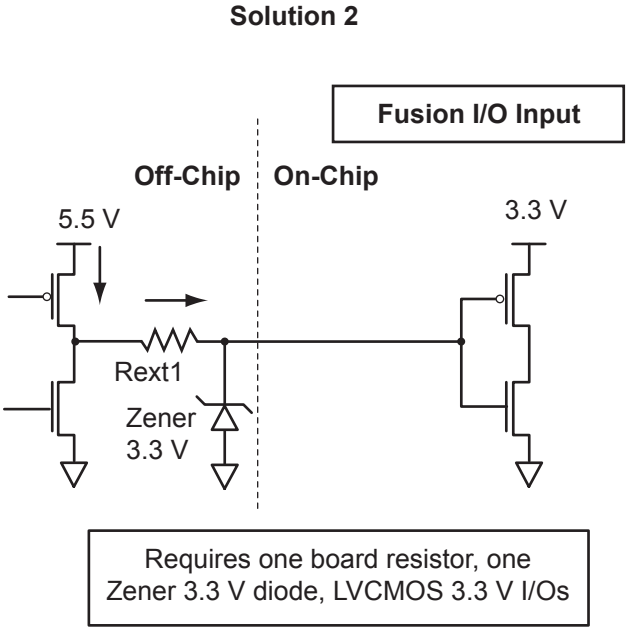



***Figure 2-104 •*** **Solution 2**

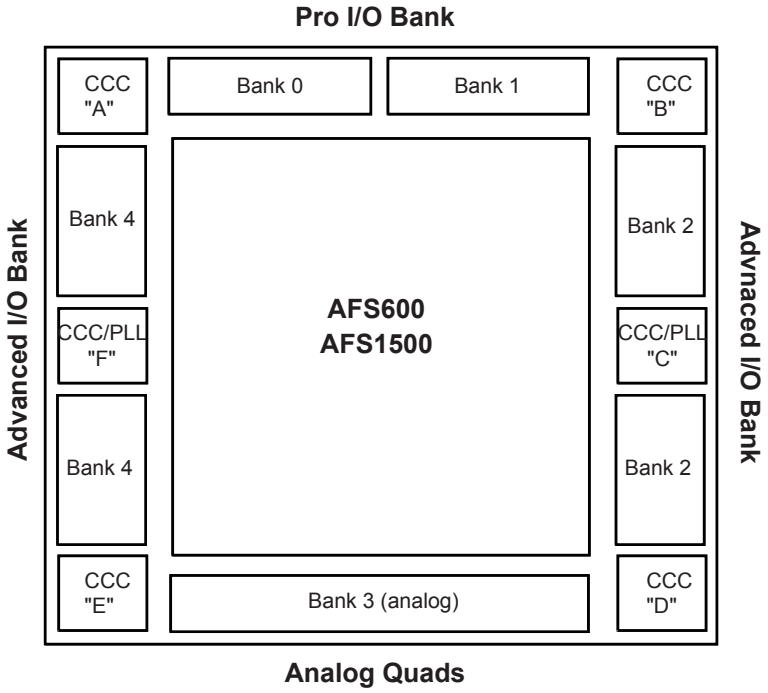



***Figure 2-114 •*** **Naming Conventions of Fusion Devices with Four I/O Banks**

**Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = I/O Standard Dependent**
**Applicable to Pro I/Os**

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ohm) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL/ 3.3 V LVCMOS | 12 mA | High | 35 | – | 0.49 | 2.74 | 0.03 | 0.90 | 1.17 | 0.32 | 2.79 | 2.14 | 2.45 | 2.70 | 4.46 | 3.81 | ns |
| 2.5 V LVCMOS | 12 mA | High | 35 | – | 0.49 | 2.80 | 0.03 | 1.13 | 1.24 | 0.32 | 2.85 | 2.61 | 2.51 | 2.61 | 4.52 | 4.28 | ns |
| 1.8 V LVCMOS | 12 mA | High | 35 | – | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 | ns |
| 1.5 V LVCMOS | 12 mA | High | 35 | – | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 | ns |
| 3.3 V PCI | Per PCI spec | High | 10 | 25 [2] | 0.49 | 2.09 | 0.03 | 0.78 | 1.25 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 | ns |
| 3.3 V PCI-X | Per PCI-X spec | High | 10 | 25 [2] | 0.49 | 2.09 | 0.03 | 0.77 | 1.17 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 | ns |
| 3.3 V GTL | 20 mA | High | 10 | 25 | 0.49 | 1.55 | 0.03 | 2.19 | – | 0.32 | 1.52 | 1.55 | 0.00 | 0.00 | 3.19 | 3.22 | ns |
| 2.5 V GTL | 20 mA | High | 10 | 25 | 0.49 | 1.59 | 0.03 | 1.83 | – | 0.32 | 1.61 | 1.59 | 0.00 | 0.00 | 3.28 | 3.26 | ns |
| 3.3 V GTL+ | 35 mA | High | 10 | 25 | 0.49 | 1.53 | 0.03 | 1.19 | – | 0.32 | 1.56 | 1.53 | 0.00 | 0.00 | 3.23 | 3.20 | ns |
| 2.5 V GTL+ | 33 mA | High | 10 | 25 | 0.49 | 1.65 | 0.03 | 1.13 | – | 0.32 | 1.68 | 1.57 | 0.00 | 0.00 | 3.35 | 3.24 | ns |
| HSTL (I) | 8 mA | High | 20 | 50 | 0.49 | 2.37 | 0.03 | 1.59 | – | 0.32 | 2.42 | 2.35 | 0.00 | 0.00 | 4.09 | 4.02 | ns |
| HSTL (II) | 15 mA | High | 20 | 25 | 0.49 | 2.26 | 0.03 | 1.59 | – | 0.32 | 2.30 | 2.03 | 0.00 | 0.00 | 3.97 | 3.70 | ns |
| SSTL2 (I) | 17 mA | High | 30 | 50 | 0.49 | 1.59 | 0.03 | 1.00 | – | 0.32 | 1.62 | 1.38 | 0.00 | 0.00 | 3.29 | 3.05 | ns |
| SSTL2 (II) | 21 mA | High | 30 | 25 | 0.49 | 1.62 | 0.03 | 1.00 | – | 0.32 | 1.65 | 1.32 | 0.00 | 0.00 | 3.32 | 2.99 | ns |
| SSTL3 (I) | 16 mA | High | 30 | 50 | 0.49 | 1.72 | 0.03 | 0.93 | – | 0.32 | 1.75 | 1.37 | 0.00 | 0.00 | 3.42 | 3.04 | ns |
| SSTL3 (II) | 24 mA | High | 30 | 25 | 0.49 | 1.54 | 0.03 | 0.93 | – | 0.32 | 1.57 | 1.25 | 0.00 | 0.00 | 3.24 | 2.92 | ns |
| LVDS | 24 mA | High | – | – | 0.49 | 1.57 | 0.03 | 1.36 | – | – | – | – | – | – | – | – | ns |
| LVPECL | 24 mA | High | – | – | 0.49 | 1.60 | 0.03 | 1.22 | – | – | – | – | – | – | – | – | ns |

*Notes:*

1. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-123 on page 2-197 for connectivity. This resistor is not required during normal operation.*

**Table 2-114 • 2.5 V LVCMOS Low Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Advanced I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.66 | 11.40 | 0.04 | 1.31 | 0.43 | 11.22 | 11.40 | 2.68 | 2.20 | 13.45 | 13.63 | ns |
| | –1 | 0.56 | 9.69 | 0.04 | 1.11 | 0.36 | 9.54 | 9.69 | 2.28 | 1.88 | 11.44 | 11.60 | ns |
| | –2 | 0.49 | 8.51 | 0.03 | 0.98 | 0.32 | 8.38 | 8.51 | 2.00 | 1.65 | 10.05 | 10.18 | ns |
| 8 mA | Std. | 0.66 | 7.96 | 0.04 | 1.31 | 0.43 | 8.11 | 7.81 | 3.05 | 2.89 | 10.34 | 10.05 | ns |
| | –1 | 0.56 | 6.77 | 0.04 | 1.11 | 0.36 | 6.90 | 6.65 | 2.59 | 2.46 | 8.80 | 8.55 | ns |
| | –2 | 0.49 | 5.94 | 0.03 | 0.98 | 0.32 | 6.05 | 5.84 | 2.28 | 2.16 | 7.72 | 7.50 | ns |
| 12 mA | Std. | 0.66 | 6.18 | 0.04 | 1.31 | 0.43 | 6.29 | 5.92 | 3.30 | 3.32 | 8.53 | 8.15 | ns |
| | –1 | 0.56 | 5.26 | 0.04 | 1.11 | 0.36 | 5.35 | 5.03 | 2.81 | 2.83 | 7.26 | 6.94 | ns |
| | –2 | 0.49 | 4.61 | 0.03 | 0.98 | 0.32 | 4.70 | 4.42 | 2.47 | 2.48 | 6.37 | 6.09 | ns |
| 16 mA | Std. | 0.66 | 6.18 | 0.04 | 1.31 | 0.43 | 6.29 | 5.92 | 3.30 | 3.32 | 8.53 | 8.15 | ns |
| | –1 | 0.56 | 5.26 | 0.04 | 1.11 | 0.36 | 5.35 | 5.03 | 2.81 | 2.83 | 7.26 | 6.94 | ns |
| | –2 | 0.49 | 4.61 | 0.03 | 0.98 | 0.32 | 4.70 | 4.42 | 2.47 | 2.48 | 6.37 | 6.09 | ns |
| 24 mA | Std. | 0.66 | 6.18 | 0.04 | 1.31 | 0.43 | 6.29 | 5.92 | 3.30 | 3.32 | 8.53 | 8.15 | ns |
| | –1 | 0.56 | 5.26 | 0.04 | 1.11 | 0.36 | 5.35 | 5.03 | 2.81 | 2.83 | 7.26 | 6.94 | ns |
| | –2 | 0.49 | 4.61 | 0.03 | 0.98 | 0.32 | 4.70 | 4.42 | 2.47 | 2.48 | 6.37 | 6.09 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-159 • Minimum and Maximum DC Input and Output Levels**

| SSTL2 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 18 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI – 0.43 | 18 | 18 | 124 | 169 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

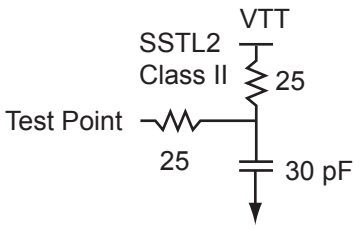



**Figure 2-131 • AC Loading**

**Table 2-160 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-161 • SSTL 2 Class II**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.17 | 0.04 | 1.33 | 0.43 | 2.21 | 1.77 | | | 4.44 | 4.01 | ns |
| –1 | 0.56 | 1.84 | 0.04 | 1.14 | 0.36 | 1.88 | 1.51 | | | 3.78 | 3.41 | ns |
| –2 | 0.49 | 1.62 | 0.03 | 1.00 | 0.32 | 1.65 | 1.32 | | | 3.32 | 2.99 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

## Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

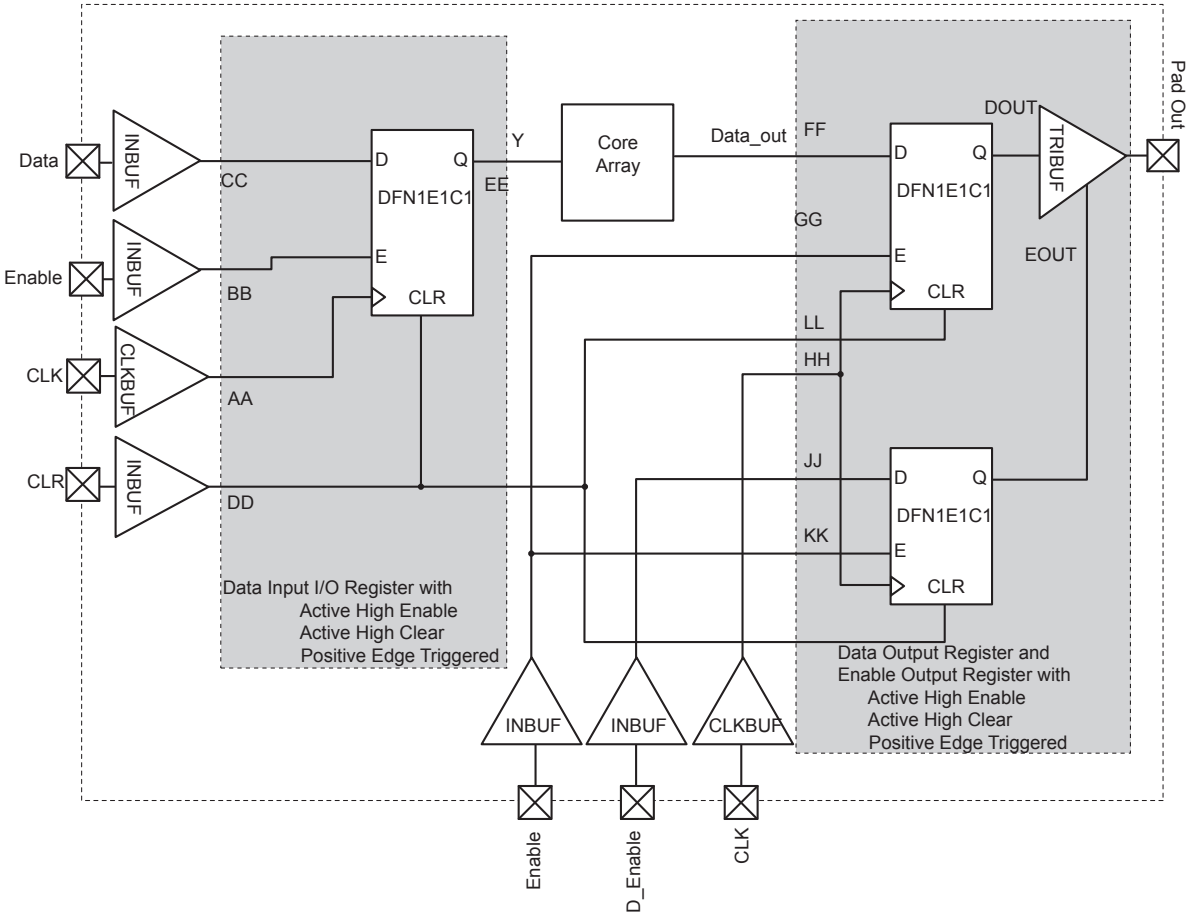



***Figure 2-138 •*** **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{ja(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

*EQ 7*

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

*EQ 8*

where

$\theta_{JA}$ = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$\theta_{SA}$ = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

*EQ 9*

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Microsemi FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

## Temperature and Voltage Derating Factors

***Table 3-7 •*** **Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J$ = 70°C, Worst-Case VCC = 1.425 V)**

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **100°C** |
| 1.425 | 0.88 | 0.93 | 0.95 | 1.00 | 1.02 | 1.05 |
| 1.500 | 0.83 | 0.88 | 0.90 | 0.95 | 0.96 | 0.99 |
| 1.575 | 0.80 | 0.85 | 0.87 | 0.91 | 0.93 | 0.96 |

| QN180 | | |
|---|---|---|
| Pin Number | AFS090 Function | AFS250 Function |
| B9 | XTAL2 | XTAL2 |
| B10 | GEA0/IO44NDB3V0 | GFA0/IO66NDB3V0 |
| B11 | GEB2/IO42PDB3V0 | IO60NDB3V0 |
| B12 | VCC | VCC |
| B13 | VCCNVM | VCCNVM |
| B14 | VCC15A | VCC15A |
| B15 | NCAP | NCAP |
| B16 | VCC33N | VCC33N |
| B17 | GNDAQ | GNDAQ |
| B18 | AC0 | AC0 |
| B19 | AT0 | AT0 |
| B20 | AT1 | AT1 |
| B21 | AV1 | AV1 |
| B22 | AC2 | AC2 |
| B23 | ATRTN1 | ATRTN1 |
| B24 | AG3 | AG3 |
| B25 | AV3 | AV3 |
| B26 | AG4 | AG4 |
| B27 | ATRTN2 | ATRTN2 |
| B28 | NC | AC5 |
| B29 | VCC33A | VCC33A |
| B30 | VAREF | VAREF |
| B31 | PUB | PUB |
| B32 | PTEM | PTEM |
| B33 | GNDNVM | GNDNVM |
| B34 | VCC | VCC |
| B35 | TCK | TCK |
| B36 | TMS | TMS |
| B37 | TRST | TRST |
| B38 | GDB2/IO41PSB1V0 | GDA2/IO55PSB1V0 |
| B39 | GDC0/IO38NDB1V0 | GDB0/IO53NDB1V0 |
| B40 | VCCIB1 | VCCIB1 |
| B41 | GCA1/IO36PDB1V0 | GCA1/IO49PDB1V0 |
| B42 | GCC0/IO34NDB1V0 | GCC0/IO47NDB1V0 |
| B43 | GCB2/IO33PSB1V0 | GBC2/IO42PSB1V0 |
| B44 | VCC | VCC |

| QN180 | | |
|---|---|---|
| Pin Number | AFS090 Function | AFS250 Function |
| B45 | GBA2/IO31PDB1V0 | GBA2/IO40PDB1V0 |
| B46 | GNDQ | GNDQ |
| B47 | GBA1/IO30RSB0V0 | GBA0/IO38RSB0V0 |
| B48 | GBB1/IO28RSB0V0 | GBC1/IO35RSB0V0 |
| B49 | VCC | VCC |
| B50 | GBC0/IO25RSB0V0 | IO31RSB0V0 |
| B51 | IO23RSB0V0 | IO28RSB0V0 |
| B52 | IO20RSB0V0 | IO25RSB0V0 |
| B53 | VCC | VCC |
| B54 | IO11RSB0V0 | IO14RSB0V0 |
| B55 | IO08RSB0V0 | IO11RSB0V0 |
| B56 | GAC1/IO05RSB0V0 | IO08RSB0V0 |
| B57 | VCCIB0 | VCCIB0 |
| B58 | GAB0/IO02RSB0V0 | GAC0/IO04RSB0V0 |
| B59 | GAA0/IO00RSB0V0 | GAA1/IO01RSB0V0 |
| B60 | VCCPLA | VCCPLA |
| C1 | NC | NC |
| C2 | NC | VCCIB3 |
| C3 | GND | GND |
| C4 | NC | GFC2/IO69PPB3V0 |
| C5 | GFC1/IO49PDB3V0 | GFC1/IO68PDB3V0 |
| C6 | GFA0/IO47NPB3V0 | GFB0/IO67NPB3V0 |
| C7 | VCCIB3 | NC |
| C8 | GND | GND |
| C9 | GEA1/IO44PDB3V0 | GFA1/IO66PDB3V0 |
| C10 | GEA2/IO42NDB3V0 | GEC2/IO60PDB3V0 |
| C11 | NC | GEA2/IO58PSB3V0 |
| C12 | NC | NC |
| C13 | GND | GND |
| C14 | NC | NC |
| C15 | NC | NC |
| C16 | GNDA | GNDA |
| C17 | NC | NC |
| C18 | NC | NC |
| C19 | NC | NC |
| C20 | NC | NC |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| A1 | NC |
| A2 | GND |
| A3 | NC |
| A4 | NC |
| A5 | GND |
| A6 | NC |
| A7 | NC |
| A8 | GND |
| A9 | IO17NDB0V2 |
| A10 | IO17PDB0V2 |
| A11 | GND |
| A12 | IO18NDB0V2 |
| A13 | IO18PDB0V2 |
| A14 | IO20NDB0V2 |
| A15 | IO20PDB0V2 |
| A16 | GND |
| A17 | IO21PDB0V2 |
| A18 | IO21NDB0V2 |
| A19 | GND |
| A20 | IO39NDB1V2 |
| A21 | IO39PDB1V2 |
| A22 | GND |
| A23 | NC |
| A24 | NC |
| A25 | GND |
| A26 | NC |
| AA1 | NC |
| AA2 | VCCIB4 |
| AA3 | IO93PDB4V0 |
| AA4 | GND |
| AA5 | IO93NDB4V0 |
| AA6 | GEB2/IO86PDB4V0 |
| AA7 | IO86NDB4V0 |
| AA8 | AV0 |
| AA9 | GNDA |
| AA10 | AV1 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| AA11 | AV2 |
| AA12 | GNDA |
| AA13 | AV3 |
| AA14 | AV6 |
| AA15 | GNDA |
| AA16 | AV7 |
| AA17 | AV8 |
| AA18 | GNDA |
| AA19 | AV9 |
| AA20 | VCCIB2 |
| AA21 | IO68PPB2V0 |
| AA22 | TCK |
| AA23 | GND |
| AA24 | IO76PPB2V0 |
| AA25 | VCCIB2 |
| AA26 | NC |
| AB1 | GND |
| AB2 | NC |
| AB3 | GEC2/IO87PDB4V0 |
| AB4 | IO87NDB4V0 |
| AB5 | GEA2/IO85PDB4V0 |
| AB6 | IO85NDB4V0 |
| AB7 | NCAP |
| AB8 | AC0 |
| AB9 | VCC33A |
| AB10 | AC1 |
| AB11 | AC2 |
| AB12 | VCC33A |
| AB13 | AC3 |
| AB14 | AC6 |
| AB15 | VCC33A |
| AB16 | AC7 |
| AB17 | AC8 |
| AB18 | VCC33A |
| AB19 | AC9 |
| AB20 | ADCGNDREF |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| AB21 | PTBASE |
| AB22 | GNDNVM |
| AB23 | VCCNVM |
| AB24 | VPUMP |
| AB25 | NC |
| AB26 | GND |
| AC1 | NC |
| AC2 | NC |
| AC3 | NC |
| AC4 | GND |
| AC5 | VCCIB4 |
| AC6 | VCCIB4 |
| AC7 | PCAP |
| AC8 | AG0 |
| AC9 | GNDA |
| AC10 | AG1 |
| AC11 | AG2 |
| AC12 | GNDA |
| AC13 | AG3 |
| AC14 | AG6 |
| AC15 | GNDA |
| AC16 | AG7 |
| AC17 | AG8 |
| AC18 | GNDA |
| AC19 | AG9 |
| AC20 | VAREF |
| AC21 | VCCIB2 |
| AC22 | PTEM |
| AC23 | GND |
| AC24 | NC |
| AC25 | NC |
| AC26 | NC |
| AD1 | NC |
| AD2 | NC |
| AD3 | GND |
| AD4 | NC |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| G13 | IO22NDB1V0 |
| G14 | IO22PDB1V0 |
| G15 | GND |
| G16 | IO32PPB1V1 |
| G17 | IO36NPB1V2 |
| G18 | VCCIB1 |
| G19 | GND |
| G20 | IO47NPB2V0 |
| G21 | IO49PDB2V0 |
| G22 | VCCIB2 |
| G23 | IO46NDB2V0 |
| G24 | GBC2/IO46PDB2V0 |
| G25 | IO48NPB2V0 |
| G26 | NC |
| H1 | GND |
| H2 | NC |
| H3 | IO118NDB4V0 |
| H4 | IO118PDB4V0 |
| H5 | IO119NPB4V0 |
| H6 | IO124NDB4V0 |
| H7 | GND |
| H8 | VCOMPLA |
| H9 | VCCPLA |
| H10 | VCCIB0 |
| H11 | IO12NDB0V1 |
| H12 | IO12PDB0V1 |
| H13 | VCCIB0 |
| H14 | VCCIB1 |
| H15 | IO30NDB1V1 |
| H16 | IO30PDB1V1 |
| H17 | VCCIB1 |
| H18 | IO36PPB1V2 |
| H19 | IO38NPB1V2 |
| H20 | GND |
| H21 | IO49NDB2V0 |
| H22 | IO50PDB2V0 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| H23 | IO50NDB2V0 |
| H24 | IO51PDB2V0 |
| H25 | NC |
| H26 | GND |
| J1 | NC |
| J2 | VCCIB4 |
| J3 | IO115PDB4V0 |
| J4 | GND |
| J5 | IO116NDB4V0 |
| J6 | IO116PDB4V0 |
| J7 | VCCIB4 |
| J8 | IO117PDB4V0 |
| J9 | VCCIB4 |
| J10 | GND |
| J11 | IO06NDB0V1 |
| J12 | IO06PDB0V1 |
| J13 | IO16NDB0V2 |
| J14 | IO16PDB0V2 |
| J15 | IO28NDB1V1 |
| J16 | IO28PDB1V1 |
| J17 | GND |
| J18 | IO38PPB1V2 |
| J19 | IO53PDB2V0 |
| J20 | VCCIB2 |
| J21 | IO52PDB2V0 |
| J22 | IO52NDB2V0 |
| J23 | GND |
| J24 | IO51NDB2V0 |
| J25 | VCCIB2 |
| J26 | NC |
| K1 | NC |
| K2 | NC |
| K3 | IO115NDB4V0 |
| K4 | IO113PDB4V0 |
| K5 | VCCIB4 |
| K6 | IO114NDB4V0 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| K7 | IO114PDB4V0 |
| K8 | IO117NDB4V0 |
| K9 | GND |
| K10 | VCC |
| K11 | VCCIB0 |
| K12 | GND |
| K13 | VCCIB0 |
| K14 | VCCIB1 |
| K15 | GND |
| K16 | VCCIB1 |
| K17 | GND |
| K18 | GND |
| K19 | IO53NDB2V0 |
| K20 | IO57PDB2V0 |
| K21 | GCA2/IO59PDB2V0 |
| K22 | VCCIB2 |
| K23 | IO54NDB2V0 |
| K24 | IO54PDB2V0 |
| K25 | NC |
| K26 | NC |
| L1 | GND |
| L2 | NC |
| L3 | IO112PPB4V0 |
| L4 | IO113NDB4V0 |
| L5 | GFB2/IO109PDB4V0 |
| L6 | GFA2/IO110PDB4V0 |
| L7 | IO112NPB4V0 |
| L8 | IO104PDB4V0 |
| L9 | IO111PDB4V0 |
| L10 | VCCIB4 |
| L11 | GND |
| L12 | VCC |
| L13 | GND |
| L14 | VCC |
| L15 | GND |
| L16 | VCC |

| Revision | Changes | Page |
|---|---|---|
| Advance v1.5 (continued) | This bullet was added to the "Integrated A/D Converter (ADC) and Analog I/O" section: ADC Accuracy is Better than 1% | I |
| | In the "Integrated Analog Blocks and Analog I/Os" section, ±4 LSB was changed to 0.72. The following sentence was deleted:<br>The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V.<br>In addition, 2°C was changed to 3°C:<br>"One analog input in each quad can be connected to an external temperature monitor diode and achieves detection accuracy of ±3ºC."<br>The following sentence was deleted:<br>The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V. | 1-4 |
| | The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA. | N/A |
| Advance v1.4 (July 2008) | In Table 3-8 · Quiescent Supply Current Characteristics (IDDQ)1, footnote references were updated for $I_{DC2}$ and $I_{DC3}$.<br>Footnote 3 and 4 were updated and footnote 5 is new. | 3-11 |
| Advance v1.3 (July 2008) | The "ADC Description" section was significantly updated. Please review carefully. | 2-102 |
| Advance v1.2 (May 2008) | Table 2-25 • Flash Memory Block Timing was significantly updated. | 2-55 |
| | The "$V_{AREF}$ Analog Reference Voltage" pin description section was significantly update. Please review it carefully. | 2-226 |
| | Table 2-45 • ADC Interface Timing was significantly updated. | 2-110 |
| | Table 2-56 • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3) was significantly updated. | 2-131 |
| | The following sentence was deleted from the "Voltage Monitor" section:<br>The Analog Quad inputs are tolerant up to 12 V + 10%. | 2-86 |
| | The "180-Pin QFN" figure was updated. D1 to D4 are new and the figure was changed to bottom view. The note below the figure is new. | 3-3 |
| Advance v1.1 (May 2008) | The following text was incorrect and therefore deleted:<br>**VCC33A** **Analog Power Filter**<br>Analog power pin for the analog power supply low-pass filter. An external 100 pF capacitor should be connected between this pin and ground.<br>There is still a description of $V_{CC33A}$ on page 2-224. | 2-204 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.6 (continued) | The "Analog-to-Digital Converter Block" section was updated with the following statement:<br>"All results are MSB justified in the ADC." | 2-99 |
| | The information about the ADCSTART signal was updated in the "ADC Description" section. | 2-102 |
| | Table 2-46 · Analog Channel Specifications was updated. | 2-118 |
| | Table 2-47 · ADC Characteristics in Direct Input Mode was updated. | 2-121 |
| | Table 2-51 • ACM Address Decode Table for Analog Quad was updated. | 2-127 |
| | In Table 2-53 • Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated. | 2-130 |
| | The "Introduction" section was updated to include information about digital inputs, outputs, and bibufs. | 2-133 |
| | In Table 2-69 • Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features:<br>Single-ended receiver<br>Voltage-referenced differential receiver<br>LVDS/LVPECL differential receiver features | 2-137 |
| | The "User I/O Naming Convention" section was updated to include "V" and "z" descriptions | 2-159 |
| | The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw. | 2-224 |
| | The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw. | 2-224 |
| | The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and $V_{CCI}$ pins within a given I/O bank. | 2-185 |
| | The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The "PTEM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090. | 3-8 |