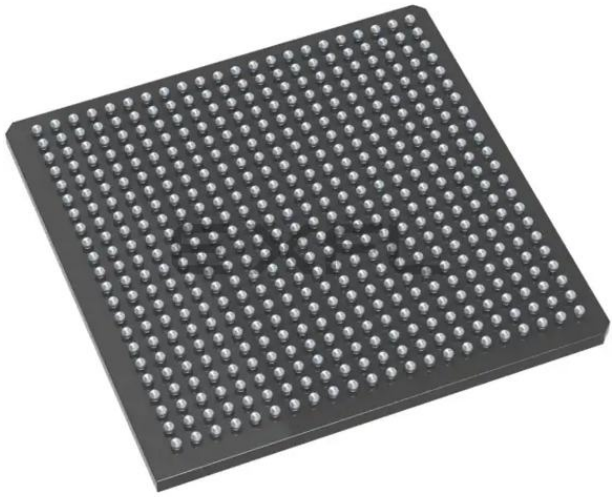

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-fg484i

The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a highly secure, low power, single-chip solution that is Instant On. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based Fusion devices are Instant On and do not need to be loaded from an external boot PROM.
On-board security mechanisms prevent access to the programming information and enable remote updates of the FPGA logic that are protected with high level security. Designers can perform remote in-system reprogramming to support future design iterations and field upgrades, with confidence that valuable IP is highly unlikely to be compromised or copied. ISP can be performed using the
industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a
built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with
AES-based security provide a high level of protection for remote field updates over public networks, such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with
industry-standard security, making remote ISP possible. A Fusion device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Data operations are performed in widths of 1 to 4 bytes. A write to a location in a page that is not already in the Page Buffer will cause the page to be read from the FB Array and stored in the Page Buffer. The block that was addressed during the write will be put into the Block Buffer, and the data written by WD will overwrite the data in the Block Buffer. After the data is written to the Block Buffer, the Block Buffer is then written to the Page Buffer to keep both buffers in sync. Subsequent writes to the same block will overwrite the Block Buffer and the Page Buffer. A write to another block in the page will cause the addressed block to be loaded from the Page Buffer, and the write will be performed as described previously.

The data width can be selected dynamically via the DATAWIDTH input bus. The truth table for the data width settings is detailed in Table 2-21. The minimum resolvable address is one 8-bit byte. For data widths greater than 8 bits, the corresponding address bits are ignored—when DATAWIDTH = 0 (2 bytes), ADDR[0] is ignored, and when DATAWIDTH = '10' or '11' (4 bytes), ADDR[1:0] are ignored. Data pins are LSB-oriented and unused WD data pins must be grounded.

Table 2-21 • **Data Width Settings**

DATAWIDTH[1:0]	Data Width
00	1 byte [7:0]
01	2 byte [15:0]
10, 11	4 bytes [31:0]

Flash Memory Block Protection

Page Loss Protection

When the PAGELOSSPROTECT pin is set to logic 1, it prevents writes to any page other than the current page in the Page Buffer until the page is either discarded or programmed.

A write to another page while the current page is Page Loss Protected will return a STATUS of '11'.

Overwrite Protection

Any page that is Overwrite Protected will result in the STATUS being set to '01' when an attempt is made to either write, program, or erase it. To set the Overwrite Protection state for a page, set the OVERWRITEPROTECT pin when a Program operation is undertaken. To clear the Overwrite Protect state for a given page, an Unprotect Page operation must be performed on the page, and then the page must be programmed with the OVERWRITEPROTECT pin cleared to save the new page.

LOCKREQUEST

The LOCKREQUEST signal is used to give the user interface control over simultaneous access of the FB from both the User and JTAG interfaces. When LOCKREQUEST is asserted, the JTAG interface will hold off any access attempts until LOCKREQUEST is deasserted.

Flash Memory Block Operations

FB Operation Priority

The FB provides for priority of operations when multiple actions are requested simultaneously. Table 2-22 shows the priority order (priority 0 is the highest).

Table 2-22 • **FB Operation Priority**

Operation	Priority
System Initialization	0
FB Reset	1
Read	2
Write	3
Erase Page	4
Program	5
Unprotect Page	6
Discard Page	7

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

ADC Interface Timing

Table 2-48 • ADC Interface Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{SUMODE}	Mode Pin Setup Time	0.56	0.64	0.75	ns
t_{HDMODE}	Mode Pin Hold Time	0.26	0.29	0.34	ns
t_{SUTVC}	Clock Divide Control (TVC) Setup Time	0.68	0.77	0.90	ns
t_{HDTVC}	Clock Divide Control (TVC) Hold Time	0.32	0.36	0.43	ns
t_{SUSTC}	Sample Time Control (STC) Setup Time	1.58	1.79	2.11	ns
t_{HDSTC}	Sample Time Control (STC) Hold Time	1.27	1.45	1.71	ns
$t_{SUVAREFSEL}$	Voltage Reference Select (VAREFSEL) Setup Time	0.00	0.00	0.00	ns
$t_{HDVAREFSEL}$	Voltage Reference Select (VAREFSEL) Hold Time	0.67	0.76	0.89	ns
$t_{SUCHNUM}$	Channel Select (CHNUMBER) Setup Time	0.90	1.03	1.21	ns
$t_{HDCHNUM}$	Channel Select (CHNUMBER) Hold Time	0.00	0.00	0.00	ns
$t_{SUADCSTART}$	Start of Conversion (ADCSTART) Setup Time	0.75	0.85	1.00	ns
$t_{HDADCSTART}$	Start of Conversion (ADCSTART) Hold Time	0.43	0.49	0.57	ns
$t_{CK2QBUSY}$	Busy Clock-to-Q	1.33	1.51	1.78	ns
$t_{CK2QCAL}$	Power-Up Calibration Clock-to-Q	0.63	0.71	0.84	ns
$t_{CK2QVAL}$	Valid Conversion Result Clock-to-Q	3.12	3.55	4.17	ns
$t_{CK2QSAMPLE}$	Sample Clock-to-Q	0.22	0.25	0.30	ns
$t_{CK2QRESULT}$	Conversion Result Clock-to-Q	2.53	2.89	3.39	ns
$t_{CLR2QBUSY}$	Busy Clear-to-Q	2.06	2.35	2.76	ns
$t_{CLR2QCAL}$	Power-Up Calibration Clear-to-Q	2.15	2.45	2.88	ns
$t_{CLR2QVAL}$	Valid Conversion Result Clear-to-Q	2.41	2.74	3.22	ns
$t_{CLR2QSAMPLE}$	Sample Clear-to-Q	2.17	2.48	2.91	ns
$t_{CLR2QRESULT}$	Conversion result Clear-to-Q	2.25	2.56	3.01	ns
t_{RECCLR}	Recovery Time of Clear	0.00	0.00	0.00	ns
t_{REMCLR}	Removal Time of Clear	0.63	0.72	0.84	ns
$t_{MPWSYSCLK}$	Clock Minimum Pulse Width for the ADC	4.00	4.00	4.00	ns
$t_{FMAXSYSCLK}$	Clock Maximum Frequency for the ADC	100.00	100.00	100.00	MHz

***Table 2-73* • Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os; All I/O Bank Types (maximum drive strength and high slew selected)**

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
LVPECL	300 MHz

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 kΩ (or lower) output drive resistance at hot insertion, and 1 kΩ (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

1. Grounds
2. Powers, I/Os, other pins

Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks and standard I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If Standard I/O banks are used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the standard I/O buffers do not have built-in I/O clamp diodes.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull down resistor and driven in the opposite direction. A small static current is induced on each IO pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Please refer to Table 2-95 on page 2-169, Table 2-96 on page 2-169, and Table 2-97 on page 2-171 for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTL 3.3 V, pull-up resistor is ~45 kΩ and the resulting current is equal to 3.3 V / 45 kΩ = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven low
- Input buffers with pull-down, driven high
- Bidirectional buffers with pull-up, driven low
- Bidirectional buffers with pull-down, driven high
- Output buffers with pull-up, driven low
- Output buffers with pull-down, driven high
- Tristate buffers with pull-up, driven low
- Tristate buffers with pull-down, driven high

Selectable Skew between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

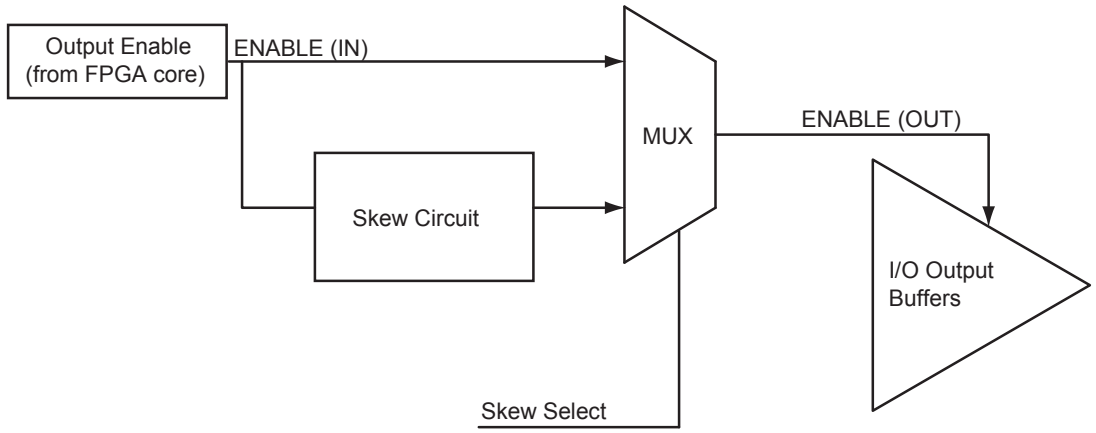

***Figure 2-107* • Block Diagram of Output Enable Path**

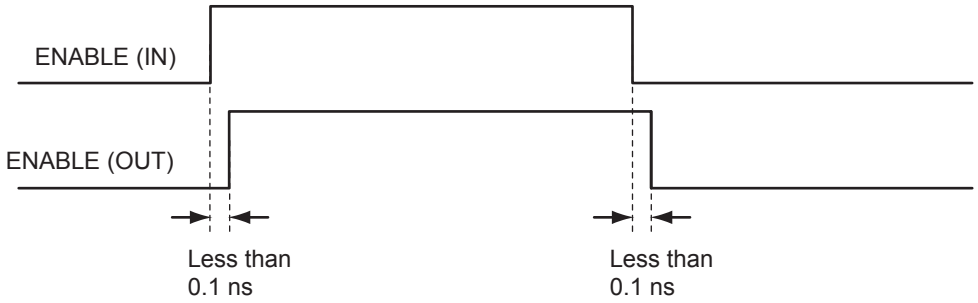

***Figure 2-108* • Timing Diagram (option1: bypasses skew circuit)**

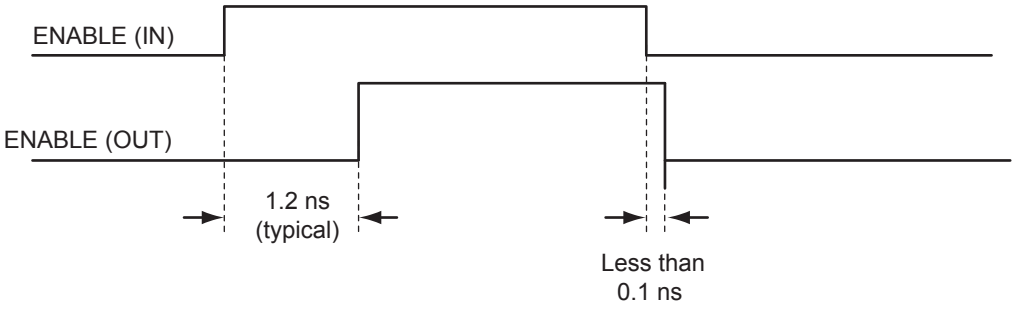

***Figure 2-109* • Timing Diagram (option 2: enables skew circuit)**

I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-84 and Table 2-85 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

Table 2-84 • **Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)*	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3
PCI (3.3 V)			3		3	3
PCI-X (3.3 V)	3		3		3	3
LVDS, BLVDS, M-LVDS			3			3
LVPECL						3

*Note: * This feature does not apply to the standard I/O banks, which are the north I/O banks of AFS090 and AFS250 devices*

***Table 2-85* • Fusion Pro I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3	3	3	3	3
PCI (3.3 V)			3		3	3	3	3		
PCI-X (3.3 V)	3		3		3	3	3	3		
GTL+ (3.3 V)			3		3	3	3	3		3
GTL+ (2.5 V)			3		3	3	3	3		3
GTL (3.3 V)			3		3	3	3	3		3
GTL (2.5 V)			3		3	3	3	3		3
HSTL Class I			3		3	3	3	3		3
HSTL Class II			3		3	3	3	3		3
SSTL2 Class I and II			3		3	3	3	3		3
SSTL3 Class I and II			3		3	3	3	3		3
LVDS, BLVDS, M-LVDS			3			3	3	3		3
LVPECL						3	3	3		3

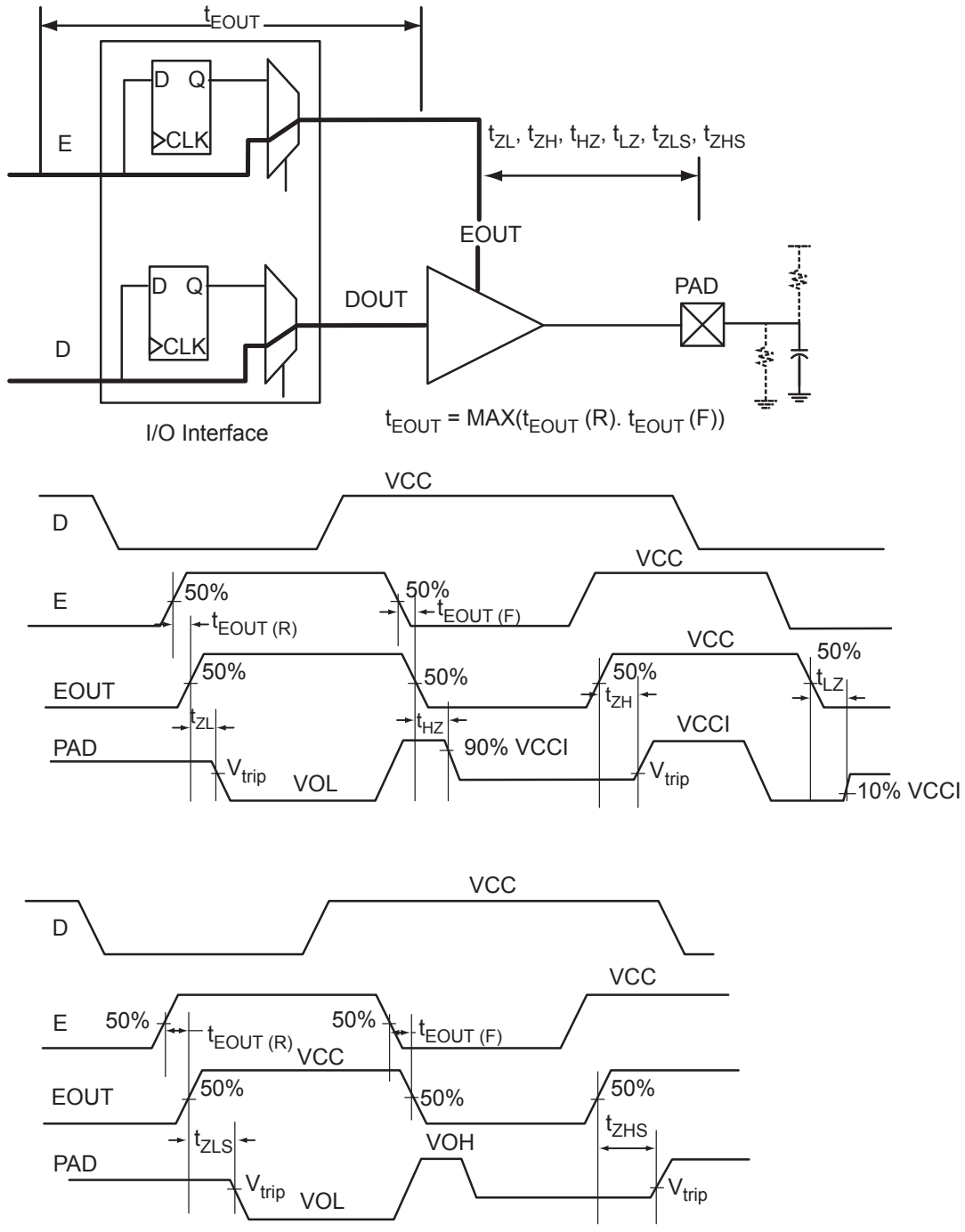

***Figure 2-118* • Tristate Output Buffer Timing Model and Delays (example)**

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

Table 2-126 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable to Pro I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

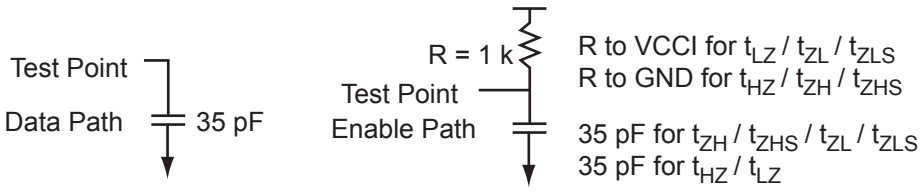

Figure 2-122 • AC Loading

Table 2-127 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

3.3 V PCI, 3.3 V PCI-X

The Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-134 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Per PCI specification	Per PCI curves										10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-123.

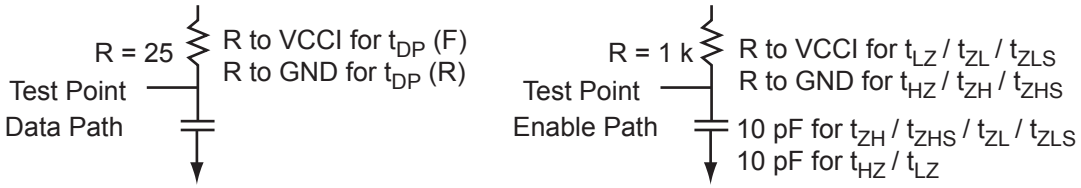

Figure 2-123 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the data path; Microsemi loading for tristate is described in Table 2-135.

Table 2-135 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$	–	10

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-136 • 3.3 V PCI/PCI-X
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.81	0.04	1.05	1.67	0.43	2.86	2.00	3.28	3.61	5.09	4.23	ns
–1	0.56	2.39	0.04	0.89	1.42	0.36	2.43	1.70	2.79	3.07	4.33	3.60	ns
–2	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-137 • 3.3 V PCI/PCI-X
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.68	0.04	0.86	0.43	2.73	1.95	3.21	3.58	4.97	4.19	0.66	ns
–1	0.56	2.28	0.04	0.73	0.36	2.32	1.66	2.73	3.05	4.22	3.56	0.56	ns
–2	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	0.49	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Output Enable Register

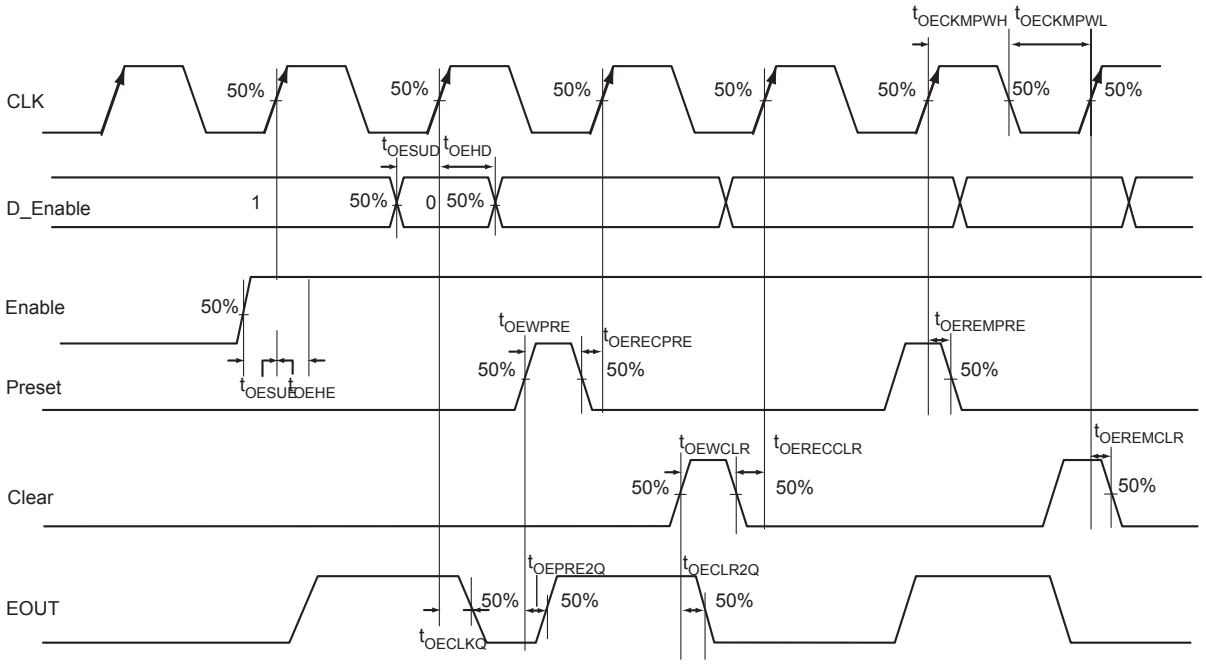

***Figure 2-141* • Output Enable Register Timing Diagram**

Timing Characteristics

***Table 2-178* • Output Enable Register Propagation Delays**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.44	0.51	0.59	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

ATRTN*x* **Temperature Monitor Return**

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The *x* in the ATRTN*x* designator indicates the quad pairing (*x* = 0 for AQ1 and AQ2, *x* = 1 for AQ2 and AQ3, ..., *x* = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURN*xy* in the software (where *x* and *y* refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-22.

Refer to the "User I/O Naming Convention" section on page 2-158 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

TCK **Test Clock**

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 2-183 for more information.

***Table 2-183* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance[2, 3]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on JTAG chain.*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin can only be pulled down.*

TDI **Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO **Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • **AFS1500 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min.	Typ.	Max.	Unit
ICC[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		20	40	mA
			T_J = 85°C		32	65	mA
			T_J = 100°C		59	120	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
ICC33[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		10.7	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.31	2	mA
			T_J = 85°C		0.35	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.9	3.6	mA
			T_J = 85°C		2.9	4	mA
			T_J = 100°C		3.3	6	mA
		Sleep mode[6], VCC33 = 3.63 V	T_J = 25°C		17	19	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
ICCI[3]	I/O quiescent current	Operational standby[4], Standby mode, and Sleep Mode[6], VCCIx = 3.63 V	T_J = 25°C		417	649	µA
			T_J = 85°C		417	649	µA
			T_J = 100°C		417	649	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

Methodology

Total Power Consumption—P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Operating Mode

$P_{STAT} = PDC1 + (N_{NVM\text{-}BLOCKS} * PDC4) + PDC5+ (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLS} * PDC9)$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = PDC2$

Sleep Mode

$P_{STAT} = PDC3$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

Sleep Mode

$P_{DYN} = 0$ W

Global Clock Dynamic Contribution—P_{CLOCK}

Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Sleep Mode

$P_{CLOCK} = 0$ W

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

Operating Mode

RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$

Operating Mode

$P_{RC\text{-}OSC}$ = PAC19

Standby Mode and Sleep Mode

$P_{RC\text{-}OSC}$ = 0 W

Analog System Dynamic Contribution—P_{AB}

Operating Mode

P_{AB} = PAC20

Standby Mode and Sleep Mode

P_{AB} = 0 W

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

***Table 3-16* • Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

***Table 3-17* • Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%
β_4	NVM enable rate for read operations	0%

FG484		
Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND
A2	VCC	NC
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0
A6	IO07NDB0V1	IO07NDB0V1
A7	IO07PDB0V1	IO07PDB0V1
A8	IO10PDB0V1	IO09PDB0V1
A9	IO14NDB0V1	IO13NDB0V2
A10	IO14PDB0V1	IO13PDB0V2
A11	IO17PDB1V0	IO24PDB1V0
A12	IO18PDB1V0	IO26PDB1V0
A13	IO19NDB1V0	IO27NDB1V1
A14	IO19PDB1V0	IO27PDB1V1
A15	IO24NDB1V1	IO35NDB1V2
A16	IO24PDB1V1	IO35PDB1V2
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A19	IO29NDB1V1	IO43NDB1V2
A20	IO29PDB1V1	IO43PDB1V2
A21	VCC	NC
A22	GND	GND
AA1	VCC	NC
AA2	GND	GND
AA3	VCCIB4	VCCIB4
AA4	VCCIB4	VCCIB4
AA5	PCAP	PCAP
AA6	AG0	AG0
AA7	GNDA	GNDA
AA8	AG1	AG1
AA9	AG2	AG2
AA10	GNDA	GNDA
AA11	AG3	AG3
AA12	AG6	AG6
AA13	GNDA	GNDA

FG484		
Pin Number	AFS600 Function	AFS1500 Function
AA14	AG7	AG7
AA15	AG8	AG8
AA16	GNDA	GNDA
AA17	AG9	AG9
AA18	VAREF	VAREF
AA19	VCCIB2	VCCIB2
AA20	PTEM	PTEM
AA21	GND	GND
AA22	VCC	NC
AB1	GND	GND
AB2	VCC	NC
AB3	NC	IO94NSB4V0
AB4	GND	GND
AB5	VCC33N	VCC33N
AB6	AT0	AT0
AB7	ATRTN0	ATRTN0
AB8	AT1	AT1
AB9	AT2	AT2
AB10	ATRTN1	ATRTN1
AB11	AT3	AT3
AB12	AT6	AT6
AB13	ATRTN3	ATRTN3
AB14	AT7	AT7
AB15	AT8	AT8
AB16	ATRTN4	ATRTN4
AB17	AT9	AT9
AB18	VCC33A	VCC33A
AB19	GND	GND
AB20	NC	IO76NPB2V0
AB21	VCC	NC
AB22	GND	GND
B1	VCC	NC
B2	GND	GND
B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
B4	GND	GND

Revision	Changes	Page
Advance v1.5 (continued)	This bullet was added to the "Integrated A/D Converter (ADC) and Analog I/O" section: ADC Accuracy is Better than 1%	I
	In the "Integrated Analog Blocks and Analog I/Os" section, ±4 LSB was changed to 0.72. The following sentence was deleted: The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V. In addition, 2°C was changed to 3°C: "One analog input in each quad can be connected to an external temperature monitor diode and achieves detection accuracy of ±3ºC." The following sentence was deleted: The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V.	1-4
	The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA.	N/A
Advance v1.4 (July 2008)	In Table 3-8 · Quiescent Supply Current Characteristics (IDDQ)1, footnote references were updated for I_{DC2} and I_{DC3}. Footnote 3 and 4 were updated and footnote 5 is new.	3-11
Advance v1.3 (July 2008)	The "ADC Description" section was significantly updated. Please review carefully.	2-102
Advance v1.2 (May 2008)	Table 2-25 • Flash Memory Block Timing was significantly updated.	2-55
	The "V_{AREF} Analog Reference Voltage" pin description section was significantly update. Please review it carefully.	2-226
	Table 2-45 • ADC Interface Timing was significantly updated.	2-110
	Table 2-56 • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3) was significantly updated.	2-131
	The following sentence was deleted from the "Voltage Monitor" section: The Analog Quad inputs are tolerant up to 12 V + 10%.	2-86
	The "180-Pin QFN" figure was updated. D1 to D4 are new and the figure was changed to bottom view. The note below the figure is new.	3-3
Advance v1.1 (May 2008)	The following text was incorrect and therefore deleted: **VCC33A** **Analog Power Filter** Analog power pin for the analog power supply low-pass filter. An external 100 pF capacitor should be connected between this pin and ground. There is still a description of V_{CC33A} on page 2-224.	2-204