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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	252
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-fg676

$$t_{PD} = MAX(t_{PD(RR)}, t_{PD(RF)}, t_{PD(FF)}, t_{PD(FR)})$$
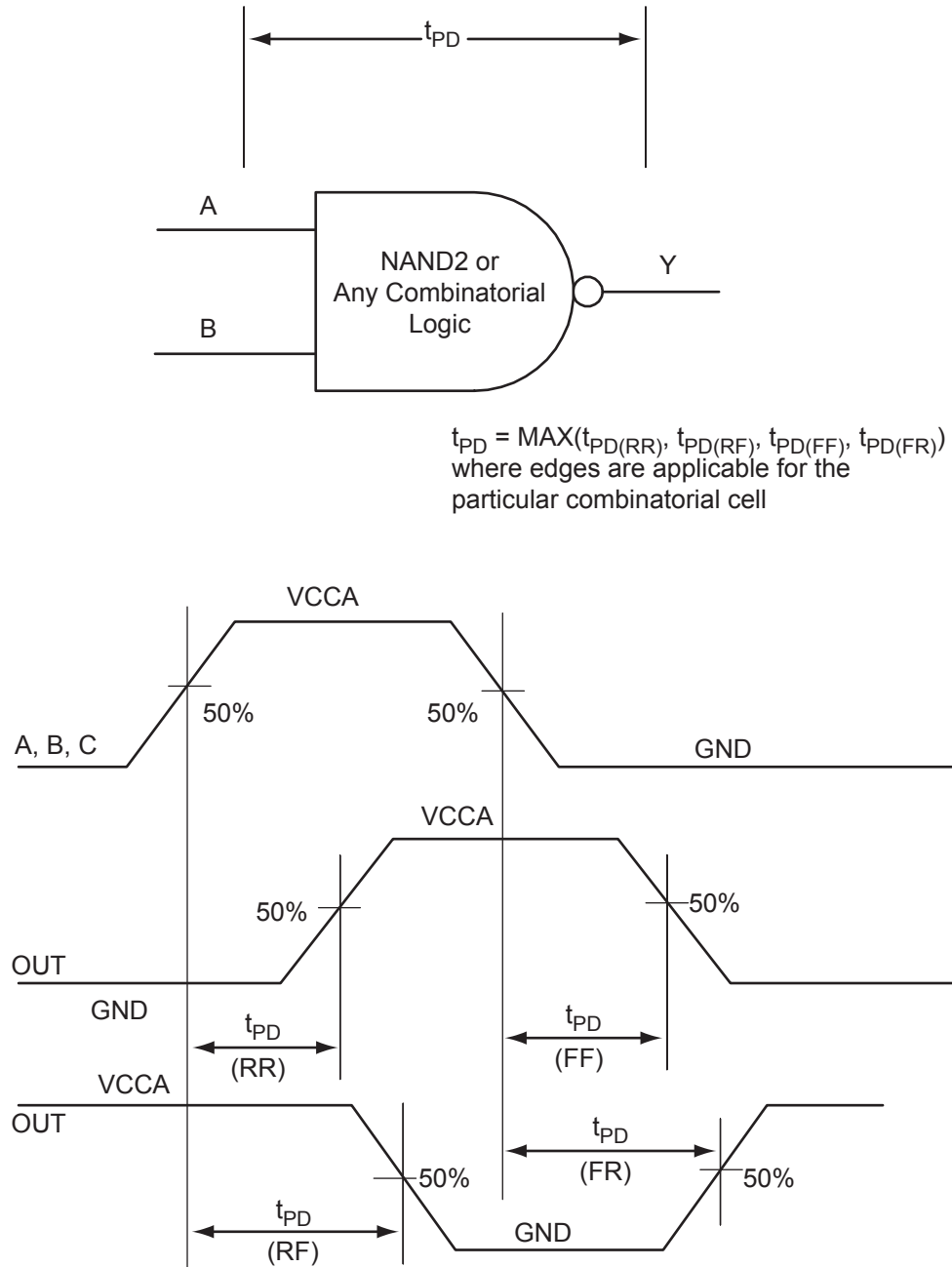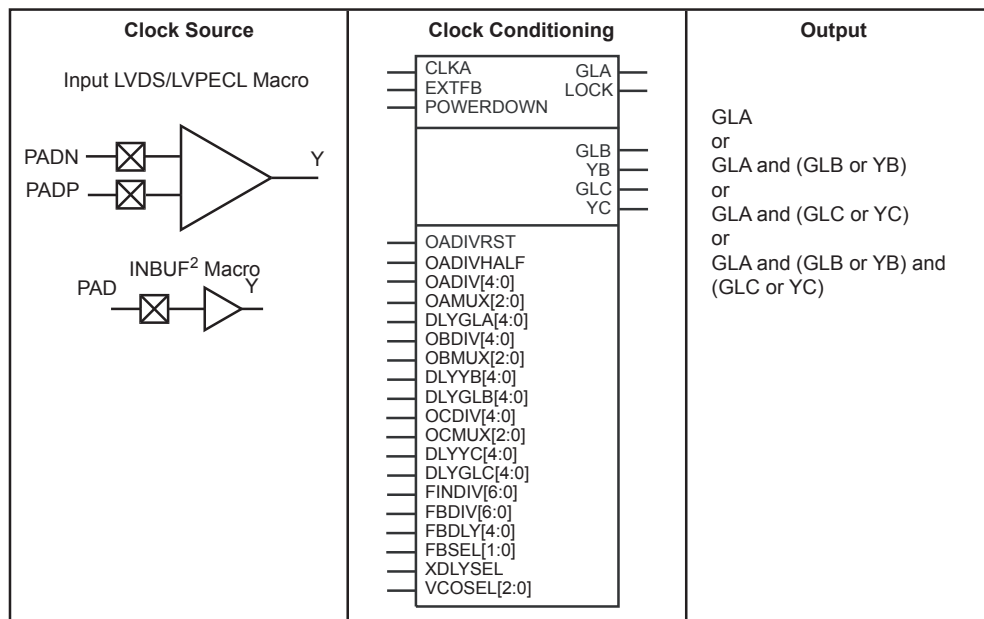where edges are applicable for the particular combinatorial cell

Figure 2-4 •   Combinatorial Timing Model and Waveforms

Notes:

1. Visit the Microsemi SoC Products Group website for application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-27 for signal descriptions.
2. Many specific INBUF macros support the wide variety of single-ended and differential I/O standards for the Fusion family.
3. Refer to the IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide for more information.

Figure 2-19 • **Fusion CCC Options: Global Buffers with the PLL Macro**

Table 2-11 • **Available Selections of I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33[1]
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_LVDS[2]
CLKBUF_LVPECL

Notes:

1. This is the default macro. For more details, refer to the IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide.
2. The B-LVDS and M-LVDS standards are supported with CLKBUF_LVDS.

Table 2-16 • **RTC Control/Status Register**

Bit	Name	Description	Default Value
7	rtc_rst	RTC Reset 1 – Resets the RTC 0 – Deassert reset on after two ACM_CLK cycle.	
6	cntr_en	Counter Enable 1 – Enables the counter; rtc_rst must be deasserted as well. First counter increments after 64 RTCCLK positive edges. 0 – Disables the crystal prescaler but does not reset the counter value. Counter value can only be updated when the counter is disabled.	0
5	vr_en_mat	Voltage Regulator Enable on Match 1 – Enables RTCMATCH and RTCPSMMATCH to output 1 when the counter value equals the Match Register value. This enables the 1.5 V voltage regulator when RTCPSMMATCH connects to the RTCPSMMATCH signal in VRPSM. 0 – RTCMATCH and RTCPSMMATCH output 0 at all times.	0
4:3	xt_mode[1:0]	Crystal Mode Controls RTCXTLMODE[1:0]. Connects to RTC_MODE signal in XTLOSC. XTL_MODE uses this value when xtal_en is 1. See the "Crystal Oscillator" section on page 2-20 for mode configuration.	00
2	rst_cnt_omat	Reset Counter on Match 1 – Enables the sync clear of the counter when the counter value equals the Match Register value. The counter clears on the rising edge of the clock. If all the Match Registers are set to 0, the clear is disabled. 0 – Counter increments indefinitely	0
1	rstb_cnt	Counter Reset, active Low 0 - Resets the 40-bit counter value	0
0	xtal_en	Crystal Enable Controls RTCXTLSEL. Connects to SELMODE signal in XTLOSC. 0 – XTLOSC enables control by FPGA_EN; xt_mode is not used. Sleep mode requires this bit to equal 0. 1 – Enables XTLOSC, XTL_MODE control by xt_mode Standby mode requires this bit to be set to 1. See the "Crystal Oscillator" section on page 2-20 for further details on SELMODE configuration.	0

Program Operation

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, the total programming (including erase) time per page of the eNVM is 6.8 ms. While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified. Program errors include the following:

1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
3. Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in Figure 2-36.

Figure 2-36 • **FB Program Waveform**

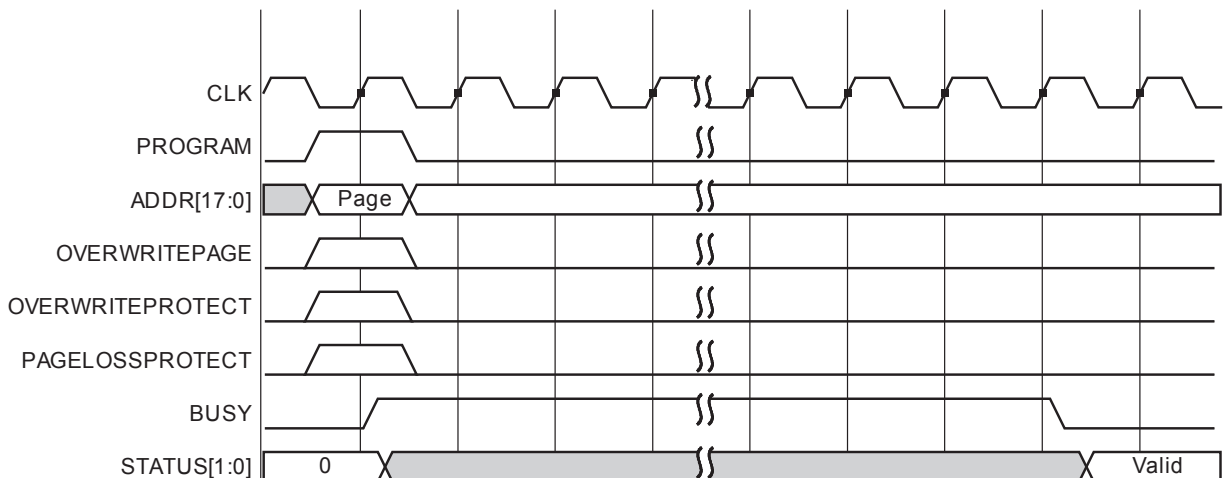Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.
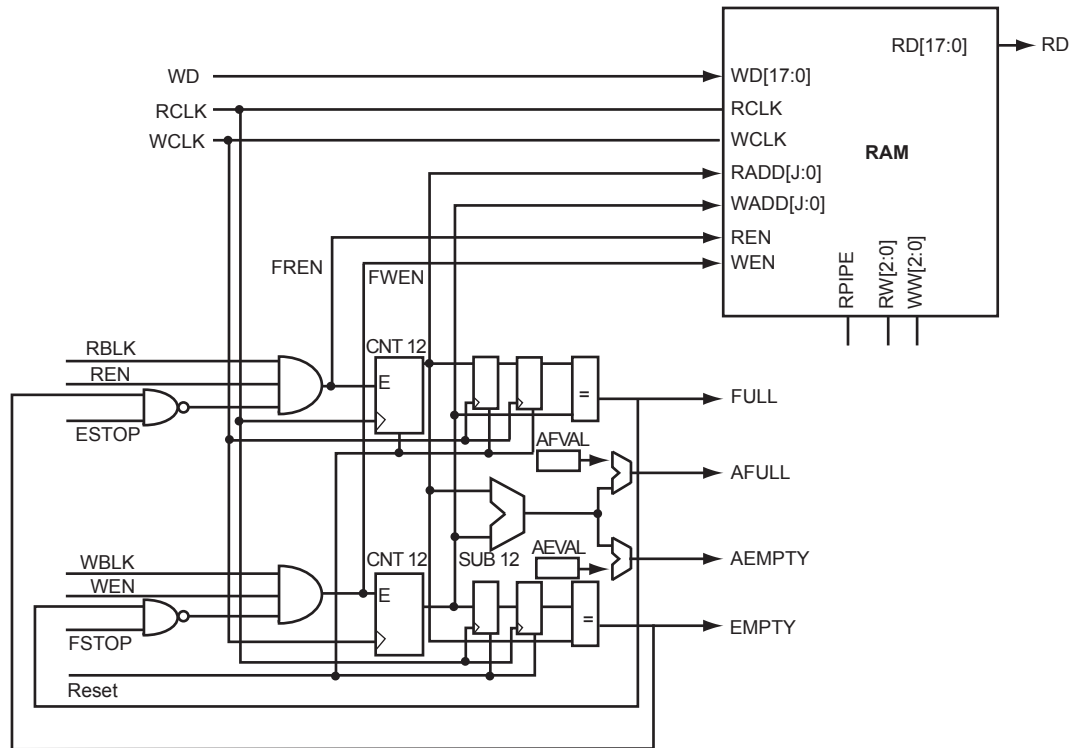

Figure 2-47 • **Fusion RAM Block with Embedded FIFO Controller**

The following signals are used to configure the RAM4K9 memory element.

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-27).

Table 2-27 • **Allowable Aspect Ratio Settings for WIDTHA[1:0]**

WIDTHA1, WIDTHA0	WIDTHB1, WIDTHB0	D×W
00	00	4k×1
01	01	2k×2
10	10	1k×4
11	11	512×9
Note: The aspect ratio settings are constant and cannot be changed on the fly.		

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the corresponding port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write mode for the respective ports. A Low on these signals indicates a write operation, and a High indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A Low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A High indicates a pipelined, read and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A Low on these signals makes the output retain data from the previous read. A High indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the output to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-28).

Table 2-28 • **Address Pins Unused/Used for Various Supported Bus Widths**

D×W	ADDRx	
	Unused	**Used**
4k×1	None	[11:0]
2k×2	[11]	[10:0]
1k×4	[11:10]	[9:0]
512×9	[11:9]	[8:0]

Note: The "x" in ADDRx implies A or B.

FIFO Characteristics
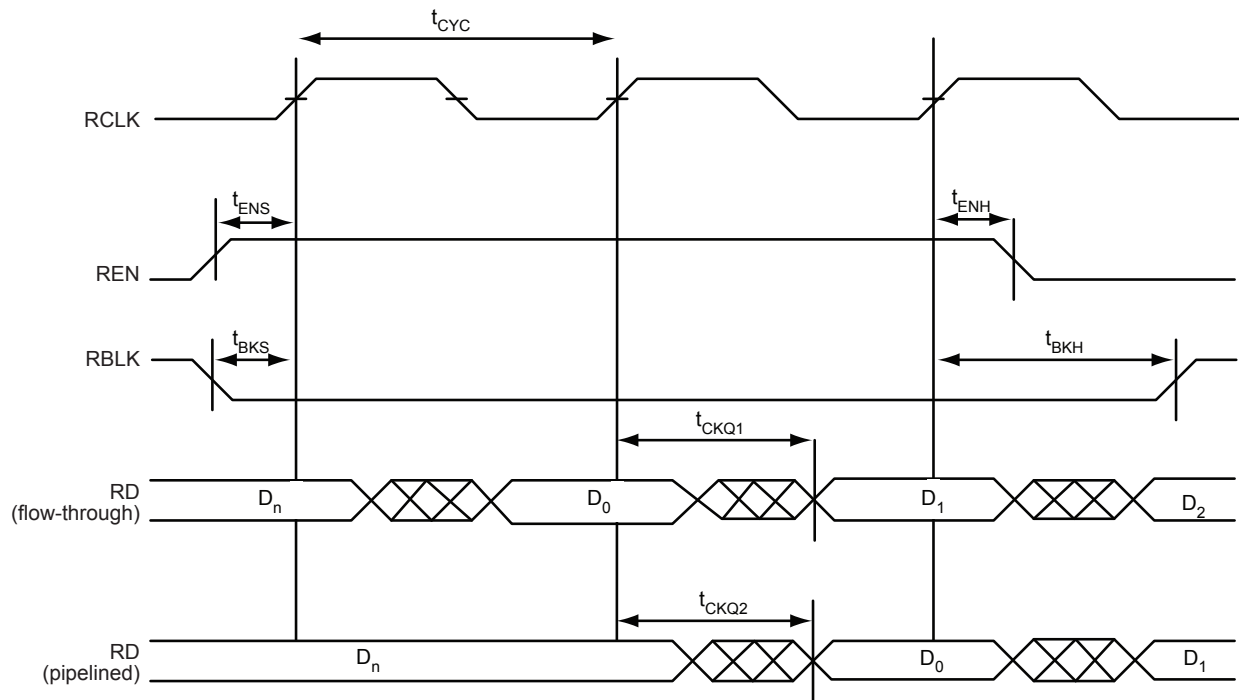
Timing Waveforms
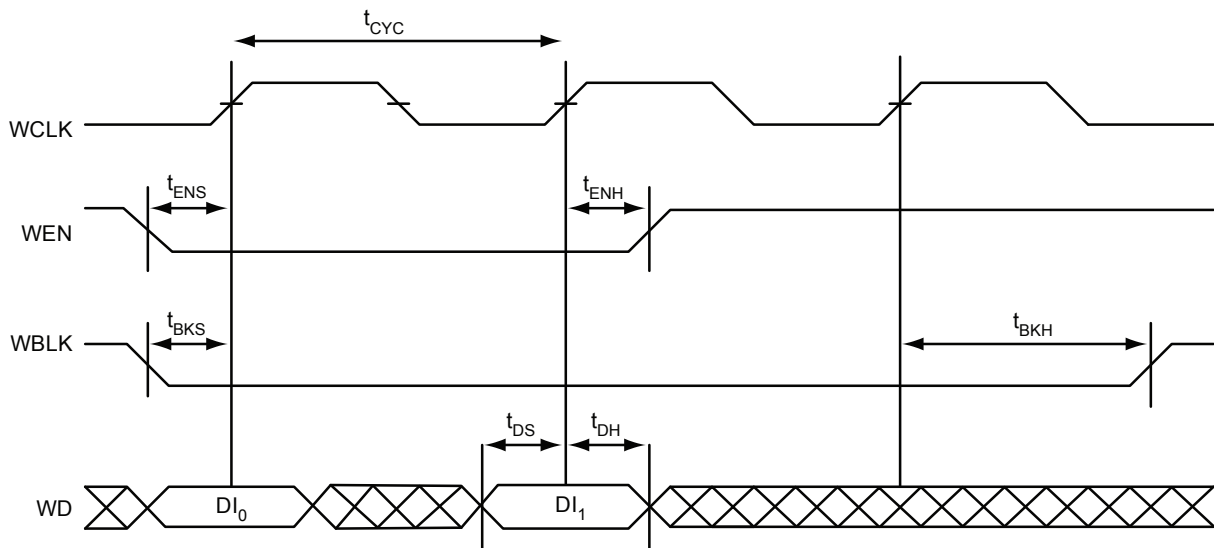

Figure 2-57 • FIFO Read

Figure 2-58 • FIFO Write

Table 2-36 • **Analog Block Pin Description (continued)**

Signal Name	Number of Bits	Direction	Function	Location of Details
AG6	1	Output		Analog Quad
AT6	1	Input		Analog Quad
ATRETURN67	1	Input	Temperature monitor return shared by Analog Quads 6 and 7	Analog Quad
AV7	1	Input	Analog Quad 7	Analog Quad
AC7	1	Input		Analog Quad
AG7	1	Output		Analog Quad
AT7	1	Input		Analog Quad
AV8	1	Input	Analog Quad 8	Analog Quad
AC8	1	Input		Analog Quad
AG8	1	Output		Analog Quad
AT8	1	Input		Analog Quad
ATRETURN89	1	Input	Temperature monitor return shared by Analog Quads 8 and 9	Analog Quad
AV9	1	Input	Analog Quad 9	Analog Quad
AC9	1	Input		Analog Quad
AG9	1	Output		Analog Quad
AT9	1	Input		Analog Quad
RTCMATCH	1	Output	MATCH	RTC
RTCPSMMATCH	1	Output	MATCH connected to VRPSM	RTC
RTCXTLMODE[1:0]	2	Output	Drives XTLOSC RTCMODE[1:0] pins	RTC
RTCXTLSEL	1	Output	Drives XTLOSC MODESEL pin	RTC
RTCCLK	1	Input	RTC clock input	RTC

Analog Quad

With the Fusion family, Microsemi introduces the Analog Quad, shown in Figure 2-65 on page 2-81, as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending it to the ADC for conversion into a digital signal. To maximize the usefulness of the Analog Quad, the analog input signals can also be configured as LVTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block, and its input pin is named AV. It contains a two-channel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler can be configured to accept analog signals between –12 V and 0 or between 0 and +12 V. The prescaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin can also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than 1 Ω) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage that can then be read using the ADC.

ADC Terminology

Conversion Time

Conversion time is the interval between the release of the hold state (imposed by the input circuitry of a track-and-hold) and the instant at which the voltage on the sampling capacitor settles to within one LSB of a new input value.

DNL – Differential Non-Linearity

For an ideal ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB in defined as DNL (Figure 2-83).
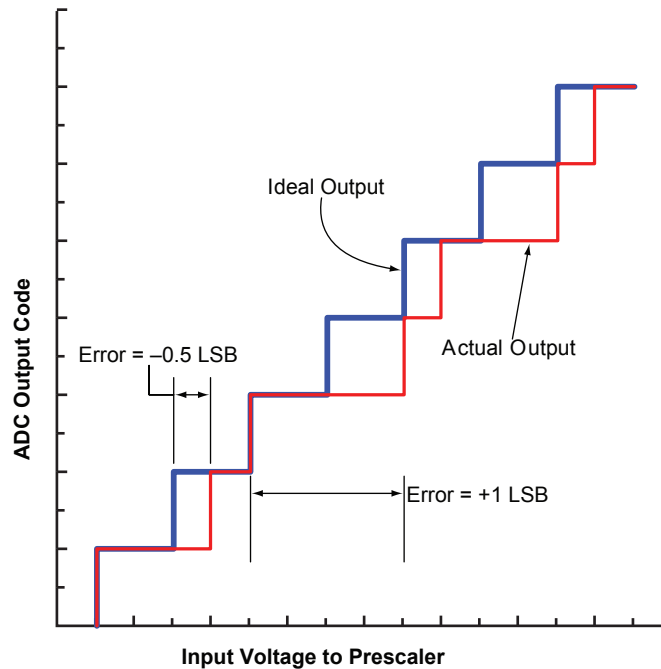
Figure 2-83 • **Differential Non-Linearity (DNL)**

ENOB – Effective Number of Bits

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization of noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD (also see "Signal-to-Noise and Distortion Ratio (SINAD)".) ENOB for a full-scale, sinusoidal input waveform is computed using EQ 12.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

EQ 12

FS Error – Full-Scale Error

Full-scale error is the difference between the actual value that triggers that transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error.

Typical Performance Characteristics

Temperature Errror vs. Die Temperature

Figure 2-94 • **Temperature Error**

Temperature Error vs. Interconnect Capacitance

Figure 2-95 • **Effect of External Sensor Capacitance**

***Table 2-49* •** Analog Channel Specifications (continued)
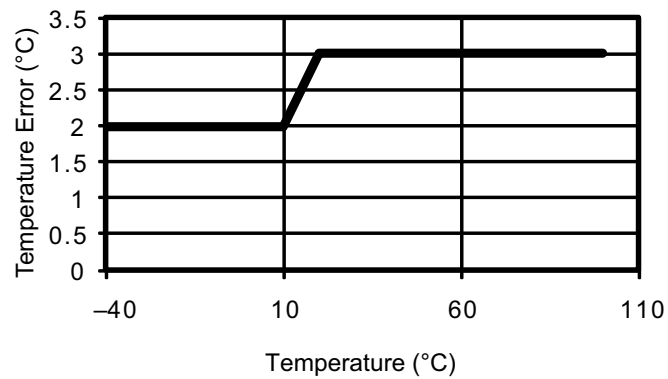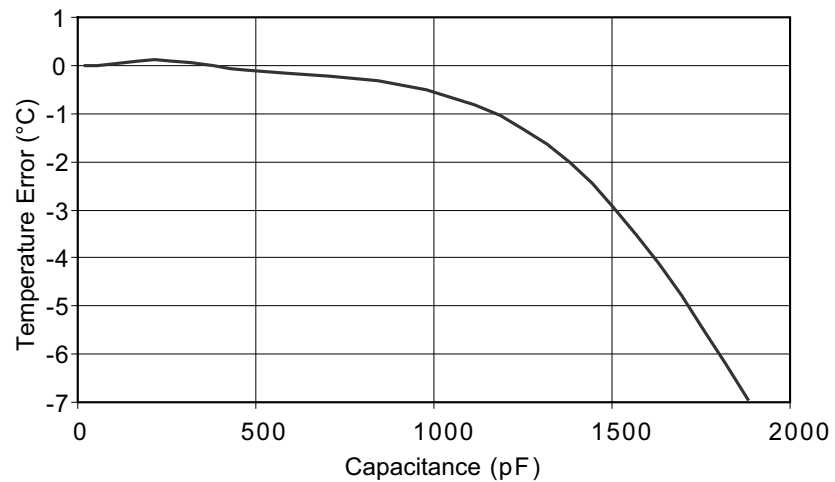Commercial Temperature Range Conditions, T$_J$ = 85°C (unless noted otherwise),
Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Digital Input using Analog Pads AV, AC and AT						
VIND[2,3]	Input Voltage	Refer to Table 3-2 on page 3-3				
VHYSDIN	Hysteresis			0.3		V
VIHDIN	Input High			1.2		V
VILDIN	Input Low			0.9		V
VMPWDIN	Minimum Pulse With		50			ns
F$_{DIN}$	Maximum Frequency				10	MHz
ISTBDIN	Input Leakage Current			2		µA
IDYNDIN	Dynamic Current			20		µA
t$_{INDIN}$	Input Delay			10		ns
Gate Driver Output Using Analog Pad AG						
VG	Voltage Range	Refer to Table 3-2 on page 3-3				
IG	Output Current Drive	High Current Mode[6] at 1.0 V			±20	mA
		Low Current Mode: ±1 µA	0.8	1.0	1.3	µA
		Low Current Mode: ±3 µA	2.0	2.7	3.3	µA
		Low Current Mode: ± 10 µA	7.4	9.0	11.5	µA
		Low Current Mode: ± 30 µA	21.0	27.0	32.0	µA
IOFFG	Maximum Off Current				100	nA
F$_G$	Maximum switching rate	High Current Mode[6] at 1.0 V, 1 kΩ resistive load		1.3		MHz
		Low Current Mode: ±1 µA, 3 MΩ resistive load		3		KHz
		Low Current Mode: ±3 µA, 1 MΩ resistive load		7		KHz
		Low Current Mode: ±10 µA, 300 kΩ resistive load		25		KHz
		Low Current Mode: ±30 µA, 105 kΩ resistive load		78		KHz

Notes:

1. *VRSM is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.*
3. *VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User Guide.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-90 • **Summary of AC Measuring Points**
Applicable to All I/O Bank Types

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-91 • **I/O AC Parameter Definitions**

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Timing Characteristics

Table 2-128 • **1.5 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	−1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	−2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	−1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	−2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
8 mA	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	−1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	−2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
12 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	−1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	−2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-129 • **1.5 V LVCMOS High Slew**
Commercial Temperature Range Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	−1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	−2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	−1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	−2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
8 mA	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	−1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	−2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
12 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	−1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	−2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-165 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
	Min.	Max.	Min.	Max.	Max.	Min.			Max.	Max.		
Drive Strength	V	V	V	V	V	V	mA	mA	mA[3]	mA[3]	μA[4]	μA[4]
21 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*

2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
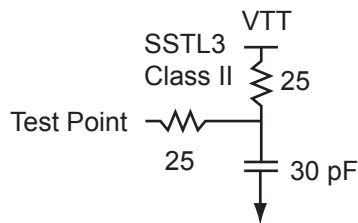
4. *Currents are measured at 85°C junction temperature.*

Figure 2-133 • **AC Loading**

Table 2-166 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_LOAD (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-167 • **SSTL3- Class II**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_DOUT	t_DP	t_DIN	t_PY	t_EOUT	t_ZL	t_ZH	t_LZ	t_HZ	t_ZLS	t_ZHS	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
–1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
–2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

PLL/CCC Contribution—P$_{PLL}$

PLL is not used in this application.

P_{PLL} = 0 W

Nonvolatile Memory—P$_{NVM}$

Nonvolatile memory is not used in this application.

P_{NVM} = 0 W

Crystal Oscillator—P$_{XTL-OSC}$

The application utilizes standby mode. The crystal oscillator is assumed to be active.

Operating Mode

$P_{XTL-OSC}$ = PAC18
$P_{XTL-OSC}$ = 0.63 mW

Standby Mode

$P_{XTL-OSC}$ = PAC18
$P_{XTL-OSC}$ = 0.63 mW

Sleep Mode

$P_{XTL-OSC}$ = 0 W

RC Oscillator—P$_{RC-OSC}$

Operating Mode

P_{RC-OSC} = PAC19
P_{RC-OSC} = 3.30 mW

Standby Mode and Sleep Mode

P_{RC-OSC} = 0 W

Analog System—P$_{AB}$

Number of Quads used: N_{QUADS} = 4

Operating Mode

P_{AB} = PAC20
P_{AB} = 3.00 mW

Standby Mode and Sleep Mode

P_{AB} = 0 W

Total Dynamic Power Consumption—P$_{DYN}$

Operating Mode

P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + $P_{OUTPUTS}$ + P_{MEMORY} + P_{PLL} + P_{NVM}+ $P_{XTL-OSC}$ + P_{RC-OSC} + P_{AB}

P_{DYN} = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P_{DYN} = 143.06 mW

Standby Mode

P_{DYN} = $P_{XTL-OSC}$
P_{DYN} = 0.63 mW

Sleep Mode

P_{DYN} = 0 W

FG256			
Pin Number	**AFS090 Function**	**AFS250 Function**	**AFS600 Function**	**AFS1500 Function**
C7	IO09RSB0V0	IO12RSB0V0	IO06NDB0V0	IO09NDB0V1
C8	IO14RSB0V0	IO22RSB0V0	IO16PDB1V0	IO23PDB1V0
C9	IO15RSB0V0	IO23RSB0V0	IO16NDB1V0	IO23NDB1V0
C10	IO22RSB0V0	IO30RSB0V0	IO25NDB1V1	IO31NDB1V1
C11	IO20RSB0V0	IO31RSB0V0	IO25PDB1V1	IO31PDB1V1
C12	VCCIB0	VCCIB0	VCCIB1	VCCIB1
C13	GBB1/IO28RSB0V0	GBC1/IO35RSB0V0	GBC1/IO26PPB1V1	GBC1/IO40PPB1V2
C14	VCCIB1	VCCIB1	VCCIB2	VCCIB2
C15	GND	GND	GND	GND
C16	VCCIB1	VCCIB1	VCCIB2	VCCIB2
D1	GFC2/IO50NPB3V0	IO75NDB3V0	IO84NDB4V0	IO124NDB4V0
D2	GFA2/IO51NDB3V0	GAB2/IO75PDB3V0	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
D3	GAC2/IO51PDB3V0	IO76NDB3V0	IO85NDB4V0	IO125NDB4V0
D4	GAA2/IO52PDB3V0	GAA2/IO76PDB3V0	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D5	GAB2/IO52NDB3V0	GAB0/IO02RSB0V0	GAB0/IO02NPB0V0	GAB0/IO02NPB0V0
D6	GAC0/IO04RSB0V0	GAC0/IO04RSB0V0	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	IO08RSB0V0	IO13RSB0V0	IO06PDB0V0	IO09PDB0V1
D8	NC	IO20RSB0V0	IO14NDB0V1	IO15NDB0V2
D9	NC	IO21RSB0V0	IO14PDB0V1	IO15PDB0V2
D10	IO21RSB0V0	IO28RSB0V0	IO23PDB1V1	IO37PDB1V2
D11	IO23RSB0V0	GBB0/IO36RSB0V0	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2
D12	NC	NC	VCCIB1	VCCIB1
D13	GBA2/IO31PDB1V0	GBA2/IO40PDB1V0	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
D14	GBB2/IO31NDB1V0	IO40NDB1V0	IO30NDB2V0	IO44NDB2V0
D15	GBC2/IO32PDB1V0	GBB2/IO41PDB1V0	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D16	GCA2/IO32NDB1V0	IO41NDB1V0	IO31NDB2V0	IO45NDB2V0
E1	GND	GND	GND	GND
E2	GFB0/IO48NPB3V0	IO73NDB3V0	IO81NDB4V0	IO118NDB4V0
E3	GFB2/IO50PPB3V0	IO73PDB3V0	IO81PDB4V0	IO118PDB4V0
E4	VCCIB3	VCCIB3	VCCIB4	VCCIB4
E5	NC	IO74NPB3V0	IO83NPB4V0	IO123NPB4V0
E6	NC	IO08RSB0V0	IO04NPB0V0	IO05NPB0V1
E7	GND	GND	GND	GND
E8	NC	IO18RSB0V0	IO08PDB0V1	IO11PDB0V1
E9	NC	NC	IO20NDB1V0	IO27NDB1V1
E10	GND	GND	GND	GND
E11	IO24RSB0V0	GBB1/IO37RSB0V0	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
E12	NC	IO50PPB1V0	IO33PSB2V0	IO48PSB2V0

FG484			FG484		
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
E9	NC	IO08PDB0V1	F22	IO35PDB2V0	IO51PDB2V0
E10	GND	GND	G1	IO77PDB4V0	IO115PDB4V0
E11	IO15NDB1V0	IO22NDB1V0	G2	GND	GND
E12	IO15PDB1V0	IO22PDB1V0	G3	IO78NDB4V0	IO116NDB4V0
E13	GND	GND	G4	IO78PDB4V0	IO116PDB4V0
E14	NC	IO32PPB1V1	G5	VCCIB4	VCCIB4
E15	NC	IO36NPB1V2	G6	NC	IO117PDB4V0
E16	VCCIB1	VCCIB1	G7	VCCIB4	VCCIB4
E17	GND	GND	G8	GND	GND
E18	NC	IO47NPB2V0	G9	IO04NDB0V0	IO06NDB0V1
E19	IO33PDB2V0	IO49PDB2V0	G10	IO04PDB0V0	IO06PDB0V1
E20	VCCIB2	VCCIB2	G11	IO12NDB0V1	IO16NDB0V2
E21	IO32NDB2V0	IO46NDB2V0	G12	IO12PDB0V1	IO16PDB0V2
E22	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0	G13	NC	IO28NDB1V1
F1	IO80NDB4V0	IO118NDB4V0	G14	NC	IO28PDB1V1
F2	IO80PDB4V0	IO118PDB4V0	G15	GND	GND
F3	NC	IO119NSB4V0	G16	NC	IO38PPB1V2
F4	IO84NDB4V0	IO124NDB4V0	G17	NC	IO53PDB2V0
F5	GND	GND	G18	VCCIB2	VCCIB2
F6	VCOMPLA	VCOMPLA	G19	IO36PDB2V0	IO52PDB2V0
F7	VCCPLA	VCCPLA	G20	IO36NDB2V0	IO52NDB2V0
F8	VCCIB0	VCCIB0	G21	GND	GND
F9	IO08NDB0V1	IO12NDB0V1	G22	IO35NDB2V0	IO51NDB2V0
F10	IO08PDB0V1	IO12PDB0V1	H1	IO77NDB4V0	IO115NDB4V0
F11	VCCIB0	VCCIB0	H2	IO76PDB4V0	IO113PDB4V0
F12	VCCIB1	VCCIB1	H3	VCCIB4	VCCIB4
F13	IO22NDB1V0	IO30NDB1V1	H4	IO79NDB4V0	IO114NDB4V0
F14	IO22PDB1V0	IO30PDB1V1	H5	IO79PDB4V0	IO114PDB4V0
F15	VCCIB1	VCCIB1	H6	NC	IO117NDB4V0
F16	NC	IO36PPB1V2	H7	GND	GND
F17	NC	IO38NPB1V2	H8	VCC	VCC
F18	GND	GND	H9	VCCIB0	VCCIB0
F19	IO33NDB2V0	IO49NDB2V0	H10	GND	GND
F20	IO34PDB2V0	IO50PDB2V0	H11	VCCIB0	VCCIB0
F21	IO34NDB2V0	IO50NDB2V0	H12	VCCIB1	VCCIB1

Revision	Changes	Page
v2.0, Revision 1 (continued)	The data in the 2.5 V LCMOS and LVCMOS 2.5 V / 5.0 V rows were updated in Table 2-75 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities.	2-143
	In Table 2-78 • Fusion Standard I/O Standards—OUT_DRIVE Settings, LVCMOS 1.5 V, for OUT_DRIVE 2, was changed from a dash to a check mark.	2-152
	The "VCC15A Analog Power Supply (1.5 V)" definition was changed from "A 1.5 V analog power supply input should be used to provide this input" to "1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry."	2-223
	In the "VCC33PMP Analog Power Supply (3.3 V)" pin description, the following text was changed from "VCC33PMP should be powered up before or simultaneously with VCC33A" to "VCC33PMP should be powered up simultaneously with or after VCC33A."	2-223
	The "VCCOSC Oscillator Power Supply (3.3 V)" section was updated to include information about when to power the pin.	2-223
	In the "128-Bit AES Decryption" section, FIPS-192 was incorrect and changed to FIPS-197.	2-228
	The note in Table 2-84 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications was updated.	2-156
	For 1.5 V LVCMOS, the VIL and VIH parameters, 0.30 * VCCI was changed to 0.35 * VCCI and 0.70 * VCCI was changed to 0.65 * VCCI in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, and Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions. In Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, the VIH max column was updated.	2-164 to 2-165
	Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated to include notes 3 and 4. The temperature ranges were also updated in notes 1 and 2.	2-165
	The titles in Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings to Table 2-94 • Summary of I/O Timing Characteristics – Software Default Settings were updated to "VCCI = I/O Standard Dependent."	2-167 to 2-168
	Below Table 2-98 • I/O Short Currents IOSH/IOSL, the paragraph was updated to change 110°C to 100°C and three months was changed to six months.	2-172
	Table 2-99 • Short Current Event Duration before Failure was updated to remove 110°C data.	2-174
	In Table 2-101 • I/O Input Rise Time, Fall Time, and Related I/O Reliability, LVTTL/LVCMOS rows were changed from 110°C to 100°C.	2-174
	VCC33PMP was added to Table 3-1 • Absolute Maximum Ratings. In addition, conditions for AV, AC, AG, and AT were also updated.	3-1
	VCC33PMP was added to Table 3-2 • Recommended Operating Conditions1. In addition, conditions for AV, AC, AG, and AT were also updated.	3-3
	Table 3-5 • FPGA Programming, Storage, and Operating Limits was updated to include new data and the temperature ranges were changed. The notes were removed from the table.	3-5