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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 252 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-fg676i |

## Array Coordinates

During many place-and-route operations in the Microsemi Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

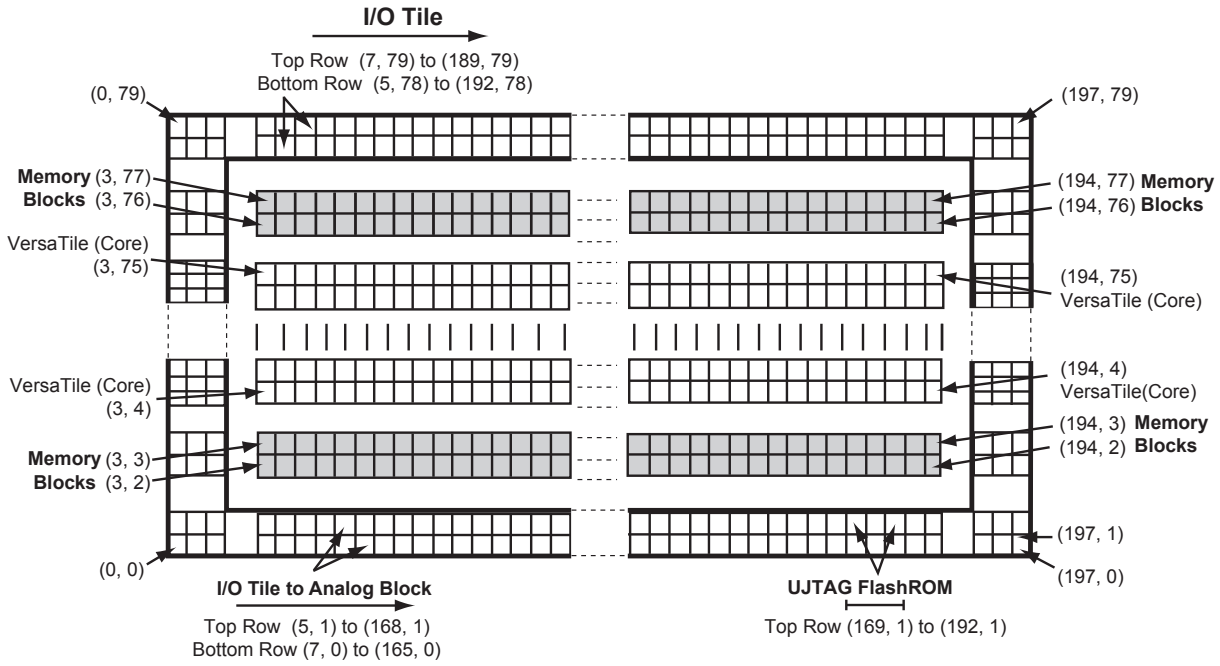
Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

***Table 2-3 •*** **Array Coordinates**

| Device | VersaTiles | | | | Memory Rows | | All | |
|---|---|---|---|---|---|---|---|---|
| | Min. | | Max. | | Bottom | Top | Min. | Max. |
| | x | y | x | y | (x, y) | (x, y) | (x, y) | (x, y) |
| AFS090 | 3 | 2 | 98 | 25 | None | (3, 26) | (0, 0) | (101, 29) |
| AFS250 | 3 | 2 | 130 | 49 | None | (3, 50) | (0, 0) | (133, 53) |
| AFS600 | 3 | 4 | 194 | 75 | (3, 2) | (3, 76) | (0, 0) | (197, 79) |
| AFS1500 | 3 | 4 | 322 | 123 | (3, 2) | (3, 124) | (0, 0) | (325, 129) |




*Note: The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.*

***Figure 2-7 •*** **Array Coordinates for AFS600**

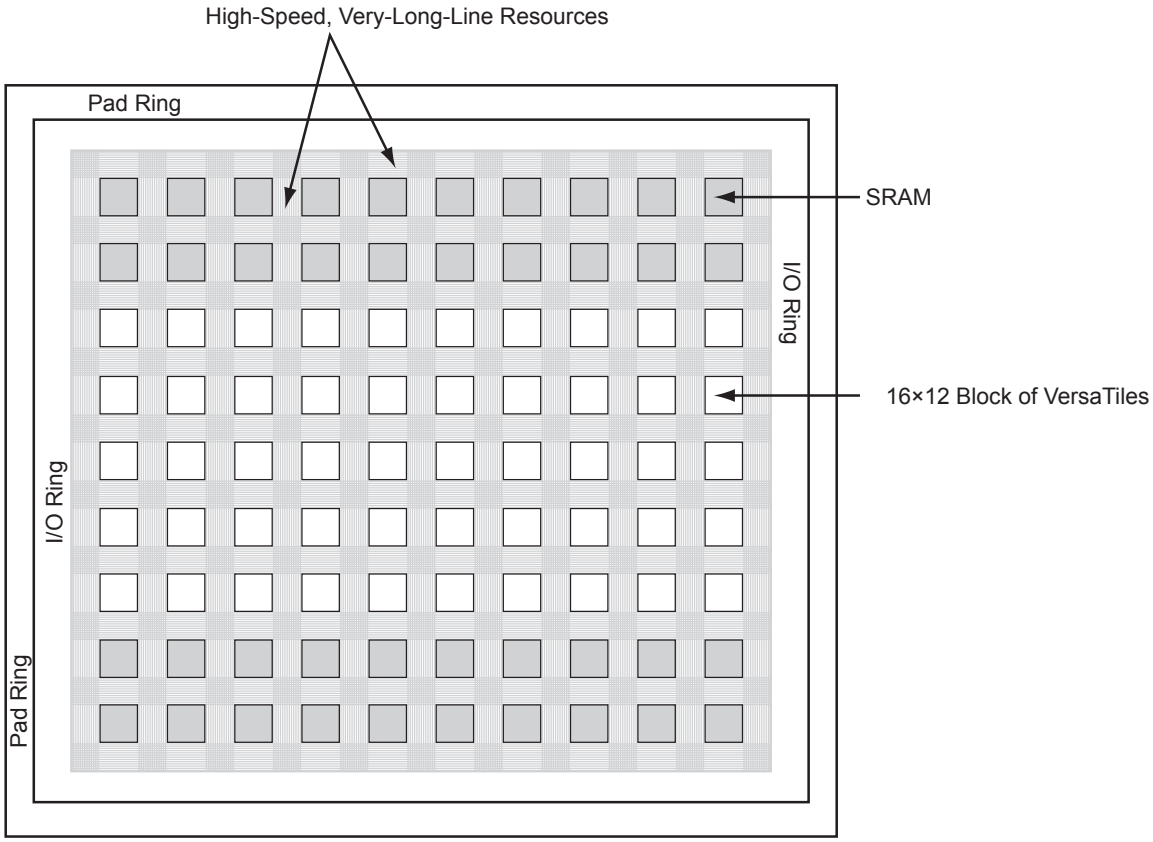



***Figure 2-10 •*** **Very-Long-Line Resources**

### Example: Calculation for Match Count

To put the Fusion device on standby for one hour using an external crystal of 32.768 KHz:

The period of the crystal oscillator is $T_{crystal}$:

$T_{crystal}$ = 1 / 32.768 KHz = 30.518 µs

The period of the counter is $T_{counter}$:

$T_{counter}$ = 30.518 us X 128 = 3.90625 ms

The Match Count for 1 hour is ∆tmatch:

∆tmatch / $T_{counter}$ = (1 hr X 60 min/hr X 60 sec/min) / 3.90625 ms = 921600 or 0xE1000

Using a 32.768 KHz crystal, the maximum standby time of the 40-bit counter is 4,294,967,296 seconds, which is 136 years.

***Table 2-15* • Memory Map for RTC in ACM Register and Description**

| ACMADDR | Register Name | Description | Use | Default Value |
|---|---|---|---|---|
| 0x40 | COUNTER0 | Counter bits 7:0 | Used to preload the counter to a specified start point. | 0x00 |
| 0x41 | COUNTER1 | Counter bits 15:8 | | 0x00 |
| 0x42 | COUNTER2 | Counter bits 23:16 | | 0x00 |
| 0x43 | COUNTER3 | Counter bits 31:24 | | 0x00 |
| 0x44 | COUNTER4 | Counter bits 39:32 | | 0x00 |
| 0x48 | MATCHREG0 | Match register bits 7:0 | The RTC comparison bits | 0x00 |
| 0x49 | MATCHREG1 | Match register bits 15:8 | | 0x00 |
| 0x4A | MATCHREG2 | Match register bits 23:16 | | 0x00 |
| 0x4B | MATCHREG3 | Match register bits 31:24 | | 0x00 |
| 0x4C | MATCHREG4 | Match register bits 39:32 | | 0x00 |
| 0x50 | MATCHBIT0 | Individual match bits 7:0 | The output of the XNOR gates<br>0 – Not matched<br>1 – Matched | 0x00 |
| 0x51 | MATCHBIT1 | Individual match bits 15:8 | | 0x00 |
| 0x52 | MATCHBIT2 | Individual match bits 23:16 | | 0x00 |
| 0x53 | MATCHBIT3 | Individual match bits 31:24 | | 0x00 |
| 0x54 | MATCHBIT4 | Individual match bits 29:32 | | 0x00 |
| 0x58 | CTRL_STAT | Control (write/read) / Status (read only) register bits | Refer to Table 2-16 on page 2-35 for details. | 0x00 |

## Flash Memory Block Diagram

A simplified diagram of the flash memory block is shown in Figure 2-33.

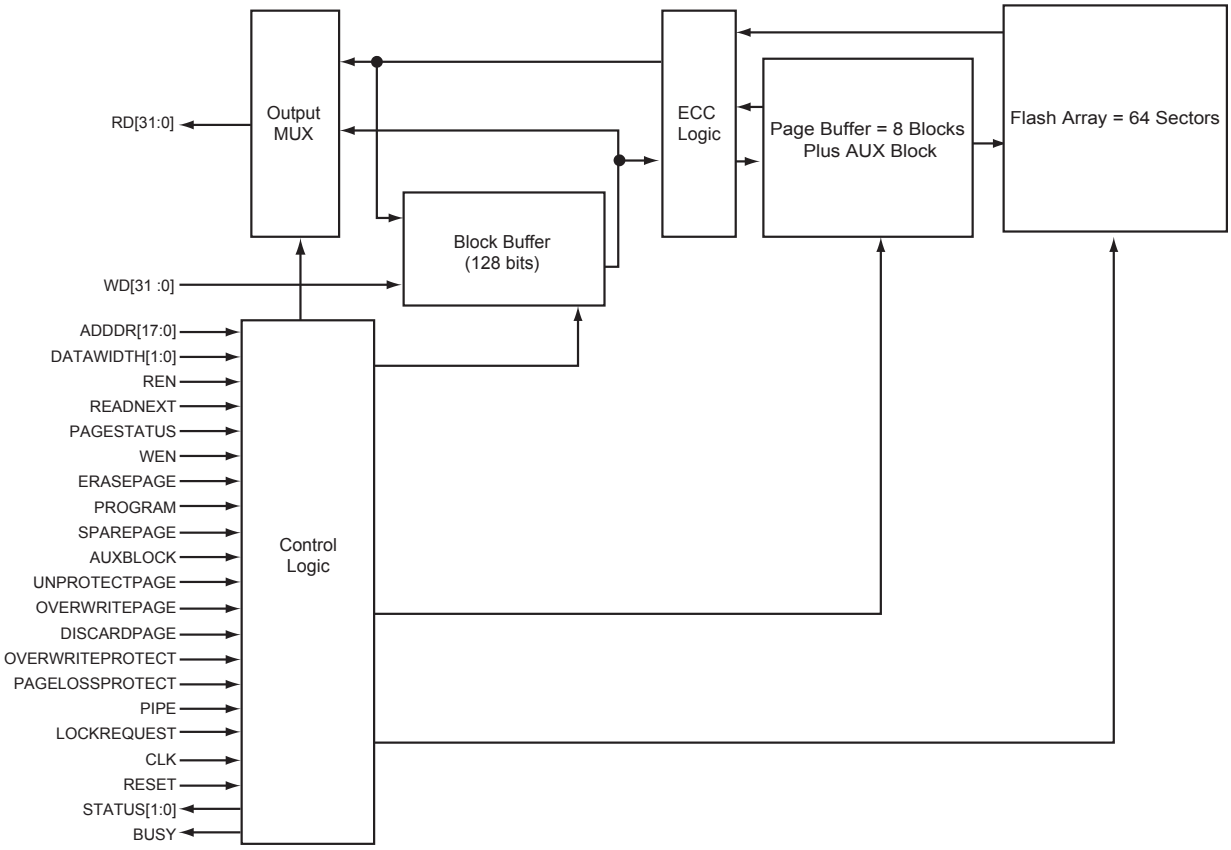



***Figure 2-33 •*** **Flash Memory Block Diagram**

The logic consists of the following sub-blocks:

- Flash Array

  Contains all stored data. The flash array contains 64 sectors, and each sector contains 33 pages of data.
- Page Buffer

  A page-wide volatile register. A page contains 8 blocks of data and an AUX block.
- Block Buffer

  Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic

The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

### Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-37.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')

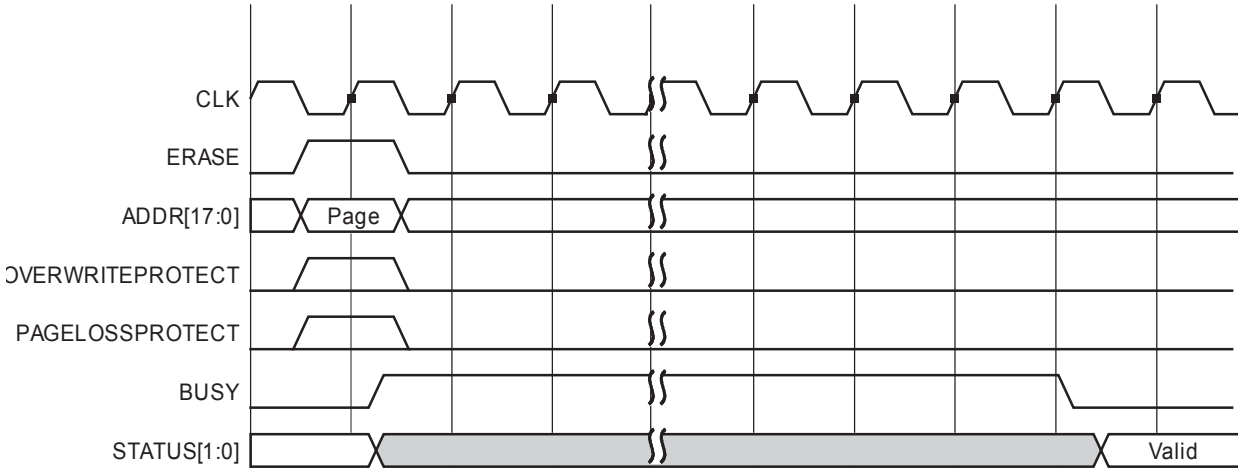



***Figure 2-37 •*** **FB Erase Page Waveform**

The following signals are used to configure the FIFO4K18 memory element.

### WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-33).

***Table 2-33* • Aspect Ratio Settings for WW[2:0]**

| WW2, WW1, WW0 | RW2, RW1, RW0 | D×W |
|---|---|---|
| 000 | 000 | 4k×1 |
| 001 | 001 | 2k×2 |
| 010 | 010 | 1k×4 |
| 011 | 011 | 512×9 |
| 100 | 100 | 256×18 |
| 101, 110, 111 | 101, 110, 111 | Reserved |

### WBLK and RBLK

These signals are active low and will enable the respective ports when Low. When the RBLK signal is High, the corresponding port's outputs hold the previous value.

### WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

### WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

### RPIPE

This signal is used to specify pipelined read on the output. A Low on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

### RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins Low, the FULL and AFULL pins Low, and the EMPTY and AEMPTY pins High (Table 2-34).

***Table 2-34* • Input Data Signal Usage for Different Aspect Ratios**

| D×W | WD/RD Unused |
|---|---|
| 4k×1 | WD[17:1], RD[17:1] |
| 2k×2 | WD[17:2], RD[17:2] |
| 1k×4 | WD[17:4], RD[17:4] |
| 512×9 | WD[17:9], RD[17:9] |
| 256×18 | – |

### WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-34).

### RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-34).

## FIFO Characteristics

### Timing Waveforms

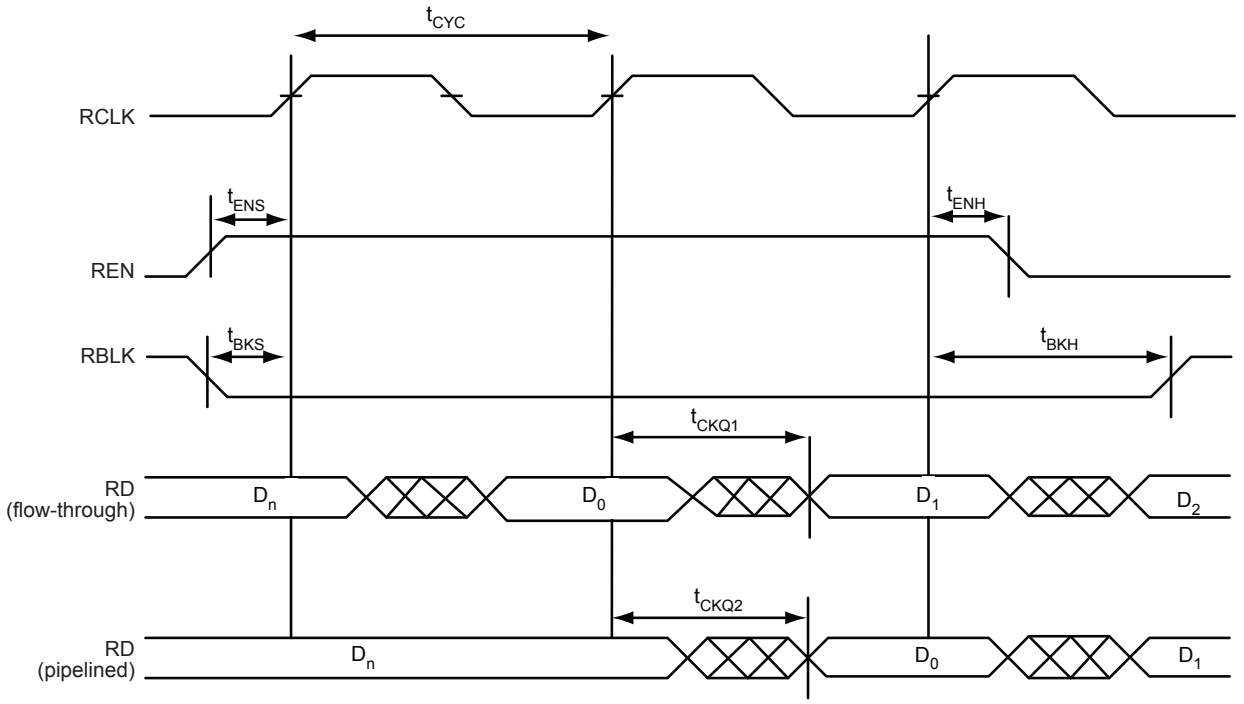



***Figure 2-57 •*** **FIFO Read**

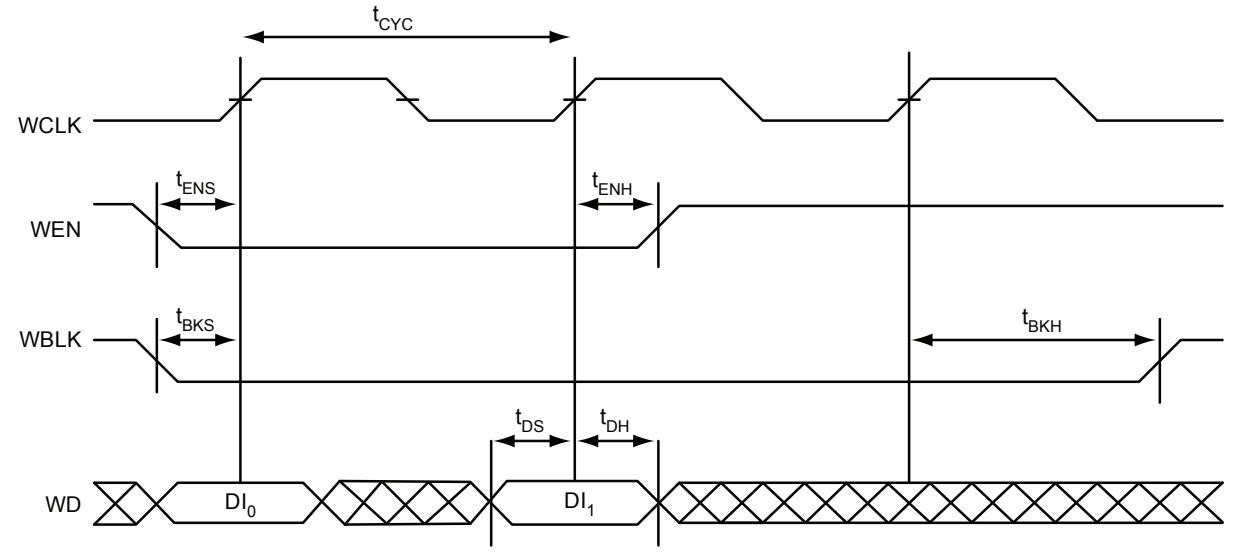



***Figure 2-58 •*** **FIFO Write**

## Analog-to-Digital Converter Block

At the heart of the Fusion analog system is a programmable Successive Approximation Register (SAR) ADC. The ADC can support 8-, 10-, or 12-bit modes of operation. In 12-bit mode, the ADC can resolve 500 ksps. All results are MSB-justified in the ADC. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 2-79. The ADC offers multiple self-calibrating modes to ensure consistent high performance both at power-up and during runtime.

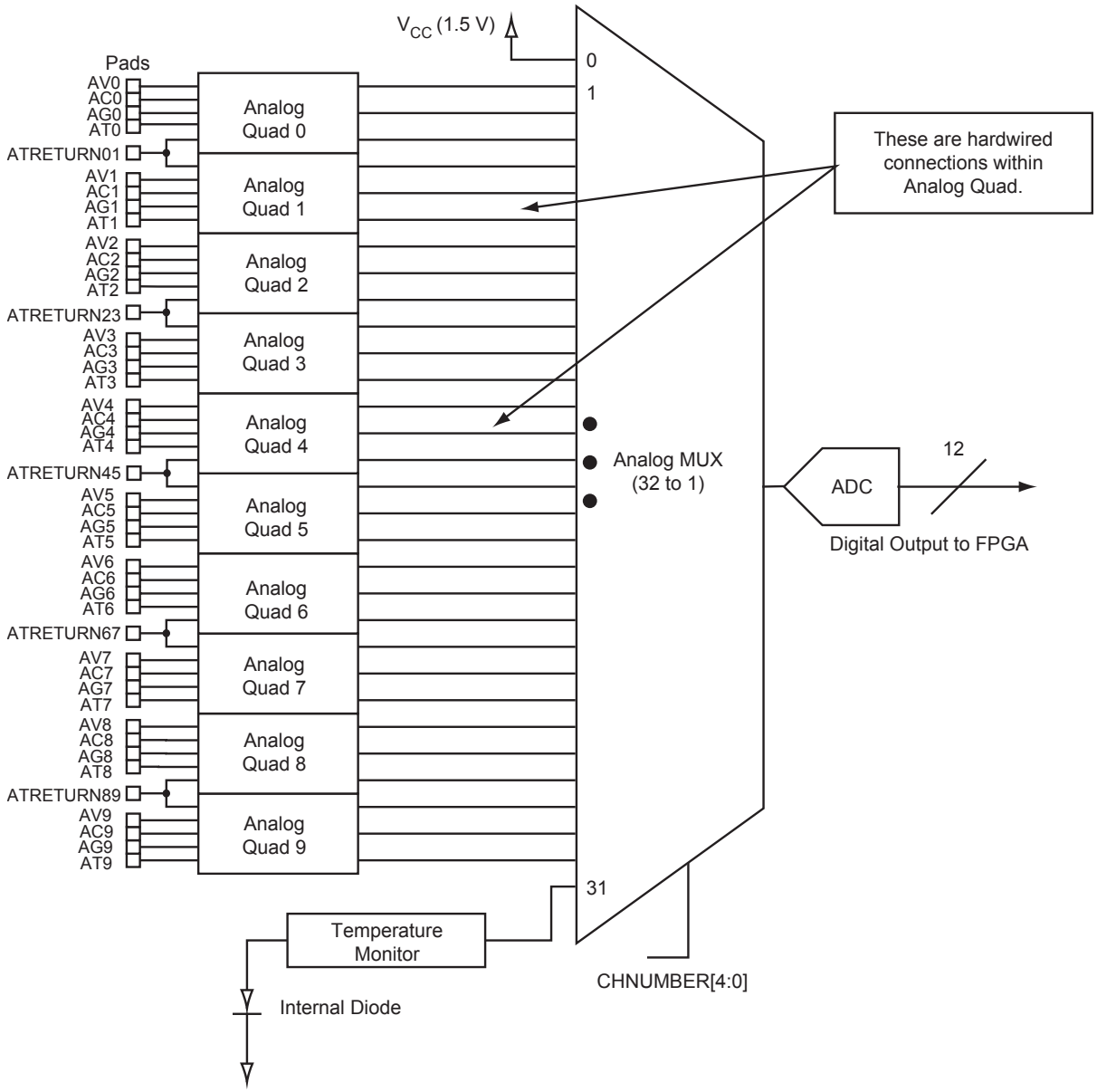



***Figure 2-79 •*** **ADC Block Diagram**

### Integrated Voltage Reference

The Fusion device has an integrated on-chip 2.56 V reference voltage for the ADC. The value of this reference voltage was chosen to make the prescaling and postscaling factors for the prescaler blocks change in a binary fashion. However, if desired, an external reference voltage of up to 3.3 V can be connected between the VAREF and ADCGNDREF pins. The VAREFSEL control pin is used to select the reference voltage.

**Table 2-42 • VAREF Bit Function**

| Name | Bit | Function |
|---|---|---|
| VAREF | 0 | Reference voltage selection<br>0 – Internal voltage reference selected. VAREF pin outputs 2.56 V.<br>1 – Input external voltage reference from VAREF and ADCGNDREF |

### ADC Clock

The speed of the ADC depends on its internal clock, ADCCLK, which is not accessible to users. The ADCCLK is derived from SYSCLK. Input signal TVC[7:0], Time Divider Control, determines the speed of the ADCCLK in relationship to SYSCLK, based on EQ 15.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK}$$

*EQ 15*

TVC: Time Divider Control (0–255)

$t_{ADCCLK}$ is the period of ADCCLK, and must be between 0.5 MHz and 10 MHz

$t_{SYSCLK}$ is the period of SYSCLK

**Table 2-43 • TVC Bits Function**

| Name | Bits | Function |
|---|---|---|
| TVC | [7:0] | SYSCLK divider control |

The frequency of ADCCLK, $f_{ADCCLK}$, must be within 0.5 Hz to 10 MHz.

The inputs to the ADC are synchronized to SYSCLK. A conversion is initiated by asserting the ADCSTART signal on a rising edge of SYSCLK. Figure 2-90 on page 2-112 and Figure 2-91 on page 2-112 show the timing diagram for the ADC.

### Acquisition Time or Sample Time Control

Acquisition time ($t_{SAMPLE}$) specifies how long an analog input signal has to charge the internal capacitor array. Figure 2-88 shows a simplified internal input sampling mechanism of a SAR ADC.

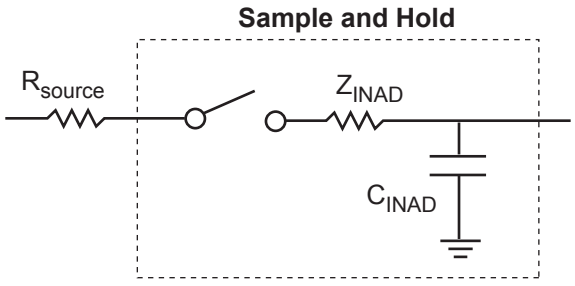



**Figure 2-88 • Simplified Sample and Hold Circuitry**

The internal impedance ($Z_{INAD}$), external source resistance ($R_{SOURCE}$), and sample capacitor ($C_{INAD}$) form a simple RC network. As a result, the accuracy of the ADC can be affected if the ADC is given insufficient time to charge the capacitor. To resolve this problem, you can either reduce the source resistance or increase the sampling time by changing the acquisition time using the STC signal.

### ADC Interface Timing

**Table 2-48 • ADC Interface Timing**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{SUMODE}$ | Mode Pin Setup Time | 0.56 | 0.64 | 0.75 | ns |
| $t_{HDMODE}$ | Mode Pin Hold Time | 0.26 | 0.29 | 0.34 | ns |
| $t_{SUTVC}$ | Clock Divide Control (TVC) Setup Time | 0.68 | 0.77 | 0.90 | ns |
| $t_{HDTVC}$ | Clock Divide Control (TVC) Hold Time | 0.32 | 0.36 | 0.43 | ns |
| $t_{SUSTC}$ | Sample Time Control (STC) Setup Time | 1.58 | 1.79 | 2.11 | ns |
| $t_{HDSTC}$ | Sample Time Control (STC) Hold Time | 1.27 | 1.45 | 1.71 | ns |
| $t_{SUVAREFSEL}$ | Voltage Reference Select (VAREFSEL) Setup Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{HDVAREFSEL}$ | Voltage Reference Select (VAREFSEL) Hold Time | 0.67 | 0.76 | 0.89 | ns |
| $t_{SUCHNUM}$ | Channel Select (CHNUMBER) Setup Time | 0.90 | 1.03 | 1.21 | ns |
| $t_{HDCHNUM}$ | Channel Select (CHNUMBER) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUADCSTART}$ | Start of Conversion (ADCSTART) Setup Time | 0.75 | 0.85 | 1.00 | ns |
| $t_{HDADCSTART}$ | Start of Conversion (ADCSTART) Hold Time | 0.43 | 0.49 | 0.57 | ns |
| $t_{CK2QBUSY}$ | Busy Clock-to-Q | 1.33 | 1.51 | 1.78 | ns |
| $t_{CK2QCAL}$ | Power-Up Calibration Clock-to-Q | 0.63 | 0.71 | 0.84 | ns |
| $t_{CK2QVAL}$ | Valid Conversion Result Clock-to-Q | 3.12 | 3.55 | 4.17 | ns |
| $t_{CK2QSAMPLE}$ | Sample Clock-to-Q | 0.22 | 0.25 | 0.30 | ns |
| $t_{CK2QRESULT}$ | Conversion Result Clock-to-Q | 2.53 | 2.89 | 3.39 | ns |
| $t_{CLR2QBUSY}$ | Busy Clear-to-Q | 2.06 | 2.35 | 2.76 | ns |
| $t_{CLR2QCAL}$ | Power-Up Calibration Clear-to-Q | 2.15 | 2.45 | 2.88 | ns |
| $t_{CLR2QVAL}$ | Valid Conversion Result Clear-to-Q | 2.41 | 2.74 | 3.22 | ns |
| $t_{CLR2QSAMPLE}$ | Sample Clear-to-Q | 2.17 | 2.48 | 2.91 | ns |
| $t_{CLR2QRESULT}$ | Conversion result Clear-to-Q | 2.25 | 2.56 | 3.01 | ns |
| $t_{RECCLR}$ | Recovery Time of Clear | 0.00 | 0.00 | 0.00 | ns |
| $t_{REMCLR}$ | Removal Time of Clear | 0.63 | 0.72 | 0.84 | ns |
| $t_{MPWSYSCLK}$ | Clock Minimum Pulse Width for the ADC | 4.00 | 4.00 | 4.00 | ns |
| $t_{FMAXSYSCLK}$ | Clock Maximum Frequency for the ADC | 100.00 | 100.00 | 100.00 | MHz |

**Table 2-49 • Analog Channel Specifications (continued)**
**Commercial Temperature Range Conditions, $T_J$ = 85°C (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Temperature Monitor Using Analog Pad AT** | | | | | | |
| External Temperature Monitor (external diode 2N3904, $T_J$ = 25°C)[4] | Resolution | 8-bit ADC | | 4 | | °C |
| | | 10-bit ADC | | 1 | | °C |
| | | 12-bit ADC | | 0.25 | | °C |
| | Systematic Offset[5] | AFS090, AFS250, AFS600, AFS1500, uncalibrated[7] | | 5 | | °C |
| | | AFS090, AFS250, AFS600, AFS1500, calibrated[7] | | ±5 | | °C |
| | Accuracy | | | ±3 | ±5 | °C |
| | External Sensor Source Current | High level, TMSTBx = 0 | | 10 | | µA |
| | | Low level, TMSTBx = 1 | | 100 | | µA |
| | Max Capacitance on AT pad | | | | 1.3 | nF |
| Internal Temperature Monitor | Resolution | 8-bit ADC | 4 | | | °C |
| | | 10-bit ADC | 1 | | | °C |
| | | 12-bit ADC | 0.25 | | | °C |
| | Systematic Offset[5] | AFS090[7] | | 5 | | °C |
| | | AFS250, AFS600, AFS1500[7] | | 11 | | °C |
| | Accuracy | | | ±3 | ±5 | °C |
| $t_{TMSHI}$ | Strobe High time | | 10 | | 105 | µs |
| $t_{TMSLO}$ | Strobe Low time | | 5 | | | µs |
| $t_{TMSSET}$ | Settling time | | 5 | | | µs |

*Notes:*

1. *VRSM is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.*
3. *VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User Guide.

## Selectable Skew between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

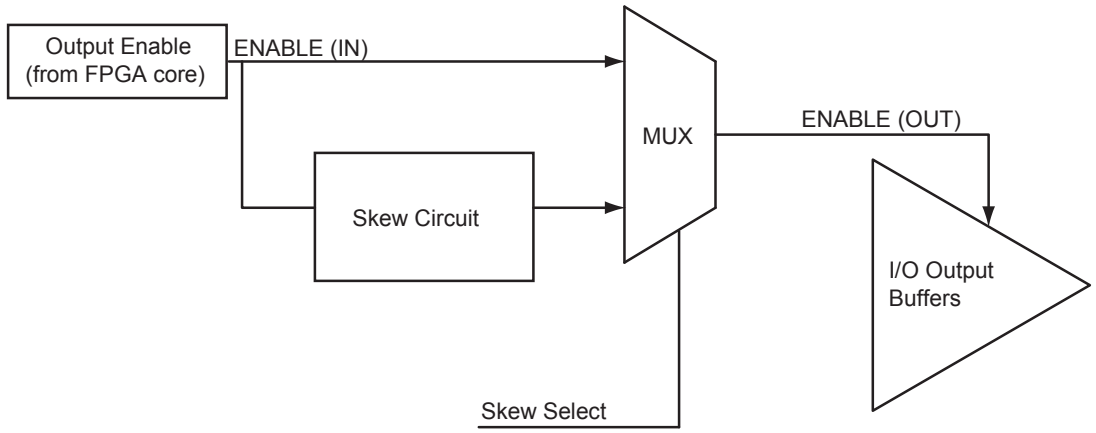



***Figure 2-107* • Block Diagram of Output Enable Path**

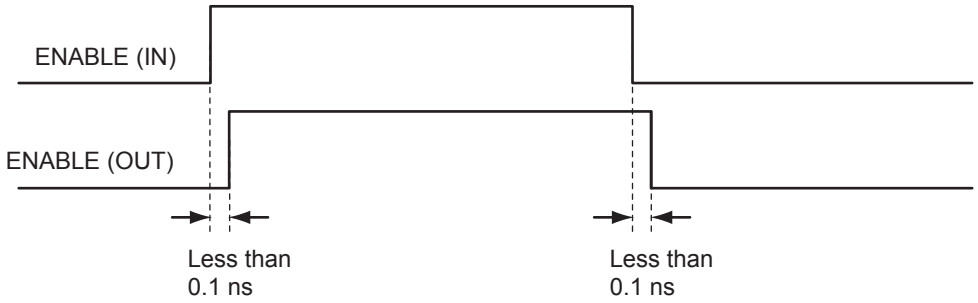



***Figure 2-108* • Timing Diagram (option1: bypasses skew circuit)**

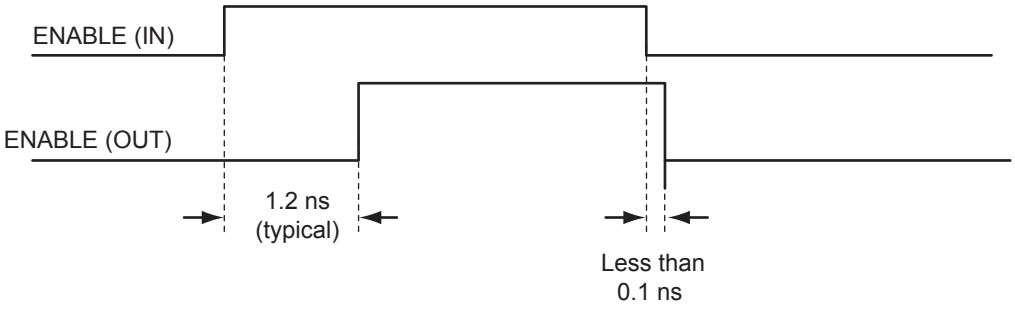
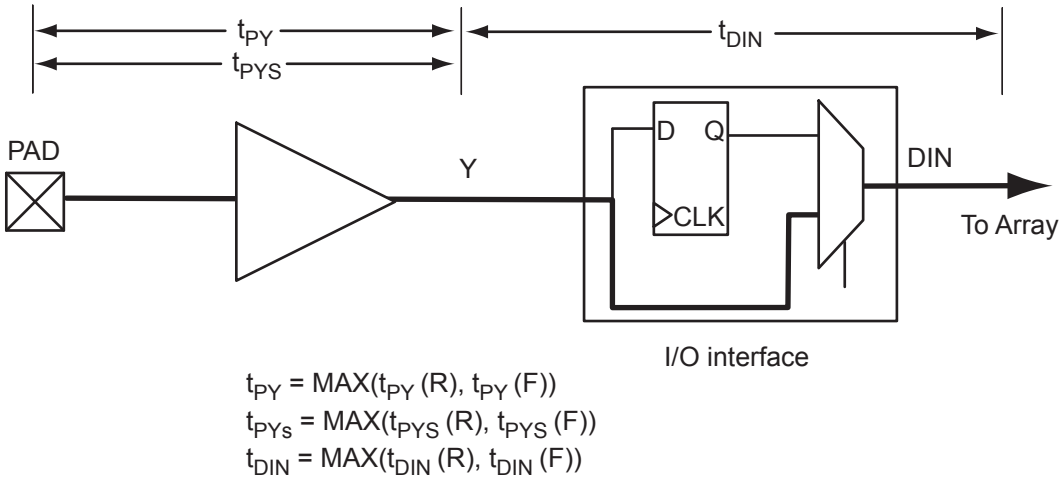



***Figure 2-109* • Timing Diagram (option 2: enables skew circuit)**




$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$
$t_{PYs} = MAX(t_{PYS}(R), t_{PYS}(F))$
$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$

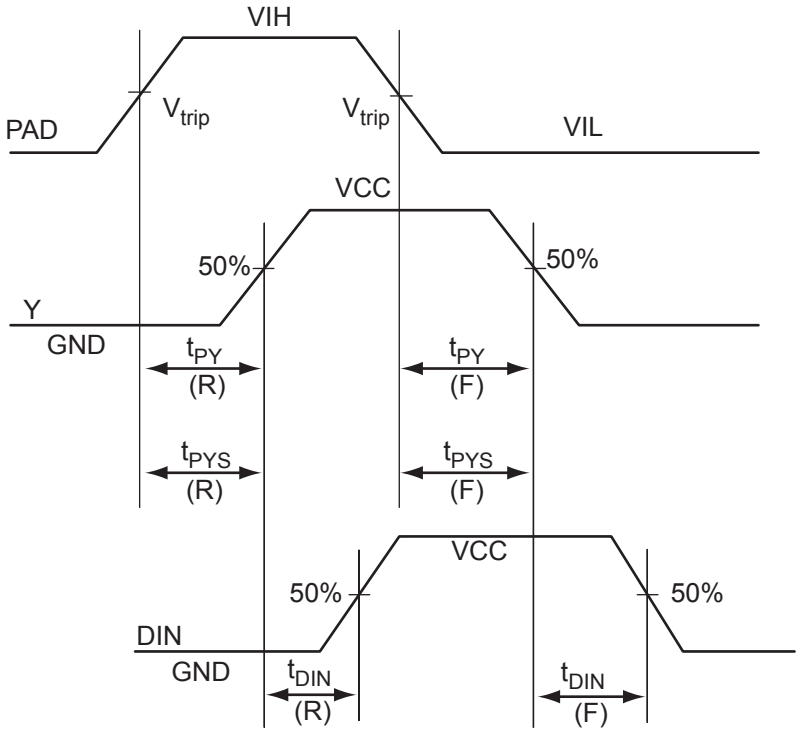



***Figure 2-116* • Input Buffer Timing Model and Delays (example)**

**Table 2-96 • I/O Output Buffer Maximum Resistances [1] (continued)**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (ohms) [2] | $R_{PULL\text{-}UP}$ (ohms) [3] |
|---|---|---|---|
| HSTL (I) | 8 mA | 50 | 50 |
| HSTL (II) | 15 mA | 25 | 25 |
| SSTL2 (I) | 17 mA | 27 | 31 |
| SSTL2 (II) | 21 mA | 13 | 15 |
| SSTL3 (I) | 16 mA | 44 | 69 |
| SSTL3 (II) | 24 mA | 18 | 32 |
| **Applicable to Advanced I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$

## User-Defined Supply Pins

**VREF** **I/O Voltage Reference**

Reference voltage for I/O minibanks. Both AFS600 and AFS1500 (north bank only) support Microsemi Pro I/O. These I/O banks support voltage reference standard I/O. The VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

**VAREF** **Analog Reference Voltage**

The Fusion device can be configured to generate a 2.56 V internal reference voltage that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREF pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF is internally generated by the Fusion device, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. Depending on the capacitor value selected in the Analog System Builder, a tool in Libero SoC, an automatic delay circuit will be generated using logic tiles available within the FPGA to ensure that VAREF has achieved the 2.56 V value. Microsemi recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF need to ensure that a stable and clean VAREF source is supplied to the VAREF pin before initiating conversions by the ADC. Designers should also make sure that the ADCRESET signal is deasserted before initiating valid conversions.[2]

If the user connects VAREF to external 3.3 V on their board, the internal VAREF driving OpAmp tries to bring the pin down to the nominal 2.56 V until the device is programmed and up/functional. Under this scenario, it is recommended to connect an external 3.3 V supply through a ~1 KOhm resistor to limit current, along with placing a 10-100nF capacitor between VAREF and GNDA.

## User Pins

**I/O** **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are configured as inputs with pull-up resistors.

During programming, I/Os become tristated and weakly pulled up to VCCI. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os get instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

**A*xy*** **Analog Input/Output**

Analog I/O pin, where *x* is the analog pad type (C = current pad, G = Gate driver pad, T = Temperature pad, V = Voltage pad) and *y* is the Analog Quad number (0 to 9). There is a minimum 1 MΩ to ground on AV, AC, and AT. This pin can be left floating when it is unused.

2. *The ADC is functional with an external reference down to 1V, however to meet the performance parameters highlighted in the datasheet refer to the VAREF specification in Table 3-2 on page 3-3.*

***Table 3-11 •*** **AFS090 Quiescent Supply Current Characteristics**

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ICC[1] | 1.5 V quiescent current | Operational standby[4], VCC = 1.575 V | $T_J$ = 25°C | | 5 | 7.5 | mA |
| | | | $T_J$ = 85°C | | 6.5 | 20 | mA |
| | | | $T_J$ = 100°C | | 14 | 48 | mA |
| | | Standby mode[5] or Sleep mode[6], $V_{CC}$ = 0 V | | | 0 | 0 | µA |
| ICC33[2] | 3.3 V analog supplies current | Operational standby[4], VCC33 = 3.63 V | $T_J$ = 25°C | | 9.8 | 12 | mA |
| | | | $T_J$ = 85°C | | 9.8 | 12 | mA |
| | | | $T_J$ = 100°C | | 10.7 | 15 | mA |
| | | Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V | $T_J$ = 25°C | | 0.30 | 2 | mA |
| | | | $T_J$ = 85°C | | 0.30 | 2 | mA |
| | | | $T_J$ = 100°C | | 0.45 | 2 | mA |
| | | Standby mode[5], VCC33 = 3.63 V | $T_J$ = 25°C | | 2.9 | 2.9 | mA |
| | | | $T_J$ = 85°C | | 2.9 | 3.0 | mA |
| | | | $T_J$ = 100°C | | 3.5 | 6 | mA |
| | | Sleep mode[6], VCC33 = 3.63 V | $T_J$ = 25°C | | 17 | 18 | µA |
| | | | $T_J$ = 85°C | | 18 | 20 | µA |
| | | | $T_J$ = 100°C | | 24 | 25 | µA |
| ICCI[3] | I/O quiescent current | Operational standby[6], VCCIx = 3.63 V | $T_J$ = 25°C | | 260 | 437 | µA |
| | | | $T_J$ = 85°C | | 260 | 437 | µA |
| | | | $T_J$ = 100°C | | 260 | 437 | µA |
| IJTAG | JTAG I/O quiescent current | Operational standby[4], VJTAG = 3.63 V | $T_J$ = 25°C | | 80 | 100 | µA |
| | | | $T_J$ = 85°C | | 80 | 100 | µA |
| | | | $T_J$ = 100°C | | 80 | 100 | µA |
| | | Standby mode[5] or Sleep mode[6], VJTAG = 0 V | | | 0 | 0 | µA |
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | $T_J$ = 25°C | | 37 | 80 | µA |
| | | | $T_J$ = 85°C | | 37 | 80 | µA |
| | | | $T_J$ = 100°C | | 80 | 100 | µA |
| | | Standby mode[5] or Sleep mode[6], VPUMP = 0 V | | | 0 | 0 | µA |

*Notes:*

1. *ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, and ICCI2.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

# 5 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 6 (March 2014) | Note added for the discontinuance of QN108 and QN180 packages to the "Package I/Os: Single-/Double-Ended (Analog)" table and the "Temperature Grade Offerings" table (SAR 55113, PDN 1306). | II and IV |
| | Updated details about page programming time in the "Program Operation" section (SAR 49291). | 2-46 |
| | ADC_START changed to ADCSTART in the "ADC Operation" section (SAR 44104). | 2-104 |
| Revision 5 (January 2014) | Calibrated offset values (AFS090, AFS250) of the external temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 51464). | 2-117 |
| | Specifications for the internal temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 50870). | 2-117 |
| Revision 4 (January 2013) | The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43177). | III |
| | The note in Table 2-12 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42563). | 2-28 |
| | Table 2-49 • Analog Channel Specifications was modified to update the uncalibrated offset values (AFS250) of the external and internal temperature monitors (SAR 43134). | 2-117 |
| | In Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3), changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 20812). | 2-130 |
| | The values for the Speed Grade (-1 and Std.) for FDDRIMAX (Table 2-180 • Input DDR Propagation Delays) and values for the Speed Grade (-2 and Std.) for FDDOMAX (Table 2-182 • Output DDR Propagation Delays) had been inadvertently interchanged. This has been rectified (SAR 38514). | 2-220, 2-222 |
| | Added description about what happens if a user connects VAREF to an external 3.3 V on their board to the "VAREF Analog Reference Voltage" section (SAR 35188). | 2-225 |
| | Added a note to Table 3-2 • Recommended Operating Conditions1 (SAR 43429): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C. | 3-3 |
| | Added the Package Thermal details for AFS600-PQ208 and AFS250-PQ208 to Table 3-6 • Package Thermal Resistance (SAR 37816). Deleted the Die Size column from the table (SAR 43503). | 3-7 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 42495).<br>Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 3 (August 2012) | Microblade U1AFS250 and U1AFS1500 devices were added to the product tables. | I – IV |
| | A sentence pertaining to the analog I/Os was added to the "Specifying I/O States During Programming" section (SAR 34831). | 1-9 |

| Revision | Changes | Page |
|---|---|---|
| Revision 2 (continued) | The prescalar range for the 'Analog Input (direct input to ADC)" configurations was removed as inapplicable for direct inputs. The input resistance for direct inputs is covered in Table 2-50 • ADC Characteristics in Direct Input Mode (SAR 31201). | 2-120 |
| | The "Examples" for calibrating accuracy for ADC channels were revised and corrected to make them consistent with terminology in the associated tables (SARs 36791, 36773). | 2-124 |
| | A note was added to Table 2-56 • Analog Quad ACM Byte Assignment and the introductory text for Table 2-66 • Internal Temperature Monitor Control Truth Table, stating that for the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set (SAR 34418). | 2-129, 2-131 |
| | $t_{DOUT}$ was corrected to $t_{DIN}$ in Figure 2-116 • Input Buffer Timing Model and Delays (example) (SAR 37115). | 2-161 |
| | The formulas in the table notes for Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34751). | 2-171 |
| | The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34877). | 2-175 |
| | The following notes were removed from Table 2-168 • Minimum and Maximum DC Input and Output Levels (SAR 34808):<br>±5%<br>Differential input voltage = ±350 mV | 2-209 |
| | An incomplete, duplicate sentence was removed from the end of the "GNDAQ Ground (analog quiet)" pin description (SAR 30185). | 2-223 |
| | Information about configuration of unused I/Os was added to the "User Pins" section (SAR 32642). | 2-225 |
| | The following information was added to the pin description for "XTAL1 Crystal Oscillator Circuit Input" and "XTAL2 Crystal Oscillator Circuit Input" (SAR 24119). | 2-227 |
| | The input resistance to ground value in Table 3-3 • Input Resistance of Analog Pads for Analog Input (direct input to ADC), was corrected from 1 MΩ (typical) to 2 kΩ (typical) (SAR 34371). | 3-4 |
| | The Storage Temperature column in Table 3-5 • FPGA Programming, Storage, and Operating Limits stated Min. $T_J$ twice for commercial and industrial product grades and has been corrected to Min. $T_J$ and Max. $T_J$ (SAR 29416). | 3-5 |
| | The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Dynamic Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *Fusion FPGA Fabric User's Guide* (SAR 34741). | 3-24 |
| | Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 36612). | 4-1 |
| July 2010 | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Fusion Device Status" table indicates the status for each device in the device family. | N/A |

| Revision | Changes | Page |
|---|---|---|
| v2.0, Revision 1 (continued) | Table 3-6 • Package Thermal Resistance was updated to include new data. | 3-7 |
| | In EQ 4 to EQ 6, the junction temperature was changed from 110°C to 100°C. | 3-8 to 3-8 |
| | Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics are new and have replaced the Quiescent Supply Current Characteristics (IDDQ) table. | 3-10 to 3-16 |
| | In Table 3-14 • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices, the power supply for PAC9 and PAC10 were changed from VMV/VCC to VCCI. | 3-22 |
| | In Table 3-15 • Different Components Contributing to the Static Power Consumption in Fusion Devices, the power supply for PDC7 and PDC8 were changed from VMV/VCC to VCCI. PDC1 was updated from TBD to 18. | 3-23 |
| | The "QN108" table was updated to remove the duplicates of pins B12 and B34. | 4-2 |
| Preliminary v1.7 (October 2008) | The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible. | |
| | For the VIL and VIH parameters, 0.30 * VCCI was changed to 0.35 * VCCI and 0.70 * VCCI was changed to 0.65 * VCCI in Table 2-126 • Minimum and Maximum DC Input and Output Levels. | 2-193 |
| | The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible. | N/A |
| | The following updates were made to Table 2-141 • Minimum and Maximum DC Input and Output Levels:<br>Temperature Digital Output<br>213 00 1111 1101<br>283 01 0001 1011<br>358 01 0110 0110 – only the digital output was updated. Temperature 358 remains in the temperature column. | 2-200 |
| | In Advance v1.2, the "VAREF Analog Reference Voltage" pin description was significantly updated but the change was not noted in the change table. | 2-225 |
| Advance v1.6 (August 2008) | The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA. | N/A |
| | The references to the *Peripherals User's Guide* in the "No-Glitch MUX (NGMUX)" section and "Voltage Regulator Power Supply Monitor (VRPSM)" section were changed to *Fusion Handbook*. | 2-32, 2-42 |
| Advance v1.5 (July 2008) | The following bullet was updated from High-Voltage Input Tolerance: ±12 V to High-Voltage Input Tolerance: 10.5 V to 12 V. | I |
| | The following bullet was updated from Programmable 1, 3, 10, 30 µA and 25 mA Drive Strengths to Programmable 1, 3, 10, 30 µA and 20 mA Drive Strengths. | I |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.8 (continued) | This sentence was updated in the "No-Glitch MUX (NGMUX)" section to delete GLA:<br>The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). | 2-32 |
| | In Table 2-13 • NGMUX Configuration and Selection Table, 10 and 11 were deleted. | 2-32 |
| | The method to enable sleep mode was updated for bit 0 in Table 2-16 • RTC Control/Status Register. | 2-38 |
| | S2 was changed to D2 in Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access) for RD[31:0] was updated. | 2-51 |
| | The definitions for bits 2 and 3 were updated in Table 2-24 • Page Status Bit Definition. | 2-52 |
| | Figure 2-46 • FlashROM Timing Diagram was updated. | 2-58 |
| | Table 2-26 • FlashROM Access Time is new. | 2-58 |
| | Figure 2-55 • Write Access After Write onto Same Address, Figure 2-56 • Read Access After Write onto Same Address, and Figure 2-57 • Write Access After Read onto Same Address are new. | 2-68–2-70 |
| | Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated. | 2-71, 2-72 |
| | The VAREF and SAMPLE functions were updated in Table 2-36 • Analog Block Pin Description. | 2-82 |
| | The title of Figure 2-72 • Timing Diagram for Current Monitor Strobe was updated to add the word "positive." | 2-91 |
| | The "Gate Driver" section was updated to give information about the switching rate in High Current Drive mode. | 2-94 |
| | The "ADC Description" section was updated to include information about the SAMPLE and BUSY signals and the maximum frequencies for SYSCLK and ADCCLK. EQ 2 was updated to add parentheses around the entire expression in the denominator. | 2-102 |
| | Table 2-46 · Analog Channel Specifications and Table 2-47 · ADC Characteristics in Direct Input Mode were updated. | 2-118, 2-121 |
| | The note was removed from Table 2-55 • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3). | 2-131 |
| | Table 2-63 • Internal Temperature Monitor Control Truth Table is new. | 2-132 |
| | The "Cold-Sparing Support" section was updated to add information about cases where current draw can occur. | 2-143 |
| | Figure 2-104 • Solution 4 was updated. | 2-147 |
| | Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings was updated. | 2-153 |
| | The "GNDA Ground (analog)" section and "GNDAQ Ground (analog quiet)" section were updated to add information about maximum differential voltage. | 2-224 |
| | The "$V_{AREF}$ Analog Reference Voltage" section and "VPUMP Programming Supply Voltage" section were updated. | 2-226 |
| | The "$V_{CCPLA/B}$ PLL Supply Voltage" section was updated to include information about the east and west PLLs. | 2-225 |
| | The $V_{COMPLF}$ pin description was deleted. | N/A |
| | The "Axy Analog Input/Output" section was updated with information about grounding and floating the pin. | 2-226 |