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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-fgg484

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VersaNet Global Networks and Spine Access

The Fusion architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles on the Fusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 180 internal/external clocks (in an AFS1500 device) or other high-fanout nets in Fusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on Fusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-12 on page 2-12).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the Fusion device (the "scope" of the spine; see Figure 2-11 on page 2-11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device. For details on using spines in Fusion devices, see the application note *Using Global Resources in Actel Fusion Devices*.

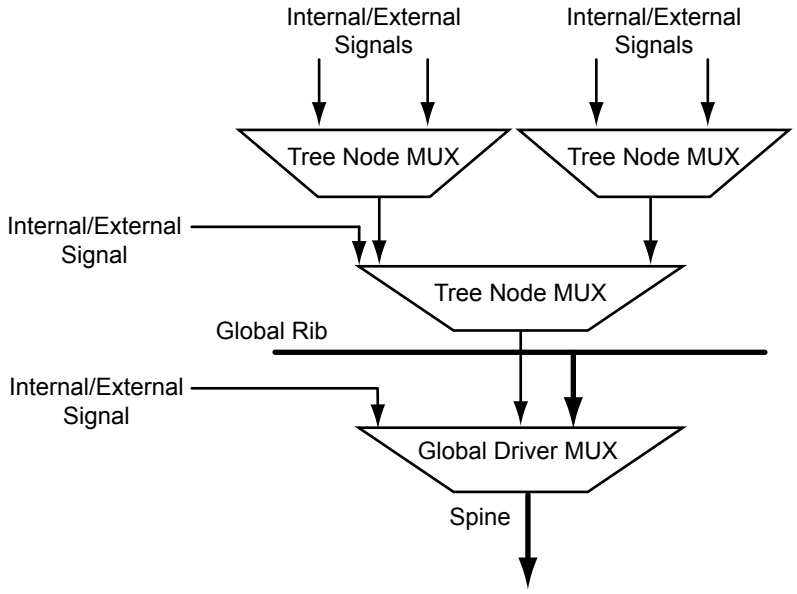


Figure 2-13 • **Spine-Selection MUX of Global Tree**

Crystal Oscillator

The Crystal Oscillator (XTLOSC) is source that generates the clock from an external crystal. The output of XTLOSC CLKOUT signal can be selected as an input to the PLL. Refer to the "Clock Conditioning Circuits" section for more details. The XTLOSC can operate in normal operations and Standby mode (RTC is running and 1.5 V is not present).

In normal operation, the internal FPGA_EN signal is '1' as long as 1.5 V is present for VCC. As such, the internal enable signal, XTL_EN, for Crystal Oscillator is enabled since FPGA_EN is asserted. The XTL_MODE has the option of using MODE or RTC_MODE, depending on SELMODE.

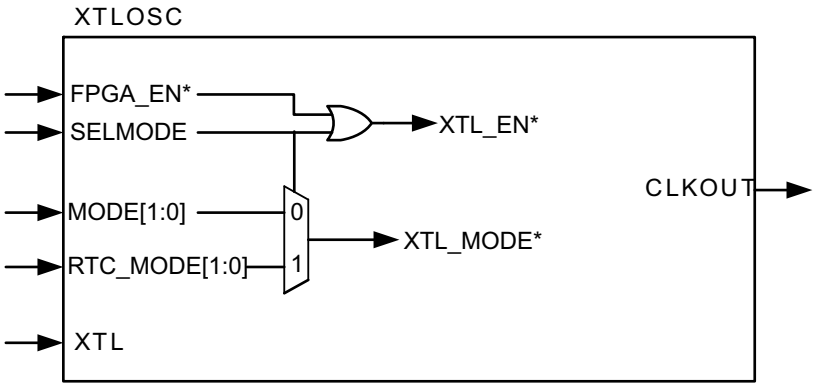
During Standby, 1.5 V is not available, as such, and FPGA_EN is '0'. SELMODE must be asserted in order for XTL_EN to be enabled; hence XTL_MODE relies on RTC_MODE. SELMODE and RTC_MODE must be connected to RTCXTLSEL and RTCXTLMODE from the AB respectively for correct operation during Standby (refer to the "Real-Time Counter System" section on page 2-31 for a detailed description).

The Crystal Oscillator can be configured in one of four modes:

- RC network, 32 KHz to 4 MHz
- Low gain, 32 to 200 KHz
- Medium gain, 0.20 to 2.0 MHz
- High gain, 2.0 to 20.0 MHz

In RC network mode, the XTAL1 pin is connected to an RC circuit, as shown in Figure 2-16 on page 2-18. The XTAL2 pin should be left floating. The RC value can be chosen based on Figure 2-18 for any desired frequency between 32 KHz and 4 MHz. The RC network mode can also accommodate an external clock source on XTAL1 instead of an RC circuit.

In Low gain, Medium gain, and High gain, an external crystal component or ceramic resonator can be added onto XTAL1 and XTAL2, as shown in Figure 2-16 on page 2-18. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.



*Note: *Internal signal—does not exist in macro.*

Figure 2-17 • **XTLOSC Macro**

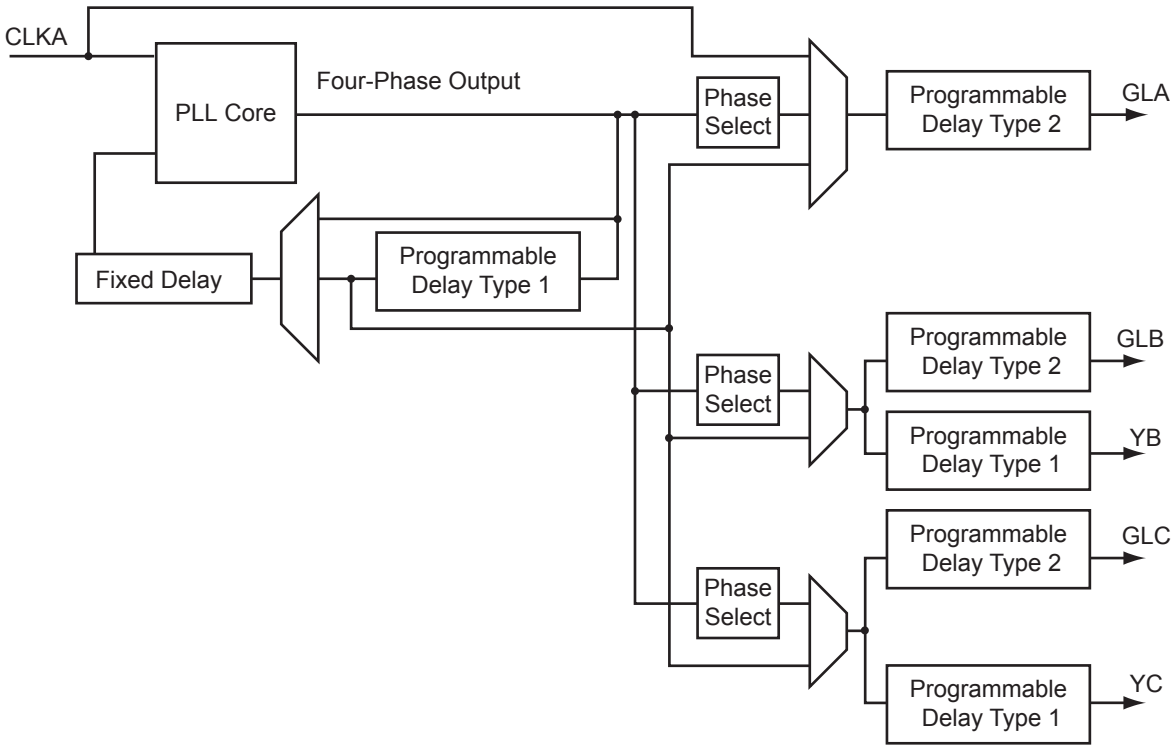
CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • **PLL Block**

Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-37.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')

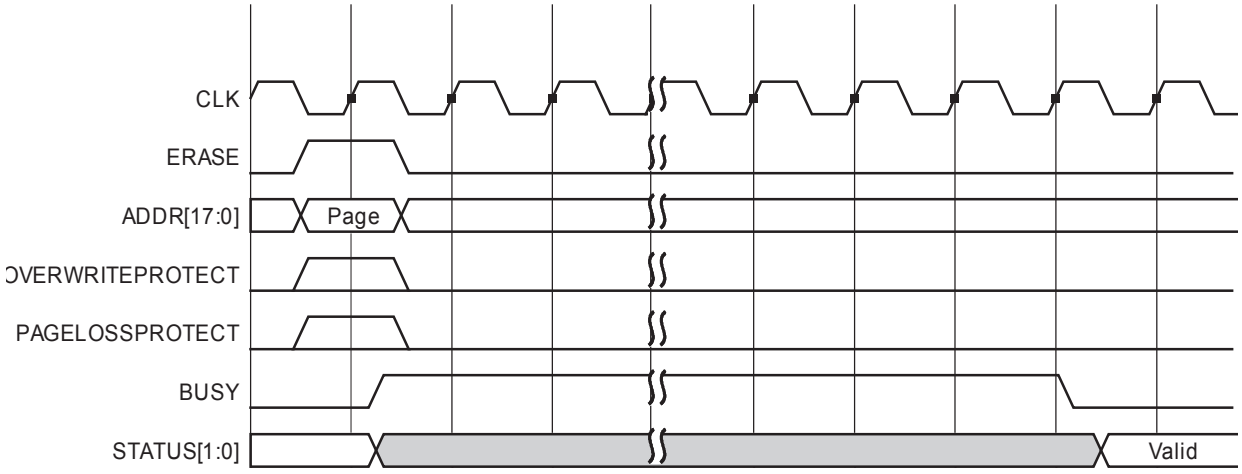


Figure 2-37 • **FB Erase Page Waveform**

Read Operation

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer, or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-38) and Pipe Mode (Figure 2-39) reads of the flash memory block interface.

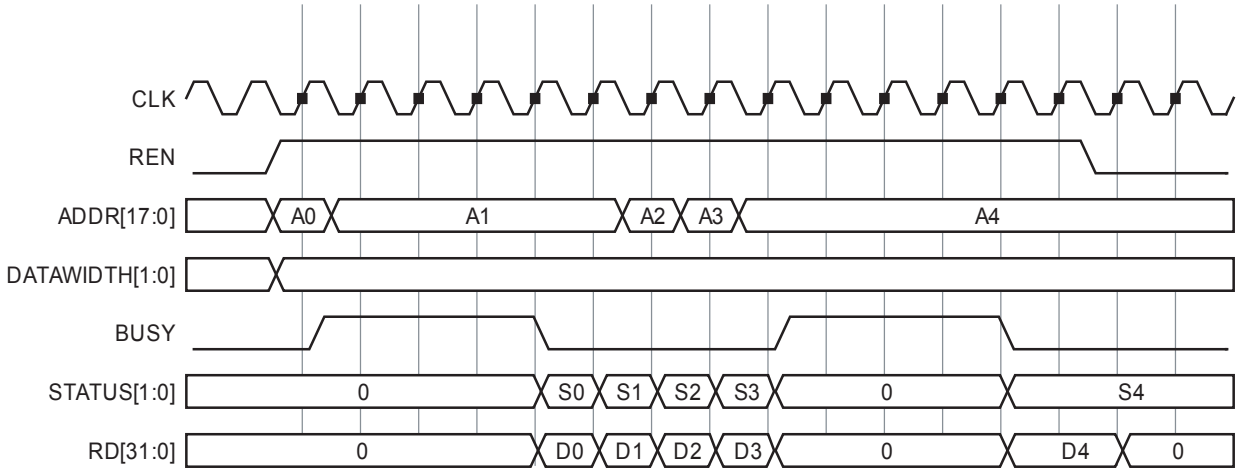


Figure 2-38 • **Read Waveform (Non-Pipe Mode, 32-bit access)**

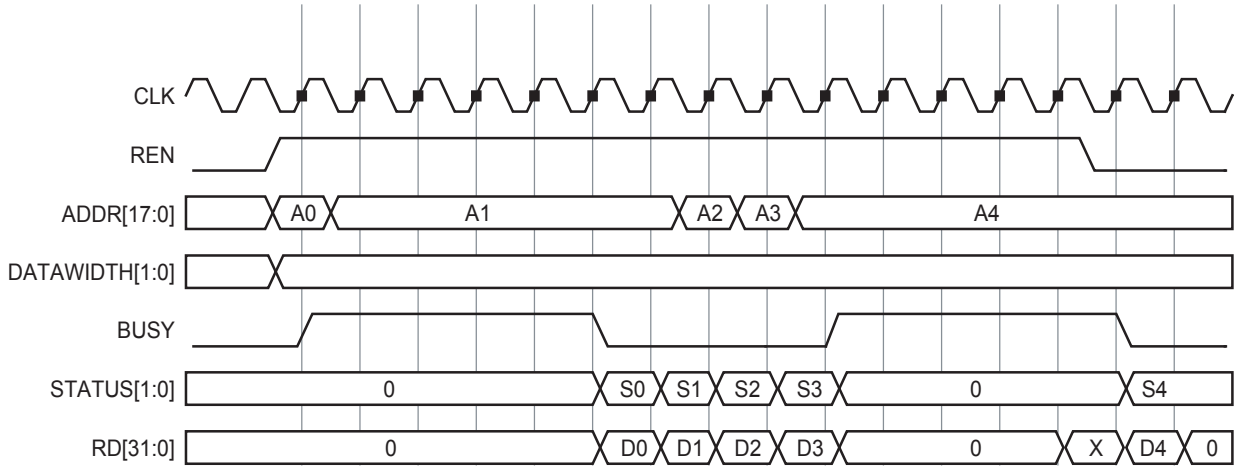


Figure 2-39 • **Read Waveform (Pipe Mode, 32-bit access)**

Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-40 and Figure 2-41.

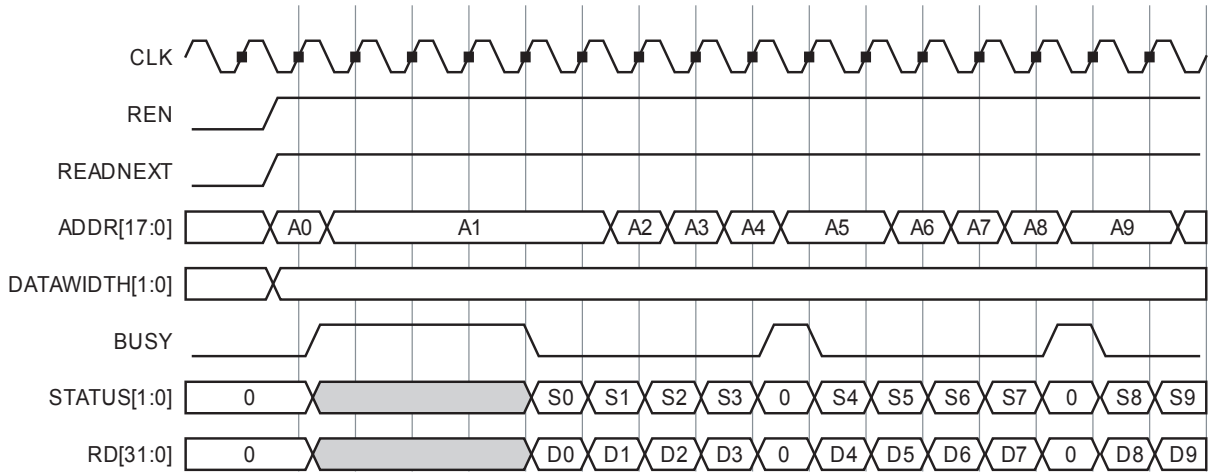


***Figure 2-40* • Read Next Waveform (Non-Pipe Mode, 32-bit access)**

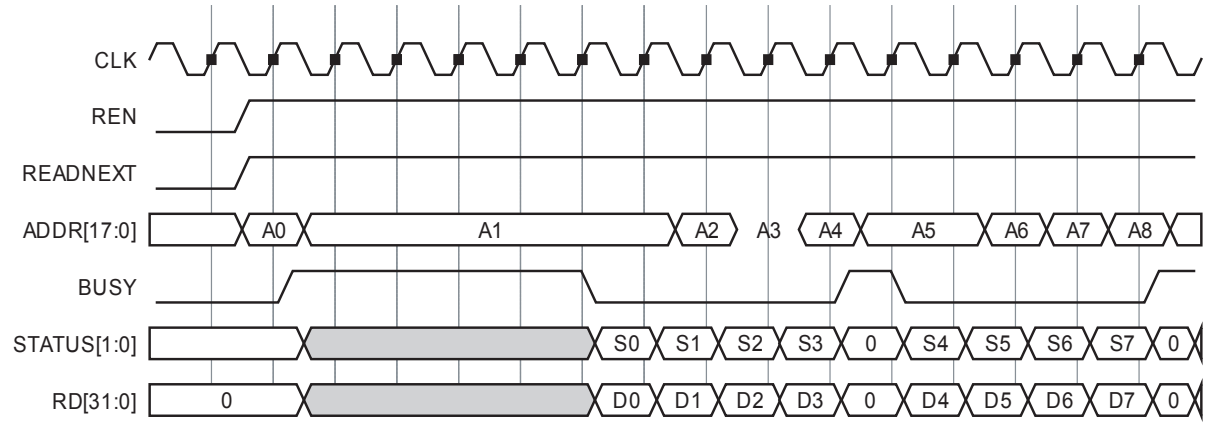


***Figure 2-41* • Read Next WaveForm (Pipe Mode, 32-bit access)**

***Table 2-32* • RAM512X18**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.10	0.12	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.59	0.50	0.44	ns
t_{RSTBQ}[1]	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

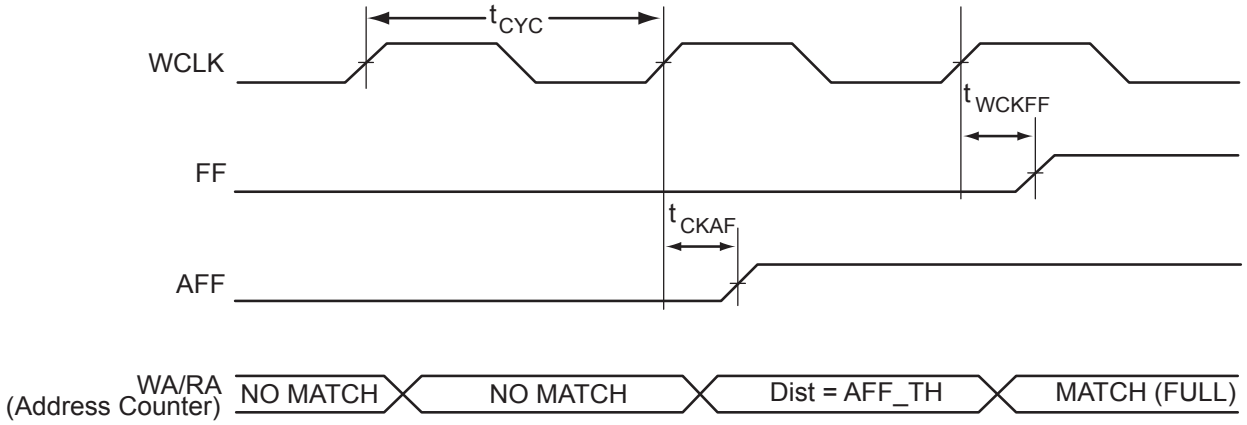


Figure 2-61 • **FIFO FULL and AFULL Flag Assertion**

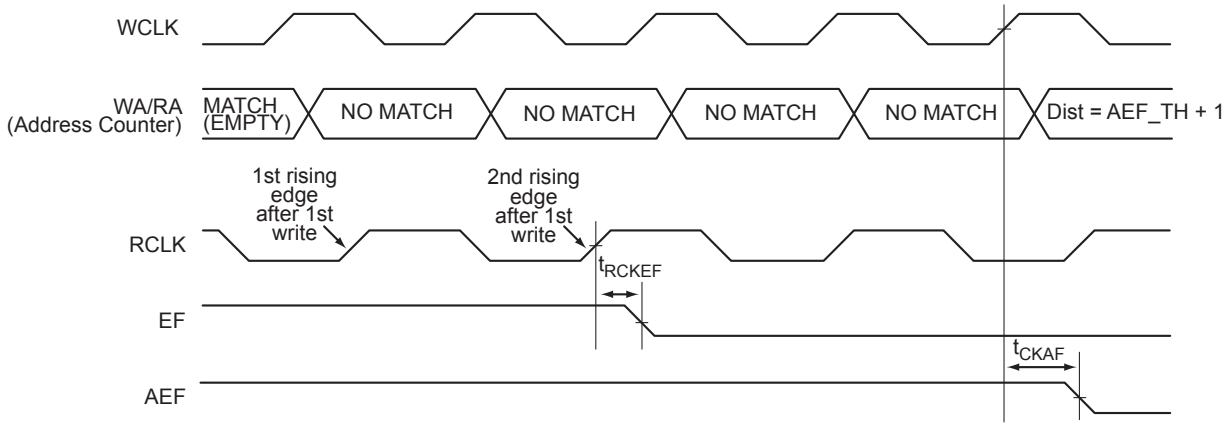


Figure 2-62 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

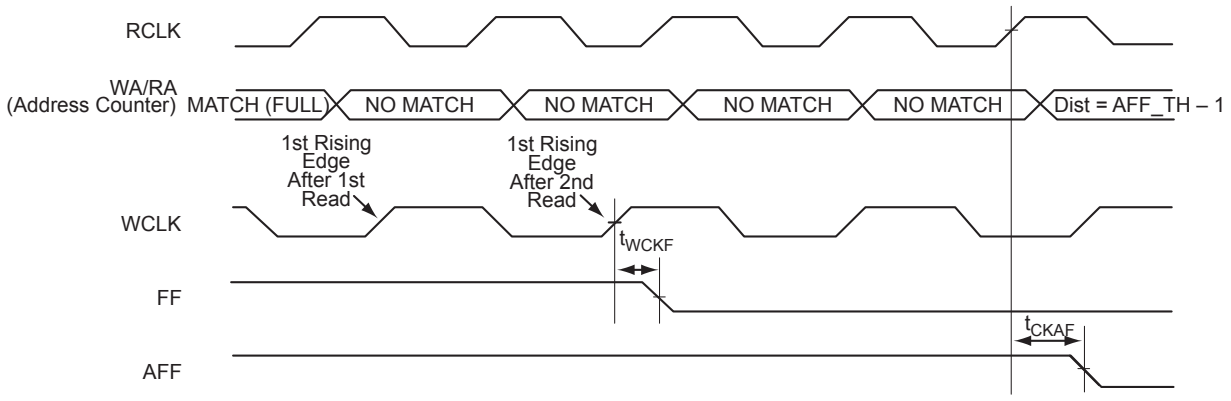


Figure 2-63 • **FIFO FULL Flag and AFULL Flag Deassertion**

Typical scaling factors are given in Table 2-57 on page 2-130, and the gain error (which contributes to the minimum and maximum) is in Table 2-49 on page 2-117.

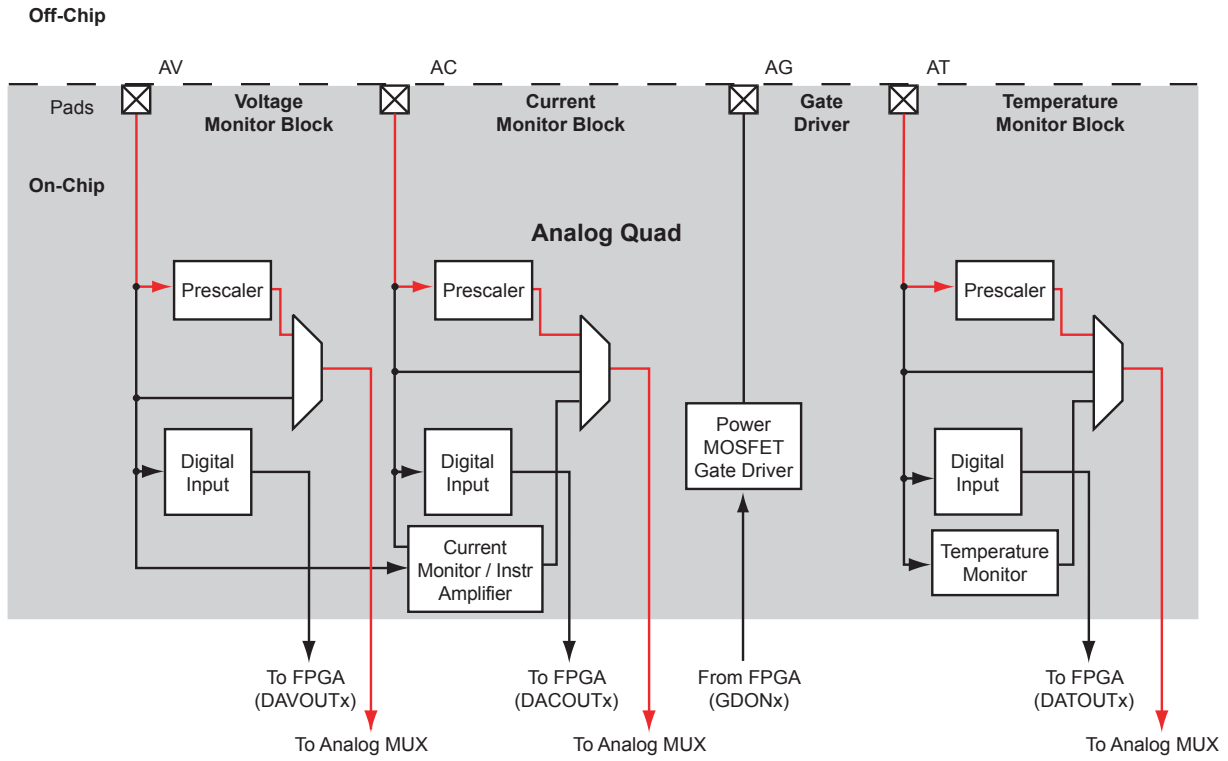


Figure 2-67 • **Analog Quad Prescaler Input Configuration**

Terminology

BW – Bandwidth

BW is a range of frequencies that a Channel can handle.

Channel

A channel is define as an analog input configured as one of the Prescaler range shown in Table 2-57 on page 2-130. The channel includes the Prescaler circuit and the ADC.

Channel Gain

Channel Gain is a measured of the deviation of the actual slope from the ideal slope. The slope is measured from the 20% and 80% point.

$$\text{Gain} = \frac{\text{Gain}_{\text{actual}}}{\text{Gain}_{\text{ideal}}}$$

EQ 1

Channel Gain Error

Channel Gain Error is a deviation from the ideal slope of the transfer function. The Prescaler Gain Error is expressed as the percent difference between the actual and ideal, as shown in EQ 2.

$$\text{Error}_{\text{Gain}} = (1\text{-Gain}) \times 100\%$$

EQ 2

Table 2-52 • Calibrated Analog Channel Accuracy [1,2,3]
Worst-Case Industrial Conditions, T_J = 85°C

		Condition	Total Channel Error (LSB)		
Analog Pad	**Prescaler Range (V)**	**Input Voltage[4] (V)**	**Negative Max.**	**Median**	**Positive Max.**
Positive Range			**ADC in 10-Bit Mode**		
AV, AC	16	0.300 to 12.0	–6	1	6
	8	0.250 to 8.00	–6	0	6
	4	0.200 to 4.00	–7	–1	7
	2	0.150 to 2.00	–7	0	7
	1	0.050 to 1.00	–6	–1	6
AT	16	0.300 to 16.0	–5	0	5
	4	0.100 to 4.00	–7	–1	7
Negative Range			**ADC in 10-Bit Mode**		
AV, AC	16	–0.400 to –10.5	–7	1	9
	8	–0.350 to –8.00	–7	–1	7
	4	–0.300 to –4.00	–7	–2	9
	2	–0.250 to –2.00	–7	–2	7
	1	–0.050 to –1.00	–16	–1	20

Notes:

1. *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Overall accuracy remains the same.*
2. *Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User Guide.
3. *Calibrated with two-point calibration methodology, using 20% and 80% full-scale points.*
4. *The lower limit of the input voltage is determined by the prescaler input offset.*

Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Standard I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Note: Currents are measured at 85°C junction temperature.

Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions
Applicable to All I/O Bank Types

DC I/O Standards	Commercial[1]		Industrial[2]	
	IIL[3]	IIH[4]	IIL[3]	IIH[4]
	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_J < 85°C)*
2. *Industrial range (–40°C < T_J < 100°C)*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

Table 2-96 • I/O Output Buffer Maximum Resistances [1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	17 mA	27	31
SSTL2 (II)	21 mA	13	15
SSTL3 (I)	16 mA	44	69
SSTL3 (II)	24 mA	18	32
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$

Table 2-113 • 2.5 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.51	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.45	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8 mA	Std.	0.60	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.51	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.45	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12 mA	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16 mA	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24 mA	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

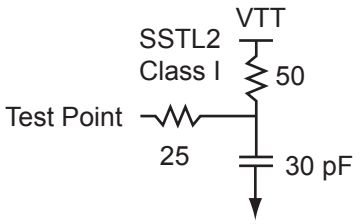


Figure 2-130 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-158 • SSTL 2 Class I
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

VCC Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the Fusion device.

VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. B*x* is the I/O bank number. There are either four (AFS090 and AFS250) or five (AFS600 and AFS1500) I/O banks on the Fusion devices plus a dedicated VJTAG bank.

Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VCCPLA/B PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V, where A and B refer to the PLL. AFS090 and AFS250 each have a single PLL. The AFS600 and AFS1500 devices each have two PLLs. Microsemi recommends tying VCCPLX to VCC and using proper filtering circuits to decouple VCC noise from PLL.

If unused, VCCPLA/B should be tied to GND.

VCOMPLA/B Ground for West and East PLL

VCOMPLA is the ground of the west PLL (CCC location F) and VCOMPLB is the ground of the east PLL (CCC location C).

VJTAG JTAG Supply Voltage

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a Fusion device is in a JTAG chain of interconnected boards and it is desired to power down the board containing the Fusion device, this may be done provided both VJTAG and VCC to the Fusion part remain powered; otherwise, JTAG signals will not be able to transition the Fusion device, even in bypass mode.

VPUMP Programming Supply Voltage

Fusion devices support single-voltage ISP programming of the configuration flash and FlashROM. For programming, VPUMP should be in the 3.3 V +/-5% range. During normal device operation, VPUMP can be left floating or can be tied to any voltage between 0 V and 3.6 V.

When the VPUMP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 19.00°C/W (taken from Table 3-6 on page 3-7).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{19.00°C/W} = 1.3\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 17.00°C/W

θ_{JC} = 8.28°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

PLL/CCC Contribution—P_{PLL}

PLL is not used in this application.

P_{PLL} = 0 W

Nonvolatile Memory—P_{NVM}

Nonvolatile memory is not used in this application.

P_{NVM} = 0 W

Crystal Oscillator—$P_{XTL-OSC}$

The application utilizes standby mode. The crystal oscillator is assumed to be active.

Operating Mode

$P_{XTL-OSC}$ = PAC18

$P_{XTL-OSC}$ = 0.63 mW

Standby Mode

$P_{XTL-OSC}$ = PAC18

$P_{XTL-OSC}$ = 0.63 mW

Sleep Mode

$P_{XTL-OSC}$ = 0 W

RC Oscillator—P_{RC-OSC}

Operating Mode

P_{RC-OSC} = PAC19

P_{RC-OSC} = 3.30 mW

Standby Mode and Sleep Mode

P_{RC-OSC} = 0 W

Analog System—P_{AB}

Number of Quads used: N_{QUADS} = 4

Operating Mode

P_{AB} = PAC20

P_{AB} = 3.00 mW

Standby Mode and Sleep Mode

P_{AB} = 0 W

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL-OSC} + P_{RC-OSC} + P_{AB}$

P_{DYN} = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P_{DYN} = 143.06 mW

Standby Mode

$P_{DYN} = P_{XTL-OSC}$

P_{DYN} = 0.63 mW

Sleep Mode

P_{DYN} = 0 W

FG256				
Pin Number	**AFS090 Function**	**AFS250 Function**	**AFS600 Function**	**AFS1500 Function**
E13	VCCIB1	VCCIB1	VCCIB2	VCCIB2
E14	GCC2/IO33NDB1V0	IO42NDB1V0	IO32NDB2V0	IO46NDB2V0
E15	GCB2/IO33PDB1V0	GBC2/IO42PDB1V0	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0
E16	GND	GND	GND	GND
F1	NC	NC	IO79NDB4V0	IO111NDB4V0
F2	NC	NC	IO79PDB4V0	IO111PDB4V0
F3	GFB1/IO48PPB3V0	IO72NDB3V0	IO76NDB4V0	IO112NDB4V0
F4	GFC0/IO49NDB3V0	IO72PDB3V0	IO76PDB4V0	IO112PDB4V0
F5	NC	NC	IO82PSB4V0	IO120PSB4V0
F6	GFC1/IO49PDB3V0	GAC2/IO74PPB3V0	GAC2/IO83PPB4V0	GAC2/IO123PPB4V0
F7	NC	IO09RSB0V0	IO04PPB0V0	IO05PPB0V1
F8	NC	IO19RSB0V0	IO08NDB0V1	IO11NDB0V1
F9	NC	NC	IO20PDB1V0	IO27PDB1V1
F10	NC	IO29RSB0V0	IO23NDB1V1	IO37NDB1V2
F11	NC	IO43NDB1V0	IO36NDB2V0	IO50NDB2V0
F12	NC	IO43PDB1V0	IO36PDB2V0	IO50PDB2V0
F13	NC	IO44NDB1V0	IO39NDB2V0	IO59NDB2V0
F14	NC	GCA2/IO44PDB1V0	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0
F15	GCC1/IO34PDB1V0	GCB2/IO45PDB1V0	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0
F16	GCC0/IO34NDB1V0	IO45NDB1V0	IO40NDB2V0	IO60NDB2V0
G1	GEC0/IO46NPB3V0	IO70NPB3V0	IO74NPB4V0	IO109NPB4V0
G2	VCCIB3	VCCIB3	VCCIB4	VCCIB4
G3	GEC1/IO46PPB3V0	GFB2/IO70PPB3V0	GFB2/IO74PPB4V0	GFB2/IO109PPB4V0
G4	GFA1/IO47PDB3V0	GFA2/IO71PDB3V0	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0
G5	GND	GND	GND	GND
G6	GFA0/IO47NDB3V0	IO71NDB3V0	IO75NDB4V0	IO110NDB4V0
G7	GND	GND	GND	GND
G8	VCC	VCC	VCC	VCC
G9	GND	GND	GND	GND
G10	VCC	VCC	VCC	VCC
G11	GDA1/IO37NDB1V0	GCC0/IO47NDB1V0	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0
G12	GND	GND	GND	GND
G13	IO37PDB1V0	GCC1/IO47PDB1V0	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0
G14	GCB0/IO35NPB1V0	IO46NPB1V0	IO41NPB2V0	IO61NPB2V0
G15	VCCIB1	VCCIB1	VCCIB2	VCCIB2
G16	GCB1/IO35PPB1V0	GCC2/IO46PPB1V0	GCC2/IO41PPB2V0	GCC2/IO61PPB2V0
H1	GEB1/IO45PDB3V0	GFC2/IO69PDB3V0	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0
H2	GEB0/IO45NDB3V0	IO69NDB3V0	IO73NDB4V0	IO108NDB4V0

FG256				
Pin Number	**AFS090 Function**	**AFS250 Function**	**AFS600 Function**	**AFS1500 Function**
H3	XTAL2	XTAL2	XTAL2	XTAL2
H4	XTAL1	XTAL1	XTAL1	XTAL1
H5	GNDOSC	GNDOSC	GNDOSC	GNDOSC
H6	VCCOSC	VCCOSC	VCCOSC	VCCOSC
H7	VCC	VCC	VCC	VCC
H8	GND	GND	GND	GND
H9	VCC	VCC	VCC	VCC
H10	GND	GND	GND	GND
H11	GDC0/IO38NDB1V0	IO51NDB1V0	IO47NDB2V0	IO69NDB2V0
H12	GDC1/IO38PDB1V0	IO51PDB1V0	IO47PDB2V0	IO69PDB2V0
H13	GDB1/IO39PDB1V0	GCA1/IO49PDB1V0	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
H14	GDB0/IO39NDB1V0	GCA0/IO49NDB1V0	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
H15	GCA0/IO36NDB1V0	GCB0/IO48NDB1V0	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
H16	GCA1/IO36PDB1V0	GCB1/IO48PDB1V0	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
J1	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
J2	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
J3	IO43NDB3V0	GFB0/IO67NDB3V0	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
J4	GEC2/IO43PDB3V0	GFB1/IO67PDB3V0	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0
J5	NC	GFC0/IO68NDB3V0	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
J6	NC	GFC1/IO68PDB3V0	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0
J7	GND	GND	GND	GND
J8	VCC	VCC	VCC	VCC
J9	GND	GND	GND	GND
J10	VCC	VCC	VCC	VCC
J11	GDC2/IO41NPB1V0	IO56NPB1V0	IO56NPB2V0	IO83NPB2V0
J12	NC	GDB0/IO53NPB1V0	GDB0/IO53NPB2V0	GDB0/IO80NPB2V0
J13	NC	GDA1/IO54PDB1V0	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
J14	GDA0/IO40PDB1V0	GDC1/IO52PPB1V0	GDC1/IO52PPB2V0	GDC1/IO79PPB2V0
J15	NC	IO50NPB1V0	IO51NSB2V0	IO77NSB2V0
J16	GDA2/IO40NDB1V0	GDC0/IO52NPB1V0	GDC0/IO52NPB2V0	GDC0/IO79NPB2V0
K1	NC	IO65NPB3V0	IO67NPB4V0	IO92NPB4V0
K2	VCCIB3	VCCIB3	VCCIB4	VCCIB4
K3	NC	IO65PPB3V0	IO67PPB4V0	IO92PPB4V0
K4	NC	IO64PDB3V0	IO65PDB4V0	IO96PDB4V0
K5	GND	GND	GND	GND
K6	NC	IO64NDB3V0	IO65NDB4V0	IO96NDB4V0
K7	VCC	VCC	VCC	VCC
K8	GND	GND	GND	GND