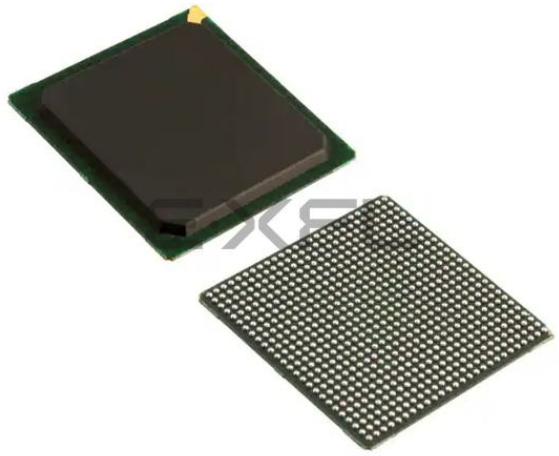

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 252 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-fgg676 |

### Timing Characteristics

**Table 2-1 • Combinatorial Cell Propagation Delays**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Combinatorial Cell | Equation | Parameter | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.40 | 0.46 | 0.54 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.47 | 0.54 | 0.63 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 0.47 | 0.54 | 0.63 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 0.49 | 0.55 | 0.65 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.49 | 0.55 | 0.65 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 0.74 | 0.84 | 0.99 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 0.70 | 0.79 | 0.93 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 0.87 | 1.00 | 1.17 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 0.51 | 0.58 | 0.68 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 0.56 | 0.64 | 0.75 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library (Figure 2-5). For more details, refer to the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide*.

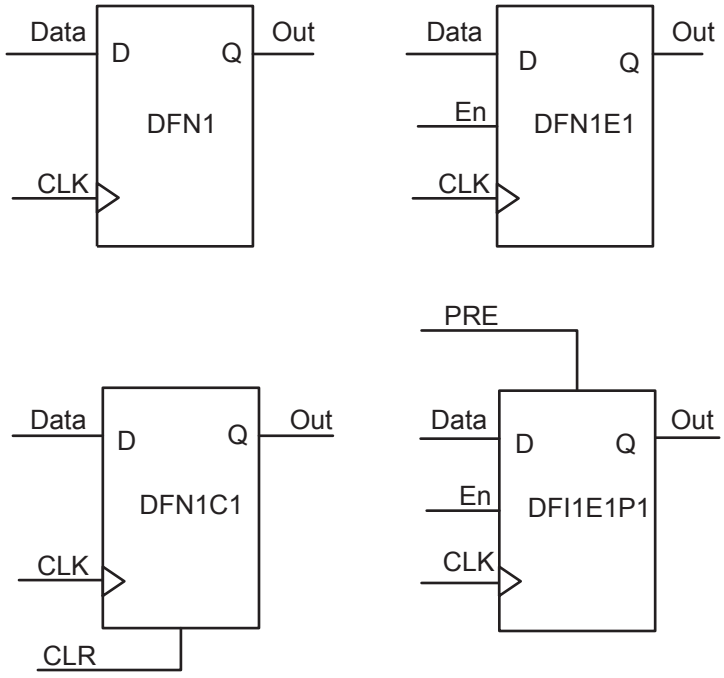



**Figure 2-5 • Sample of Sequential Cells**

## RC Oscillator

The RC oscillator is an on-chip free-running clock source generating a 100 MHz clock. It can be used as a source clock for both on-chip and off-chip resources. When used in conjunction with the Fusion PLL and CCC circuits, the RC oscillator clock source can be used to generate clocks of varying frequency and phase.

The Fusion RC oscillator is very accurate at ±1% over commercial temperature ranges and and ±3% over industrial temperature ranges. It is an automated clock, requiring no setup or configuration by the user. It requires only that the power and GNDOSC pins be connected; no external components are required. The RC oscillator can be used to drive either a PLL or another internal signal.

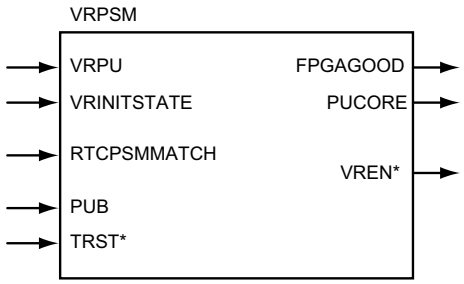
### RC Oscillator Characteristics

***Table 2-9 •*** **Electrical Characteristics of RC Oscillator**

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{RC}$ | Operating Frequency | | | 100 | | MHz |
| | Accuracy | Temperature: 0°C to 85°C<br>Voltage: 3.3 V ± 5% | | 1 | | % |
| | | Temperature: –40°C to 125°C<br>Voltage: 3.3 V ± 5% | | 3 | | % |
| | Output Jitter | Period Jitter (at 5 k cycles) | | 100 | | ps |
| | | Cycle–Cycle Jitter (at 5 k cycles) | | 100 | | ps |
| | | Period Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply | | 150 | | ps |
| | | Cycle–Cycle Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply | | 150 | | ps |
| | Output Duty Cycle | | | 50 | | % |
| $I_{DYNRC}$ | Operating Current | | | 1 | | mA |

## Voltage Regulator and Power System Monitor (VRPSM)

The VRPSM macro controls the power-up state of the FPGA. The power-up bar (PUB) pin can turn on the voltage regulator when set to 0. TRST can enable the voltage regulator when deasserted, allowing the FPGA to power-up when user want access to JTAG ports. The inputs VRINITSTATE and RTCPSMMATCH come from the flash bits and RTC, and can also power up the FPGA.




*Note: *Signals are hardwired internally and do not exist in the macro core.*

***Figure 2-30 •*** **VRPSM Macro**

***Table 2-17 •*** **VRPSM Signal Descriptions**

| Signal Name | Width | Direction | Function |
|---|---|---|---|
| VRPU | 1 | In | Voltage Regulator Power-Up<br>0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator.<br>1 – Voltage regulator enabled |
| VRINITSTATE | 1 | In | Voltage Regulator Initial State<br>Defines the voltage Regulator status upon power-up of the 3.3 V. The signal is configured by Libero SoC when the VRPSM macro is generated.<br>Tie off to 1 – Voltage regulator enables when 3.3 V is powered.<br>Tie off to 0 – Voltage regulator disables when 3.3 V is powered. |
| RTCPSMMATCH | 1 | In | RTC Power System Management Match<br>Connect from RTCPSMATCH signal from RTC in AB<br>0 transition to 1 turns on the voltage regulator |
| PUB | 1 | In | External pin, built-in weak pull-up<br>Power-Up Bar<br>0 – Enables voltage regulator at all times |
| TRST* | 1 | In | External pin, JTAG Test Reset<br>1 – Enables voltage regulator at all times |
| FPGAGOOD | 1 | Out | Indicator that the FPGA is powered and functional<br>No need to connect if it is not used.<br>1 – Indicates that the FPGA is powered up and functional.<br>0 – Not possible to read by FPGA since it has already powered off. |
| PUCORE | 1 | Out | Power-Up Core<br>Inverted signal of PUB. No need to connect if it is not used. |
| VREN* | 1 | Out | Voltage Regulator Enable<br>Connected to 1.5 V voltage regulator in Fusion device internally.<br>0 – Voltage regulator disables<br>1 – Voltage regulator enables |
| *Note: *Signals are hardwired internally and do not exist in the macro core.* | | | |

### Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is High. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "SRAM Characteristics" section on page 2-63 and the "FIFO Characteristics" section on page 2-72.

### RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG IEEE 1532" section on page 2-229 and the *Fusion SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

## Temperature Monitor

The final pin in the Analog Quad is the Analog Temperature (AT) pin. The AT pin is used to implement an accurate temperature monitor in conjunction with an external diode-connected bipolar transistor (Figure 2-76). For improved temperature measurement accuracy, it is important to use the ATRTN pin for the return path of the current sourced by the AT pin. Each ATRTN pin is shared between two adjacent Analog Quads. Additionally, if not used for temperature monitoring, the AT pin can provide functionality similar to that of the AV pad. However, in this mode only positive voltages can be applied to the AT pin, and only two prescaler factors are available (16 V and 4 V ranges—refer to Table 2-57 on page 2-130).

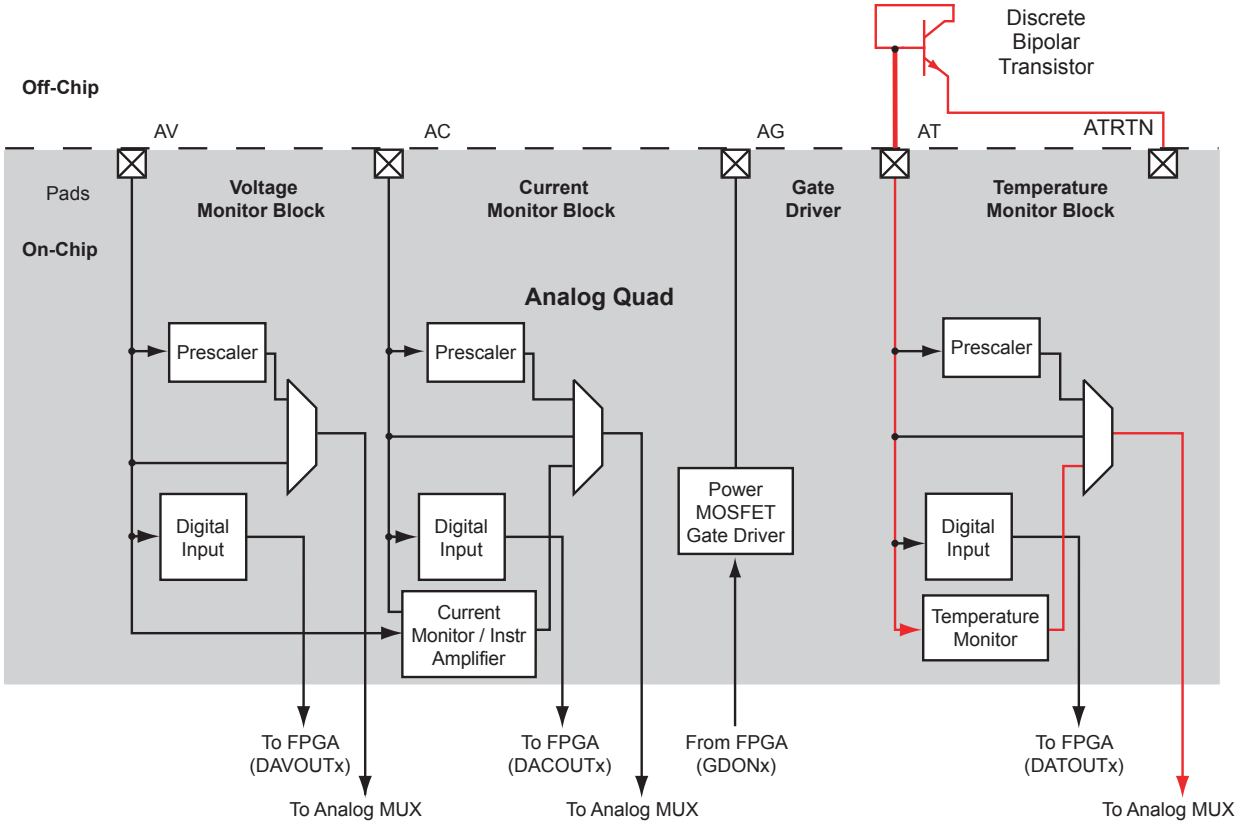



***Figure 2-76 •*** **Temperature Monitor Quad**

Fusion uses a remote diode as a temperature sensor. The Fusion Temperature Monitor uses a differential input; the AT pin and ATRTN (AT Return) pin are the differential inputs to the Temperature Monitor. There is one Temperature Monitor in each Quad. A simplified block diagram is shown in Figure 2-77.

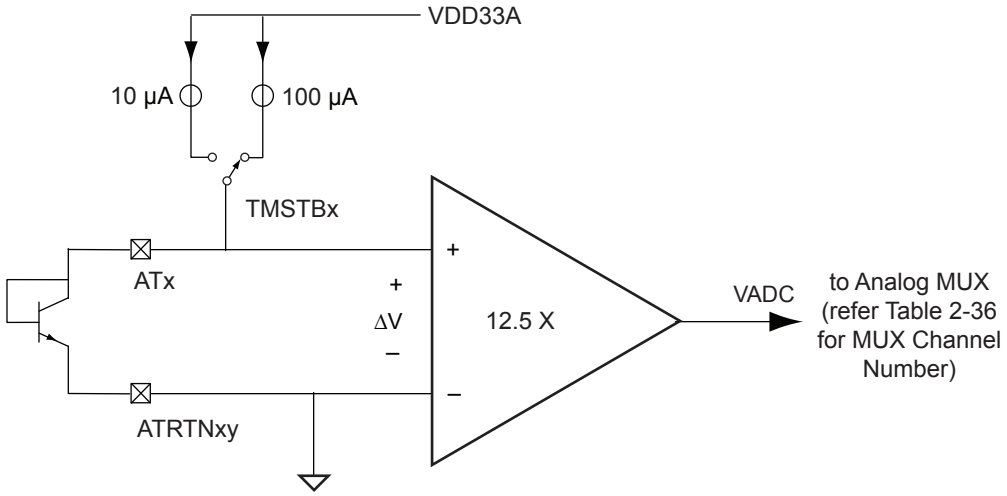



***Figure 2-77 •*** **Block Diagram for Temperature Monitor Circuit**

The Fusion approach to measuring temperature is forcing two different currents through the diode with a ratio of 10:1. The switch that controls the different currents is controlled by the Temperature Monitor Strobe signal, TMSTB. Setting TMSTB to '1' will initiate a Temperature reading. The TMSTB should remain '1' until the ADC finishes sampling the voltage from the Temperature Monitor. The minimum sample time for the Temperature Monitor cannot be less than the minimum strobe high time minus the setup time. Figure 2-78 shows the timing diagram.

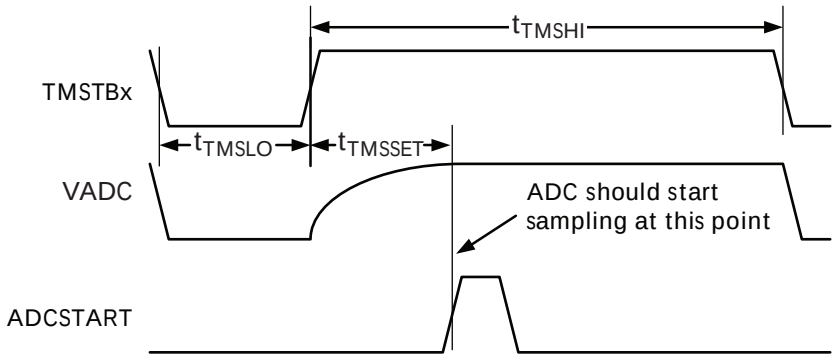



***Figure 2-78 •*** **Timing Diagram for the Temperature Monitor Strobe Signal**

Note: When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device.

Refer to Table 2-46 on page 2-109 and the "Acquisition Time or Sample Time Control" section on page 2-107

$$t_{sample} = (2 + STC) \times t_{ADCCLK}$$

*EQ 20*

STC: Sample Time Control value (0–255)

$t_{SAMPLE}$ is the sample time

***Table 2-46 •*** **STC Bits Function**

| Name | Bits | Function |
|---|---|---|
| STC | [7:0] | Sample time control |

Sample time is computed based on the period of ADCCLK.

### Distribution Phase

The second phase is called the distribution phase. During distribution phase, the ADC computes the equivalent digital value from the value stored in the input capacitor. In this phase, the output signal SAMPLE goes back to '0', indicating the sample is completed; but the BUSY signal remains '1', indicating the ADC is still busy for distribution. The distribution time depends strictly on the number of bits. If the ADC is configured as a 10-bit ADC, then 10 ADCCLK cycles are needed. EQ 8 describes the distribution time.

$$t_{distrib} = N \times t_{ADCCLK}$$

*EQ 21*

N: Number of bits

### Post-Calibration Phase

The last phase is the post-calibration phase. This is an optional phase. The post-calibration phase takes two ADCCLK cycles. The output BUSY signal will remain '1' until the post-calibration phase is completed. If the post-calibration phase is skipped, then the BUSY signal goes to '0' after distribution phase. As soon as BUSY signal goes to '0', the DATAVALID signal goes to '1', indicating the digital result is available on the RESULT output signals. DATAVAILD will remain '1' until the next ADCSTART is asserted. Microsemi recommends enabling post-calibration to compensate for drift and temperature-dependent effects. This ensures that the ADC remains consistent over time and with temperature. The post-calibration phase is enabled by bit 3 of the Mode register. EQ 9 describes the post-calibration time.

$$t_{post\text{-}cal} = MODE[3] \times (2 \times t_{ADCCLK})$$

*EQ 22*

MODE[3]: Bit 3 of the Mode register, described in Table 2-41 on page 2-106.

The calculation for the conversion time for the ADC is summarized in EQ 23.

$$t_{conv} = t_{sync\_read} + t_{sample} + t_{distrib} + t_{post\text{-}cal} + t_{sync\_write}$$

*EQ 23*

$t_{conv}$: conversion time

$t_{sync\_read}$: maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, $t_{SYSCLK}$.

$t_{sample}$: Sample time

$t_{distrib}$: Distribution time

$t_{post\text{-}cal}$: Post-calibration time

$t_{sync\_write}$: Maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, $t_{SYSCLK}$.

**Table 2-50 • ADC Characteristics in Direct Input Mode**
**Commercial Temperature Range Conditions, $T_J$ = 85°C (unless noted otherwise),**
**Typical: VCC33A = 3.3 V, VCC = 1.5 V**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Direct Input using Analog Pad AV, AC, AT** | | | | | | |
| VINADC | Input Voltage (Direct Input) | Refer to Table 3-2 on page 3-3 | | | | |
| CINADC | Input Capacitance | Channel not selected | | 7 | | pF |
| | | Channel selected but not sampling | | 8 | | pF |
| | | Channel selected and sampling | | 18 | | pF |
| ZINADC | Input Impedance | 8-bit mode | | 2 | | kΩ |
| | | 10-bit mode | | 2 | | kΩ |
| | | 12-bit mode | | 2 | | kΩ |
| **Analog Reference Voltage VAREF** | | | | | | |
| VAREF | Accuracy | $T_J$ = 25°C | 2.537 | 2.56 | 2.583 | V |
| | Temperature Drift of Internal Reference | | | 65 | | ppm / °C |
| | External Reference | | 2.527 | | VCC33A + 0.05 | V |
| **ADC Accuracy (using external reference)** [1,2] | | | | | | |
| **DC Accuracy** | | | | | | |
| TUE | Total Unadjusted Error | 8-bit mode | | 0.29 | | LSB |
| | | 10-bit mode | | 0.72 | | LSB |
| | | 12-bit mode | | 1.8 | | LSB |
| INL | Integral Non-Linearity | 8-bit mode | | 0.20 | 0.25 | LSB |
| | | 10-bit mode | | 0.32 | 0.43 | LSB |
| | | 12-bit mode | | 1.71 | 1.80 | LSB |
| DNL | Differential Non-Linearity (no missing code) | 8-bit mode | | 0.20 | 0.24 | LSB |
| | | 10-bit mode | | 0.60 | 0.65 | LSB |
| | | 12-bit mode | | 2.40 | 2.48 | LSB |
| | Offset Error | 8-bit mode | | 0.01 | 0.17 | LSB |
| | | 10-bit mode | | 0.05 | 0.20 | LSB |
| | | 12-bit mode | | 0.20 | 0.40 | LSB |
| | Gain Error | 8-bit mode | | 0.0004 | 0.003 | LSB |
| | | 10-bit mode | | 0.002 | 0.011 | LSB |
| | | 12-bit mode | | 0.007 | 0.044 | LSB |
| | Gain Error (with internal reference) | All modes | | 2 | | % FSR |

*Notes:*

1. *Accuracy of the external reference is 2.56 V ± 4.6 mV.*
2. *Data is based on characterization.*
3. *The sample rate is time-shared among active analog inputs.*

# Analog Configuration MUX

The ACM is the interface between the FPGA, the Analog Block configurations, and the real-time counter. Microsemi Libero SoC will generate IP that will load and configure the Analog Block via the ACM. However, users are not limited to using the Libero SoC IP. This section provides a detailed description of the ACM's register map, truth tables for proper configuration of the Analog Block and RTC, as well as timing waveforms so users can access and control the ACM directly from their designs.

The Analog Block contains four 8-bit latches per Analog Quad that are initialized through the ACM. These latches act as configuration bits for Analog Quads. The ACM block runs from the core voltage supply (1.5 V).

Access to the ACM is achieved via 8-bit address and data busses with enables. The pin list is provided in Table 2-36 on page 2-78. The ACM clock speed is limited to a maximum of 10 MHz, more than sufficient to handle the low-bandwidth requirements of configuring the Analog Block and the RTC (sub-block of the Analog Block).

Table 2-54 decodes the ACM address space and maps it to the corresponding Analog Quad and configuration byte for that quad.

***Table 2-54 •*** **ACM Address Decode Table for Analog Quad**

| ACMADDR [7:0] in Decimal | Name | Description | Associated Peripheral |
|---|---|---|---|
| 0 | – | – | Analog Quad |
| 1 | AQ0 | Byte 0 | Analog Quad |
| 2 | AQ0 | Byte 1 | Analog Quad |
| 3 | AQ0 | Byte 2 | Analog Quad |
| 4 | AQ0 | Byte 3 | Analog Quad |
| 5 | AQ1 | Byte 0 | Analog Quad |
| .<br>.<br>. | .<br>.<br>. | .<br>.<br>. | Analog Quad |
| 36 | AQ8 | Byte 3 | Analog Quad |
| 37 | AQ9 | Byte 0 | Analog Quad |
| 38 | AQ9 | Byte 1 | Analog Quad |
| 39 | AQ9 | Byte 2 | Analog Quad |
| 40 | AQ9 | Byte 3 | Analog Quad |
| 41 | | Undefined | Analog Quad |
| .<br>.<br>. | .<br>.<br>. | Undefined | Analog Quad |
| 63 | | Undefined | RTC |
| 64 | COUNTER0 | Counter bits 7:0 | RTC |
| 65 | COUNTER1 | Counter bits 15:8 | RTC |
| 66 | COUNTER2 | Counter bits 23:16 | RTC |
| 67 | COUNTER3 | Counter bits 31:24 | RTC |
| 68 | COUNTER4 | Counter bits 39:32 | RTC |
| 72 | MATCHREG0 | Match register bits 7:0 | RTC |

## Detailed I/O DC Characteristics

**Table 2-95 • Input Capacitance**

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | VIN = 0, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | VIN = 0, f = 1.0 MHz | | 8 | pF |

**Table 2-96 • I/O Output Buffer Maximum Resistances [1]**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (ohms) [2] | $R_{PULL\text{-}UP}$ (ohms) [3] |
|---|---|---|---|
| **Applicable to Pro I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 4 mA | 100 | 300 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 2.5 V LVCMOS | 4 mA | 100 | 200 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |
| 3.3 V GTL | 20 mA | 11 | – |
| 2.5 V GTL | 20 mA | 14 | – |
| 3.3 V GTL+ | 35 mA | 12 | – |
| 2.5 V GTL+ | 33 mA | 15 | – |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$

***Table 2-98* • I/O Short Currents IOSH/IOSL (continued)**

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|---|---|---|---|
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 103 | 109 |
| **Applicable to Standard I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |

*Note: *$T_J$ = 100°C*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

### HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-150 • Minimum and Maximum DC Input and Output Levels**

| HSTL Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 8 mA | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 8 | 8 | 39 | 32 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

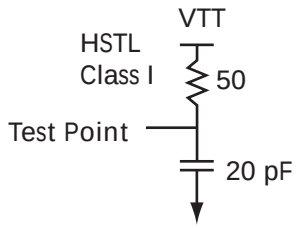



**Figure 2-128 • AC Loading**

**Table 2-151 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-152 • HSTL Class I**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 3.18 | 0.04 | 2.12 | 0.43 | 3.24 | 3.14 | | | 5.47 | 5.38 | ns |
| –1 | 0.56 | 2.70 | 0.04 | 1.81 | 0.36 | 2.75 | 2.67 | | | 4.66 | 4.58 | ns |
| –2 | 0.49 | 2.37 | 0.03 | 1.59 | 0.32 | 2.42 | 2.35 | | | 4.09 | 4.02 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-153 • Minimum and Maximum DC Input and Output Levels**

| HSTL Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 15 mA[3] | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 15 | 15 | 55 | 66 | 10 | 10 |

*Note:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

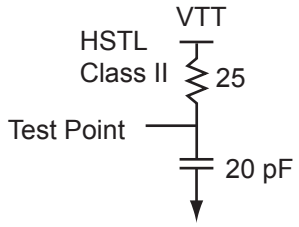



**Figure 2-129 • AC Loading**

**Table 2-154 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-155 • HSTL Class II**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 3.02 | 0.04 | 2.12 | 0.43 | 3.08 | 2.71 | | | 5.32 | 4.95 | ns |
| –1 | 0.56 | 2.57 | 0.04 | 1.81 | 0.36 | 2.62 | 2.31 | | | 4.52 | 4.21 | ns |
| –2 | 0.49 | 2.26 | 0.03 | 1.59 | 0.32 | 2.30 | 2.03 | | | 3.97 | 3.70 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-165 • Minimum and Maximum DC Input and Output Levels**

| SSTL3 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 21 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI – 0.9 | 21 | 21 | 109 | 103 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

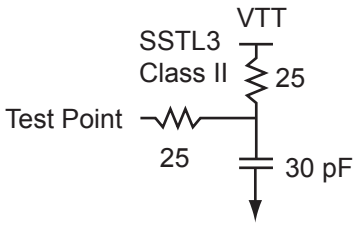



**Figure 2-133 • AC Loading**

**Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-167 • SSTL3- Class II**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.07 | 0.04 | 1.25 | 0.43 | 2.10 | 1.67 | | | 4.34 | 3.91 | ns |
| –1 | 0.56 | 1.76 | 0.04 | 1.06 | 0.36 | 1.79 | 1.42 | | | 3.69 | 3.32 | ns |
| –2 | 0.49 | 1.54 | 0.03 | 0.93 | 0.32 | 1.57 | 1.25 | | | 3.24 | 2.92 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-136. The building blocks of the LVPECL transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

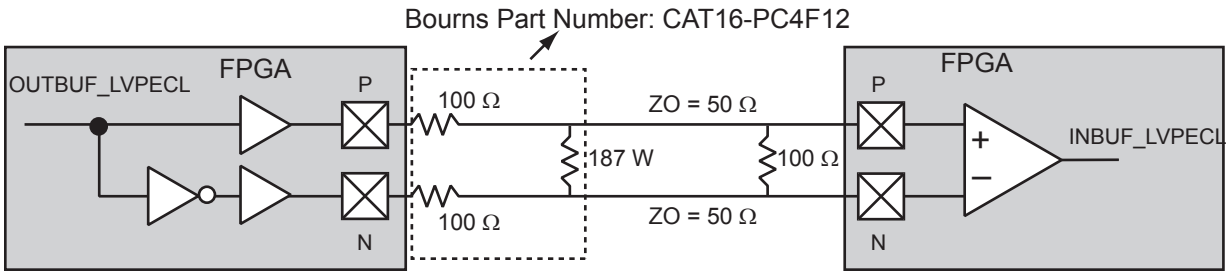



***Figure 2-136* • LVPECL Circuit Diagram and Board-Level Implementation**

***Table 2-171* • Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| VCCI | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | | 300 | | 300 | | mV |

***Table 2-172* • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---|---|---|---|
| 1.64 | 1.94 | Cross point | – |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### Timing Characteristics

***Table 2-173* • LVPECL**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 3.0 V**
**Applicable to Pro I/Os**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.66 | 2.14 | 0.04 | 1.63 | ns |
| –1 | 0.56 | 1.82 | 0.04 | 1.39 | ns |
| –2 | 0.49 | 1.60 | 0.03 | 1.22 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

## DDR Module Specifications

### Input DDR Module

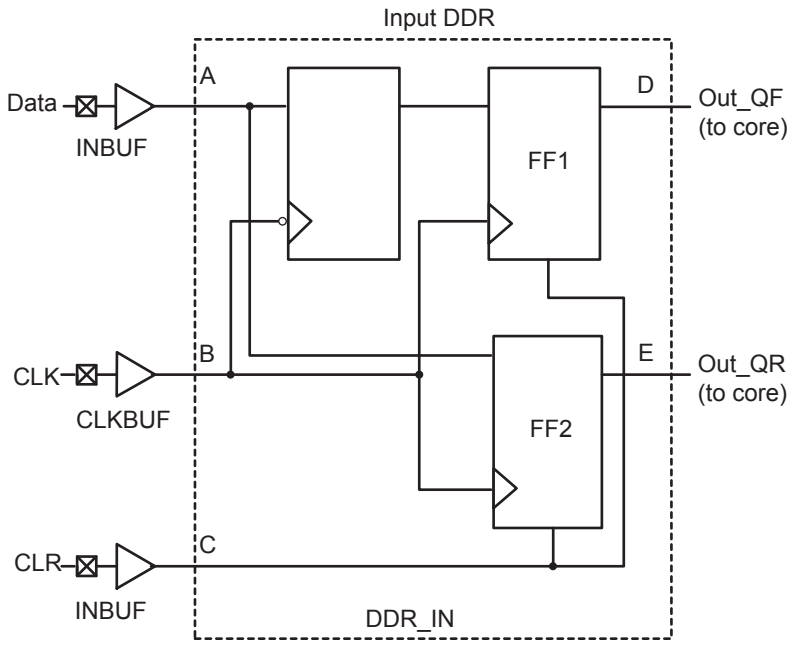



***Figure 2-142 •*** **Input DDR Timing Model**

***Table 2-179 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR Input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR Input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

# Power Consumption

***Table 3-18* • Power Consumption**

| Parameter | Description | Condition | Min. | Typical | Max. | Units |
|---|---|---|---|---|---|---|
| **Crystal Oscillator** | | | | | | |
| ISTBXTAL | Standby Current of Crystal Oscillator | | | 10 | | µA |
| IDYNXTAL | Operating Current | RC | | 0.6 | | mA |
| | | 0.032–0.2 | | 0.19 | | mA |
| | | 0.2–2.0 | | 0.6 | | mA |
| | | 2.0–20.0 | | 0.6 | | mA |
| **RC Oscillator** | | | | | | |
| IDYNRC | Operating Current | | | 1 | | mA |
| **ACM** | | | | | | |
| | Operating Current (fixed clock) | | | 200 | | µA/MHz |
| | Operating Current (user clock) | | | 30 | | µA |
| **NVM System** | | | | | | |
| | NVM Array Operating Power | Idle | | 795 | | µA |
| | | Read operation | | See Table 3-15 on page 3-23. | | See Table 3-15 on page 3-23. |
| | | Erase | | 900 | | µA |
| | | Write | | 900 | | µA |
| PNVMCTRL | NVM Controller Operating Power | | | 20 | | µW/MHz |

| QN180 | | |
|---|---|---|
| Pin Number | AFS090 Function | AFS250 Function |
| A1 | GNDQ | GNDQ |
| A2 | VCCIB3 | VCCIB3 |
| A3 | GAB2/IO52NDB3V0 | IO74NDB3V0 |
| A4 | GFA2/IO51NDB3V0 | IO71NDB3V0 |
| A5 | GFC2/IO50NDB3V0 | IO69NPB3V0 |
| A6 | VCCIB3 | VCCIB3 |
| A7 | GFA1/IO47PPB3V0 | GFB1/IO67PPB3V0 |
| A8 | GEB0/IO45NDB3V0 | NC |
| A9 | XTAL1 | XTAL1 |
| A10 | GNDOSC | GNDOSC |
| A11 | GEC2/IO43PPB3V0 | GEA1/IO61PPB3V0 |
| A12 | IO43NPB3V0 | GEA0/IO61NPB3V0 |
| A13 | NC | VCCIB3 |
| A14 | GNDNVM | GNDNVM |
| A15 | PCAP | PCAP |
| A16 | VCC33PMP | VCC33PMP |
| A17 | NC | NC |
| A18 | AV0 | AV0 |
| A19 | AG0 | AG0 |
| A20 | ATRTN0 | ATRTN0 |
| A21 | AG1 | AG1 |
| A22 | AC1 | AC1 |
| A23 | AV2 | AV2 |
| A24 | AT2 | AT2 |
| A25 | AT3 | AT3 |
| A26 | AC3 | AC3 |
| A27 | AV4 | AV4 |
| A28 | AC4 | AC4 |
| A29 | AT4 | AT4 |
| A30 | NC | AG5 |
| A31 | NC | AV5 |
| A32 | ADCGNDREF | ADCGNDREF |
| A33 | VCC33A | VCC33A |
| A34 | GNDA | GNDA |
| A35 | PTBASE | PTBASE |
| A36 | VCCNVM | VCCNVM |

| QN180 | | |
|---|---|---|
| Pin Number | AFS090 Function | AFS250 Function |
| A37 | VPUMP | VPUMP |
| A38 | TDI | TDI |
| A39 | TDO | TDO |
| A40 | VJTAG | VJTAG |
| A41 | GDB1/IO39PPB1V0 | GDA1/IO54PPB1V0 |
| A42 | GDC1/IO38PDB1V0 | GDB1/IO53PDB1V0 |
| A43 | VCC | VCC |
| A44 | GCB0/IO35NPB1V0 | GCB0/IO48NPB1V0 |
| A45 | GCC1/IO34PDB1V0 | GCC1/IO47PDB1V0 |
| A46 | VCCIB1 | VCCIB1 |
| A47 | GBC2/IO32PPB1V0 | GBB2/IO41PPB1V0 |
| A48 | VCCIB1 | VCCIB1 |
| A49 | NC | NC |
| A50 | GBA0/IO29RSB0V0 | GBB1/IO37RSB0V0 |
| A51 | VCCIB0 | VCCIB0 |
| A52 | GBB0/IO27RSB0V0 | GBC0/IO34RSB0V0 |
| A53 | GBC1/IO26RSB0V0 | IO33RSB0V0 |
| A54 | IO24RSB0V0 | IO29RSB0V0 |
| A55 | IO21RSB0V0 | IO26RSB0V0 |
| A56 | VCCIB0 | VCCIB0 |
| A57 | IO15RSB0V0 | IO21RSB0V0 |
| A58 | IO10RSB0V0 | IO13RSB0V0 |
| A59 | IO07RSB0V0 | IO10RSB0V0 |
| A60 | GAC0/IO04RSB0V0 | IO06RSB0V0 |
| A61 | GAB1/IO03RSB0V0 | GAC1/IO05RSB0V0 |
| A62 | VCC | VCC |
| A63 | GAA1/IO01RSB0V0 | GAB0/IO02RSB0V0 |
| A64 | NC | NC |
| B1 | VCOMPLA | VCOMPLA |
| B2 | GAA2/IO52PDB3V0 | GAC2/IO74PDB3V0 |
| B3 | GAC2/IO51PDB3V0 | GFA2/IO71PDB3V0 |
| B4 | GFB2/IO50PDB3V0 | GFB2/IO70PSB3V0 |
| B5 | VCC | VCC |
| B6 | GFC0/IO49NDB3V0 | GFC0/IO68NDB3V0 |
| B7 | GEB1/IO45PDB3V0 | NC |
| B8 | VCCOSC | VCCOSC |

| Revision | Changes | Page |
|---|---|---|
| Advance v1.0 (January 2008) | All Timing Characteristics tables were updated. For the Differential I/O Standards, the Standard I/O support tables are new. | N/A |
| | Table 2-3 • Array Coordinates was updated to change the max x and y values | 2-9 |
| | Table 2-12 • Fusion CCC/PLL Specification was updated. | 2-31 |
| | A note was added to Table 2-16 · RTC ACM Memory Map. | 2-37 |
| | A reference to the Peripheral's User's Guide was added to the "Voltage Regulator Power Supply Monitor (VRPSM)" section. | 2-42 |
| | In Table 2-25 • Flash Memory Block Timing, the commercial conditions were updated. | 2-55 |
| | In Table 2-26 • FlashROM Access Time, the commercial conditions were missing and have been added below the title of the table. | 2-58 |
| | In Table 2-36 • Analog Block Pin Description, the function description was updated for the ADCRESET. | 2-82 |
| | In the "Voltage Monitor" section, the following sentence originally had ± 10% and it was changed to +10%.<br>The Analog Quad inputs are tolerant up to 12 V + 10%.<br>In addition, this statement was deleted from the datasheet:<br>Each I/O will draw power when connected to power (3 mA at 3 V). | 2-86 |
| | The "Terminology" section is new. | 2-88 |
| | The "Current Monitor" section was significantly updated. Figure 2-72 • Timing Diagram for Current Monitor Strobe to Figure 2-74 • Negative Current Monitor and Table 2-37 • Recommended Resistor for Different Current Range Measurement are new. | 2-90 |
| | The "ADC Description" section was updated to add the "Terminology" section. | 2-93 |
| | In the "Gate Driver" section, 25 mA was changed to 20 mA and 1.5 MHz was changed to 1.3 MHz. In addition, the following sentence was deleted:<br>The maximum AG pad switching frequency is 1.25 MHz. | 2-94 |
| | The "Temperature Monitor" section was updated to rewrite most of the text and add Figure 2-78, Figure 2-79, and Table 2-38 • Temperature Data Format. | 2-96 |
| | In Table 2-38 • Temperature Data Format, the temperature K column was changed for 85°C from 538 to 358. | 2-98 |
| | In Table 2-45 • ADC Interface Timing, "Typical-Case" was changed to "Worst-Case." | 2-110 |
| | The "ADC Interface Timing" section is new. | 2-110 |
| | Table 2-46 • Analog Channel Specifications was updated. | 2-118 |
| | The "$V_{CC15A}$ Analog Power Supply (1.5 V)" section was updated. | 2-224 |
| | The "$V_{CCPLA/B}$ PLL Supply Voltage" section is new. | 2-225 |
| | In "$V_{CCNVM}$ Flash Memory Block Power Supply (1.5 V)" section, supply was changed to supply input. | 2-224 |
| | The "$V_{CCPLA/B}$ PLL Supply Voltage" pin description was updated to include the following statement:<br>Actel recommends tying VCCPLX to VCC and using proper filtering circuits to decouple $V_{CC}$ noise from PLL. | 2-225 |
| | The "$V_{COMPLA/B}$ Ground for West and East PLL" section was updated. | 2-225 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.5 (June 2006) | The low power modes of operation were updated and clarified. | N/A |
| | The AFS1500 digital I/O count was updated in Table 1 • Fusion Family. | i |
| | The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double-Ended (Analog)" table. | ii |
| | The "Voltage Regulator Power Supply Monitor (VRPSM)" was updated. | 2-36 |
| | Figure 2-45 • FlashROM Timing Diagram was updated. | 2-53 |
| | The "256-Pin FBGA" table for the AFS1500 is new. | 3-12 |
| Advance v0.4 (April 2006) | The G was moved in the "Product Ordering Codes" section. | III |
| Advance v0.3 (April 2006) | The "Features and Benefits" section was updated. | I |
| | The "Fusion Family" table was updated. | I |
| | The "Package I/Os: Single-/Double-Ended (Analog)" table was updated. | II |
| | The "Product Ordering Codes" table was updated. | III |
| | The "Temperature Grade Offerings" table was updated. | IV |
| | The "General Description" section was updated to include ARM information. | 1-1 |
| | Figure 2-46 • FlashROM Timing Diagram was updated. | 2-58 |
| | The "FlashROM" section was updated. | 2-57 |
| | The "RESET" section was updated. | 2-61 |
| | The "RESET" section was updated. | 2-64 |
| | Figure 2-27 · Real-Time Counter System was updated. | 2-35 |
| | Table 2-19 • Flash Memory Block Pin Names was updated. | 2-43 |
| | Figure 2-33 • Flash Memory Block Diagram was updated to include AUX block information. | 2-45 |
| | Figure 2-34 • Flash Memory Block Organization was updated to include AUX block information. | 2-46 |
| | The note in the "Program Operation" section was updated. | 2-48 |
| | Figure 2-76 • Gate Driver Example was updated. | 2-95 |
| | The "Analog Quad ACM Description" section was updated. | 2-130 |
| | Information about the maximum pad input frequency was added to the "Gate Driver" section. | 2-94 |
| | Figure 2-65 • Analog Block Macro was updated. | 2-81 |
| | Figure 2-65 • Analog Block Macro was updated. | 2-81 |
| | The "Analog Quad" section was updated. | 2-84 |
| | The "Voltage Monitor" section was updated. | 2-86 |
| | The "Direct Digital Input" section was updated. | 2-89 |
| | The "Current Monitor" section was updated. | 2-90 |
| | Information about the maximum pad input frequency was added to the "Gate Driver" section. | 2-94 |