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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

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Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs250-1fg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a highly secure, low power, single-chip solution that is Instant On. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

## Flash Advantages

## Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flashbased Fusion devices are Instant On and do not need to be loaded from an external boot PROM.

On-board security mechanisms prevent access to the programming information and enable remote updates of the FPGA logic that are protected with high level security. Designers can perform remote insystem reprogramming to support future design iterations and field upgrades, with confidence that valuable IP is highly unlikely to be compromised or copied. ISP can be performed using the

industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

## Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a

built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with

AES-based security provide a high level of protection for remote field updates over public networks, such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with

industry-standard security, making remote ISP possible. A Fusion device provides the best available security for programmable logic designs.

## Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

## CCC and PLL Characteristics

#### **Timing Characteristics**

#### Table 2-12 • Fusion CCC/PLL Specification

Parameter	Min.	Тур.	Max.	Unit
Clock Conditioning Circuitry Input Frequency fIN_CCC	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f <sub>OUT_CCC</sub>	0.75		350	MHz
Delay Increments in Programmable Delay Blocks <sup>1, 2</sup>		160 <sup>3</sup>		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F <sub>CCC_OUT</sub>	Max Pea	k-to-Peak Po	eriod Jitter	
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	1.00%		1.00%	
24 MHz to 100 MHz	1.50%		1.50%	
100 MHz to 250 MHz	2.25%		2.25%	
250 MHz to 350 MHz	3.50%		3.50%	
Acquisition Time LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter <sup>4</sup> LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 <sup>1,2</sup>	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 <sup>1, 2</sup>	0.025		5.56	ns
Delay Range in Block: Fixed Delay <sup>1, 2</sup>		2.2		ns

Notes:

1. This delay is a function of voltage and temperature. See Table 3-7 on page 3-9 for deratings.

2.  $T_J = 25^{\circ}C$ , VCC = 1.5 V

3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

4. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.



Device Architecture

#### Table 2-19 • Flash Memory Block Pin Names (continued)

Interface Name	Width	Direction	Description
STATUS[1:0]	2	Out	Status of the last operation completed:
			00: Successful completion
			01: Read-/Unprotect-Page: single error detected and corrected
			Write: operation addressed a write-protected page Erase-Page: protection violation Program: Page Buffer is unmodified Protection violation
			10: Read-/Unprotect-Page: two or more errors detected
			11: Write: attempt to write to another page before programming current page
			Erase-Page/Program: page write count has exceeded the 10-year retention threshold
UNPROTECTPAGE	1	In	When asserted, the page addressed is copied into the Page Buffer and the Page Buffer is made writable.
WD[31:0]	32	In	Write data
WEN	1	In	When asserted, stores WD in the page buffer.

All flash memory block input signals are active high, except for RESET.



Device Architecture

RAM512X18 exhibits slightly different behavior from RAM4K9, as it has dedicated read and write ports.

#### WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-30).

#### Table 2-30 • Aspect Ratio Settings for WW[1:0]

WW[1:0]	RW[1:0]	D×W
01	01	512×9
10	10	256×18
00, 11	00, 11	Reserved

#### WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, then RD[17:9] are undefined.

#### WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

#### WCLK and RCLK

These signals are the write and read clocks, respectively. They are both active high.

#### WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

#### RESET

This active low signal resets the output to zero, disables reads and/or writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

#### PIPE

This signal is used to specify pipelined read on the output. A Low on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

#### Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge or by separate clocks, by port.

Fusion devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the Fusion development tools, without performance penalty.

Signal Name	Number of Bits	Direction	Function	Location of Details
AG6	1	Output		Analog Quad
AT6	1	Input		Analog Quad
ATRETURN67	1	Input	Temperature monitor return shared by Analog Quads 6 and 7	Analog Quad
AV7	1	Input	Analog Quad 7	Analog Quad
AC7	1	Input		Analog Quad
AG7	1	Output		Analog Quad
AT7	1	Input		Analog Quad
AV8	1	Input	Analog Quad 8	Analog Quad
AC8	1	Input		Analog Quad
AG8	1	Output		Analog Quad
AT8	1	Input		Analog Quad
ATRETURN89	1	Input	Temperature monitor return shared by Analog Quads 8 and 9	Analog Quad
AV9	1	Input	Analog Quad 9	Analog Quad
AC9	1	Input		Analog Quad
AG9	1	Output		Analog Quad
AT9	1	Input		Analog Quad
RTCMATCH	1	Output	МАТСН	RTC
RTCPSMMATCH	1	Output	MATCH connected to VRPSM	RTC
RTCXTLMODE[1:0]	2	Output	Drives XTLOSC RTCMODE[1:0] pins	RTC
RTCXTLSEL	1	Output	Drives XTLOSC MODESEL pin	RTC
RTCCLK	1	Input	RTC clock input	RTC

#### Table 2-36 • Analog Block Pin Description (continued)

## **Analog Quad**

With the Fusion family, Microsemi introduces the Analog Quad, shown in Figure 2-65 on page 2-81, as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending it to the ADC for conversion into a digital signal. To maximize the usefulness of the Analog Quad, the analog input signals can also be configured as LVTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block, and its input pin is named AV. It contains a twochannel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler can be configured to accept analog signals between -12 V and 0 or between 0 and +12 V. The prescaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin can also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than 1  $\Omega$ ) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage that can then be read using the ADC.



To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least  $t_{CMSLO}$  in order to discharge the previous measurement. Then CMSTB must be asserted high for at least  $t_{CMSET}$  prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is de-asserted by the AB macro. Note that the minimum sample time cannot be less than  $t_{CMSHI}$ . Figure 2-71 shows the timing diagram of CMSTB in relationship with the ADC control signals.



Figure 2-71 • Timing Diagram for Current Monitor Strobe

Figure 2-72 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050  $\Omega$  sense resistor, The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$||| = (ADC \times V_{AREF}) / (10 \times 2^{N} \times R_{sense})$$

EQ 3

where

I is the current flowing through the sense resistor

ADC is the result from the ADC

VAREF is the Reference voltage

N is the number of bits

Rsense is the resistance of the sense resistor



#### Figure 2-90 • Input Setup Time

#### Standard Conversion



#### Notes:

1. Refer to EQ 20 on page 2-109 for the calculation on the sample time,  $t_{SAMPLE}$ .

2. See EQ 23 on page 2-109 for calculation of the conversion time,  $t_{CONV}$ .

3. Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period

Figure 2-91 • Standard Conversion Status Signal Timing Diagram



**Analog System Characteristics** 

#### Table 2-49 • Analog Channel Specifications

#### Commercial Temperature Range Conditions, T<sub>J</sub> = 85°C (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Voltage Monitor	Using Analog Pads AV,	AC and AT (using prescaler)			l	
	Input Voltage (Prescaler)	Refer to Table 3-2 on page 3-3				
VINAP	Uncalibrated Gain and Offset Errors	Refer to Table 2-51 on page 2-122				
	Calibrated Gain and Offset Errors	Refer to Table 2-52 on page 2-123				
	Bandwidth1				100	KHz
	Input Resistance	Refer to Table 3-3 on page 3-4				
	Scaling Factor	Prescaler modes (Table 2-57 on page 2-130)				
	Sample Time		10			μs
<b>Current Monitor</b>	Using Analog Pads AV	and AC		•		
VRSM <sup>1</sup>	Maximum Differential Input Voltage				VAREF / 10	mV
	Resolution	Refer to "Current Monitor" section				
	Common Mode Range				- 10.5 to +12	V
CMRR	Common Mode Rejection Ratio	DC – 1 KHz		60		dB
		1 KHz - 10 KHz		50		dB
		> 10 KHz		30		dB
t <sub>CMSHI</sub>	Strobe High time		ADC conv. time		200	μs
t <sub>CMSHI</sub>	Strobe Low time		5			μs
t <sub>CMSHI</sub>	Settling time		0.02			μs
	Accuracy	Input differential voltage > 50 mV			-2 -(0.05 x VRSM) to +2 + (0.05 x VRSM)	mV

Notes:

1. VRSM is the maximum voltage drop across the current sense resistor.

2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.

- 3. VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.
- 4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
- 5. The temperature offset is a fixed positive value.
- 6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
- 7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.



Table 2-61 details the settings available to either power down or enable the prescaler associated with the analog inputs AV, AC, and AT.

#### Table 2-61 • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Control Lines Bx[7]	Prescaler Op Amp
0	Power-down
1	Operational

Table 2-62 details the settings available to enable the Current Monitor Block associated with the AC pin.

#### Table 2-62 • Current Monitor Input Switch Control Truth Table—AV (x = 0)

Control Lines B0[4]	Current Monitor Input Switch
0	Off
1	On

Table 2-63 details the settings available to configure the drive strength of the gate drive when not in highdrive mode.

#### Table 2-63 • Low-Drive Gate Driver Current Truth Table (AG)

Control Lines B2[3]	Control Lines B2[2]	Current (µA)
0	0	1
0	1	3
1	0	10
1	1	30

Table 2-64 details the settings available to set the polarity of the gate driver (either p-channel- or n-channel-type devices).

#### Table 2-64 • Gate Driver Polarity Truth Table (AG)

Control Lines B2[6]	Gate Driver Polarity	
0	Positive	
1	Negative	

Table 2-65 details the settings available to turn on the Gate Driver and set whether high-drive mode is on or off.

#### Table 2-65 • Gate Driver Control Truth Table (AG)

Control Lines B2[7]	GDON	Gate Driver
0	0	Off
0	1	Low drive on
1	0	Off
1	1	High drive on

Table 2-66 details the settings available to turn on and off the chip internal temperature monitor.

Note: For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

#### Table 2-66 • Internal Temperature Monitor Control Truth Table

Control Lines B2[0]	PDTMB	Chip Internal Temperature Monitor
0	0	Off
1	1	On

## Features Supported on Pro I/Os

Table 2-72 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

#### Table 2-72 • Fusion Pro I/O Features

Feature	Description
Single-ended and voltage- referenced transmitter	<ul> <li>Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion)</li> </ul>
features	Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.
	Weak pull-up and pull-down
	Two slew rates
	<ul> <li>Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge); see "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-149 for more information</li> </ul>
	Five drive strengths
	5 V-tolerant receiver ("5 V Input Tolerance" section on page 2-144)
	<ul> <li>LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-148)</li> </ul>
	High performance (Table 2-76 on page 2-143)
Single-ended receiver features	Schmitt trigger option
	ESD protection
	<ul> <li>Programmable delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)</li> </ul>
	High performance (Table 2-76 on page 2-143)
	<ul> <li>Separate ground planes, GND/GNDQ, for input buffers only to avoid output- induced noise in the input circuitry</li> </ul>
Voltage-referenced differential receiver features	<ul> <li>Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)</li> </ul>
	High performance (Table 2-76 on page 2-143)
	<ul> <li>Separate ground planes, GND/GNDQ, for input buffers only to avoid output- induced noise in the input circuitry</li> </ul>
CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL	<ul> <li>Two I/Os and external resistors are used to provide a CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter solution.</li> </ul>
transmitter	Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.
	Weak pull-up and pull-down
	Fast slew rate
LVDS/LVPECL differential	ESD protection
receiver teatures	High performance (Table 2-76 on page 2-143)
	<ul> <li>Programmable delay: 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)</li> </ul>
	<ul> <li>Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry</li> </ul>

Fusion Family of Mixed Signal FPGAs

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 k $\Omega$  (or lower) output drive resistance at hot insertion, and 1 k $\Omega$  (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

- 1. Grounds
- 2. Powers, I/Os, other pins

## **Cold-Sparing Support**

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks and standard I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If Standard I/O banks are used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the standard I/O buffers do not have built-in I/O clamp diodes.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull down resistor and driven in the opposite direction. A small static current is induced on each IO pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Please refer to Table 2-95 on page 2-169, Table 2-96 on page 2-169, and Table 2-97 on page 2-171 for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTL 3.3 V, pull-up resistor is ~45 k $\Omega$  and the resulting current is equal to 3.3 V / 45 k $\Omega$  = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven low
- Input buffers with pull-down, driven high
- Bidirectional buffers with pull-up, driven low
- · Bidirectional buffers with pull-down, driven high
- Output buffers with pull-up, driven low
- Output buffers with pull-down, driven high
- Tristate buffers with pull-up, driven low
- · Tristate buffers with pull-down, driven high



## **Electrostatic Discharge (ESD) Protection**

Fusion devices are tested per JEDEC Standard JESD22-A114-B.

Fusion devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to VCCI. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the Off state, except when transient voltage is significantly above VCCI or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 2-75 and Table 2-76 on page 2-143 for more information about I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

	Clamp Diode		Hot Insertion		5 V Input 1	Tolerance <sup>1</sup>	Input	Output
I/O Assignment	Standard I/O	Advanced I/O	Standard I/O	Advanced I/O	Standard I/O	Advanced I/O	Buffer	Buffer
3.3 V LVTTL/LVCMOS	No	Yes	Yes	No	Yes <sup>1</sup>	Yes <sup>1</sup>	Enabled/I	Disabled
3.3 V PCI, 3.3 V PCI-X	N/A	Yes	N/A	No	N/A	Yes <sup>1</sup>	Enabled/Disabled	
LVCMOS 2.5 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V	N/A	Yes	N/A	No	N/A	Yes <sup>2</sup>	Enabled/I	Disabled
LVCMOS 1.8 V	No	Yes	Yes	No	No	No	Enabled/I	Disabled
LVCMOS 1.5 V	No	Yes	Yes	No	No	No	Enabled/I	Disabled
Differential, LVDS/BLVDS/M- LVDS/ LVPECL <sup>3</sup>	N/A	Yes	N/A	No	N/A	No	Enabled/I	Disabled

Table 2-75 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities

Notes:

1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.

2. Can be implemented with an external resistor and an internal clamp diode.

3. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.

#### Table 2-76 • Fusion Pro I/O – Hot-Swap and 5 V Input Tolerance Capabilities

I/O Assignment	Clamp Diode	Hot Insertion	5 V Input Tolerance	Input Buffer	Output Buffer	
3.3 V LVTTL/LVCMOS	No	Yes	Yes <sup>1</sup>	Enabled	l/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes <sup>1</sup>	Enabled/Disabled		
LVCMOS 2.5 V <sup>3</sup>	No	Yes	No	Enabled/Disabled		
LVCMOS 2.5 V / 5.0 V <sup>3</sup>	Yes	No	Yes <sup>2</sup>	Enabled/Disabled		
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled		
LVCMOS 1.5 V	No	Yes	No	Enabled/Disabled		
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled		
Differential, LVDS/BLVDS/M-LVDS/LVPECL <sup>4</sup>	No	Yes	No	Enabled	l/Disabled	

Notes:

1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.

- 2. Can be implemented with an external resistor and an internal clamp diode.
- 3. In the SmartGen, FlashROM, Flash Memory System Builder, and Analog System Builder User Guide, select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V / 0 standard.

4. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.



Device Architecture

#### Table 2-121 • 1.8 V LVCMOS High Slew

Commercial Temperature Range Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Applicable to Pro I/Os

Drive	Speed													
Strength	Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	-1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	-2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	-1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	-2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
8 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	-1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	-2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
12 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	-1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	-2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	-1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	-2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

#### Table 2-122 • 1.8 V LVCMOS Low Slew

Commercial Temperature Range Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Advanced I/Os

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
2 mA	Std.	0.66	15.53	0.04	1.31	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	-1	0.56	13.21	0.04	1.11	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	-2 <sup>2</sup>	0.49	11.60	0.03	0.98	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns
4 mA	Std.	0.66	10.48	0.04	1.31	0.43	10.41	10.48	3.23	2.73	12.65	12.71	ns
	-1	0.56	8.91	0.04	1.11	0.36	8.86	8.91	2.75	2.33	10.76	10.81	ns
	-2	0.49	7.82	0.03	0.98	0.32	7.77	7.82	2.41	2.04	9.44	9.49	ns
8 mA	Std.	0.66	8.05	0.04	1.31	0.43	8.20	7.84	3.54	3.27	10.43	10.08	ns
	-1	0.56	6.85	0.04	1.11	0.36	6.97	6.67	3.01	2.78	8.88	8.57	ns
	-2	0.49	6.01	0.03	0.98	0.32	6.12	5.86	2.64	2.44	7.79	7.53	ns
12 mA	Std.	0.66	7.50	0.04	1.31	0.43	7.64	7.30	3.61	3.41	9.88	9.53	ns
	-1	0.56	6.38	0.04	1.11	0.36	6.50	6.21	3.07	2.90	8.40	8.11	ns
	-2	0.49	5.60	0.03	0.98	0.32	5.71	5.45	2.69	2.55	7.38	7.12	ns
16 mA	Std.	0.66	7.29	0.04	1.31	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	-1	0.56	6.20	0.04	1.11	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	-2	0.49	5.45	0.03	0.98	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



# 3 – DC and Power Characteristics

# **General Specifications**

## **Operating Conditions**

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-3.

Symbol	Parameter	Commercial	Industrial	Units		
VCC	DC core supply voltage	-0.3 to 1.65	–0.3 to 1.65	V		
VJTAG	JTAG DC voltage	-0.3 to 3.75	-0.3 to 3.75	V		
VPUMP	Programming voltage	-0.3 to 3.75	-0.3 to 3.75	V		
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	-0.3 to 1.65	V		
VCCI	DC I/O output buffer supply voltage	-0.3 to 3.75	-0.3 to 3.75	V		
VI	I/O input voltage <sup>1</sup>	<ul> <li>-0.3 V to 3.6 V (when I/O hot insertion mode is enabled)</li> <li>-0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)</li> </ul>				
VCC33A	+3.3 V power supply	–0.3 to 3.75 <sup>2</sup>	–0.3 to 3.75 <sup>2</sup>	V		
VCC33PMP	+3.3 V power supply	-0.3 to 3.75 <sup>2</sup>	-0.3 to 3.75 <sup>2</sup>	V		
VAREF	Voltage reference for ADC	-0.3 to 3.75	-0.3 to 3.75	V		
VCC15A	Digital power supply for the analog system	-0.3 to 1.65	–0.3 to 1.65	V		
VCCNVM	Embedded flash power supply	-0.3 to 1.65	-0.3 to 1.65	V		
VCCOSC	Oscillator power supply	-0.3 to 3.75	-0.3 to 3.75	V		

#### Table 3-1 • Absolute Maximum Ratings

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-4.

2. Analog data not valid beyond 3.65 V.

3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.

4. For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.

Pads	Pad Configuration	Prescaler Range	Input Resistance to Ground	
AV, AC	Analog Input (direct input to ADC)	-	2 kΩ (typical)	
		-	> 10 MΩ	
	Analog Input (positive prescaler)	+16 V to +2 V	1 MΩ (typical)	
		+1 V to +0.125 V	> 10 MΩ	
	Analog Input (negative prescaler)	–16 V to –2 V	1 MΩ (typical)	
		–1 V to –0.125 V	> 10 MΩ	
	Digital input	+16 V to +2 V	1 MΩ (typical)	
	Current monitor	+16 V to +2 V	1 MΩ (typical)	
		–16 V to –2 V	1 MΩ (typical)	
AT	Analog Input (direct input to ADC)	-	1 MΩ (typical)	
	Analog Input (positive prescaler)	+16 V, +4 V	1 MΩ (typical)	
	Digital input	+16 V, +4 V	1 MΩ (typical)	
	Temperature monitor	+16 V, +4 V	> 10 MΩ	

#### Table 3-3 • Input Resistance of Analog Pads

## Table 3-4 • Overshoot and Undershoot Limits <sup>1</sup>

vccı	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle <sup>2</sup>	Maximum Overshoot/ Undershoot <sup>2</sup>
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at a junction temperature of 85°C.

2. The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.



Package Pin Assignments

	FG484		FG484		
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND	AA14	AG7	AG7
A2	VCC	NC	AA15	AG8	AG8
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0	AA16	GNDA	GNDA
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0	AA17	AG9	AG9
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0	AA18	VAREF	VAREF
A6	IO07NDB0V1	IO07NDB0V1	AA19	VCCIB2	VCCIB2
A7	IO07PDB0V1	IO07PDB0V1	AA20	PTEM	PTEM
A8	IO10PDB0V1	IO09PDB0V1	AA21	GND	GND
A9	IO14NDB0V1	IO13NDB0V2	AA22	VCC	NC
A10	IO14PDB0V1	IO13PDB0V2	AB1	GND	GND
A11	IO17PDB1V0	IO24PDB1V0	AB2	VCC	NC
A12	IO18PDB1V0	IO26PDB1V0	AB3	NC	IO94NSB4V0
A13	IO19NDB1V0	IO27NDB1V1	AB4	GND	GND
A14	IO19PDB1V0	IO27PDB1V1	AB5	VCC33N	VCC33N
A15	IO24NDB1V1	IO35NDB1V2	AB6	AT0	AT0
A16	IO24PDB1V1	IO35PDB1V2	AB7	ATRTN0	ATRTN0
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2	AB8	AT1	AT1
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2	AB9	AT2	AT2
A19	IO29NDB1V1	IO43NDB1V2	AB10	ATRTN1	ATRTN1
A20	IO29PDB1V1	IO43PDB1V2	AB11	AT3	AT3
A21	VCC	NC	AB12	AT6	AT6
A22	GND	GND	AB13	ATRTN3	ATRTN3
AA1	VCC	NC	AB14	AT7	AT7
AA2	GND	GND	AB15	AT8	AT8
AA3	VCCIB4	VCCIB4	AB16	ATRTN4	ATRTN4
AA4	VCCIB4	VCCIB4	AB17	AT9	AT9
AA5	PCAP	PCAP	AB18	VCC33A	VCC33A
AA6	AG0	AG0	AB19	GND	GND
AA7	GNDA	GNDA	AB20	NC	IO76NPB2V0
AA8	AG1	AG1	AB21	VCC	NC
AA9	AG2	AG2	AB22	GND	GND
AA10	GNDA	GNDA	B1	VCC	NC
AA11	AG3	AG3	B2	GND	GND
AA12	AG6	AG6	B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
AA13	GNDA	GNDA	B4	GND	GND



Package Pin Assignments

FG676							
Pin Number AFS1500 Function							
W25	NC						
W26	GND						
Y1	NC						
Y2	NC						
Y3	GEB1/IO89PDB4V0						
Y4	GEB0/IO89NDB4V0						
Y5	VCCIB4						
Y6	GEA1/IO88PDB4V0						
Y7	GEA0/IO88NDB4V0						
Y8	GND						
Y9	VCC33PMP						
Y10	NC						
Y11	VCC33A						
Y12	AG4						
Y13	AT4						
Y14	ATRTN2						
Y15	AT5						
Y16	VCC33A						
Y17	NC						
Y18	VCC33A						
Y19	GND						
Y20	TMS						
Y21	VJTAG						
Y22	VCCIB2						
Y23	TRST						
Y24	TDO						
Y25	NC						
Y26	NC						

Revision	Changes	Page				
Revision 3 (continued)	The "RC Oscillator" section was revised to correct a sentence that did not differentiate accuracy for commercial and industrial temperature ranges, which is given in Table 2-9 • Electrical Characteristics of RC Oscillator (SAR 33722).	2-19				
	Figure 2-57 • FIFO Read and Figure 2-58 • FIFO Write are new (SAR 34840).					
	The first paragraph of the "Offset" section was removed; it was intended to be replaced by the paragraph following it (SAR 22647).	2-95				
	IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions (SAR 39813).	2-164				
	The drive strength, IOL, and IOH for 3.3 V GTL and 2.5 V GTL were changed from 25 mA to 20 mA in the following tables (SAR 37373):					
	Table 2-86         Summary of Maximum and Minimum DC Input and Output Levels           Applicable to Commercial and Industrial Conditions,	2-164				
	Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings	2-167				
	Table 2-96 • I/O Output Buffer Maximum Resistances 1	2-169				
	Table 2-138 • Minimum and Maximum DC Input and Output Levels	2-199				
	Table 2-141 • Minimum and Maximum DC Input and Output Levels	2-200				
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34800): "It uses a 5 V-tolerant input buffer and push-pull output buffer."	2-181				
	Corrected the inadvertent error in maximum values for LVPECL VIH and VIL and revised them to "3.6" in Table 2-171 • Minimum and Maximum DC Input and Output Levels, making these consistent with Table 3-1 • Absolute Maximum Ratings, and Table 3-4 • Overshoot and Undershoot Limits 1 (SAR 37687).	2-211				
	The maximum frequency for global clock parameter was removed from Table 2-5 • AFS1500 Global Resource Timing through Table 2-8 • AFS090 Global Resource Timing because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36955).	2-16 to 2-17				
Revision 2 (March 2012)	The phrase "without debug" was removed from the "Soft ARM Cortex-M1 Fusion Devices (M1)" section (SAR 21390).	I				
	The "In-System Programming (ISP) and Security" section, "Security" section, "Flash Advantages" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34679).	l, 1-2, 2-228				
	The Y security option and Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34721).	III				
	The "Specifying I/O States During Programming" section is new (SAR 34693).	1-9				
	The following information was added before Figure 2-17 • XTLOSC Macro:	2-20				
	In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating (SAR 24119).					
	Table 2-12 • Fusion CCC/PLL Specification was updated. A note was added indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34814).	2-28				

Revision	Changes	Page
Revision 2 (continued)	The prescalar range for the 'Analog Input (direct input to ADC)" configurations was removed as inapplicable for direct inputs. The input resistance for direct inputs is covered in Table 2-50 • ADC Characteristics in Direct Input Mode (SAR 31201).	2-120
	The "Examples" for calibrating accuracy for ADC channels were revised and corrected to make them consistent with terminology in the associated tables (SARs 36791, 36773).	2-124
	A note was added to Table 2-56 • Analog Quad ACM Byte Assignment and the introductory text for Table 2-66 • Internal Temperature Monitor Control Truth Table, stating that for the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set (SAR 34418).	2-129, 2-131
	$t_{\text{DOUT}}$ was corrected to $t_{\text{DIN}}$ in Figure 2-116 $\bullet$ Input Buffer Timing Model and Delays (example) (SAR 37115).	2-161
	The formulas in the table notes for Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34751).	2-171
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34877).	2-175
	The following notes were removed from Table 2-168 • Minimum and Maximum DC Input and Output Levels (SAR 34808): ±5%	2-209
	Differential input voltage = ±350 mV	
	An incomplete, duplicate sentence was removed from the end of the "GNDAQ Ground (analog quiet)" pin description (SAR 30185).	2-223
	Information about configuration of unused I/Os was added to the "User Pins" section (SAR 32642).	2-225
	The following information was added to the pin description for "XTAL1 Crystal Oscillator Circuit Input" and "XTAL2 Crystal Oscillator Circuit Input" (SAR 24119).	2-227
	The input resistance to ground value in Table 3-3 • Input Resistance of Analog Pads for Analog Input (direct input to ADC), was corrected from 1 M $\Omega$ (typical) to 2 k $\Omega$ (typical) (SAR 34371).	3-4
	The Storage Temperature column in Table 3-5 • FPGA Programming, Storage, and Operating Limits stated Min. $T_J$ twice for commercial and industrial product grades and has been corrected to Min. $T_J$ and Max. $T_J$ (SAR 29416).	3-5
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Dynamic Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the <i>Fusion FPGA Fabric User's Guide</i> (SAR 34741).	3-24
	Package names used in the "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 36612).	4-1
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Fusion Device Status" table indicates the status for each device in the device family.	N/A