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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	
Number of Logic Elements/Cells	
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs250-1fgg256i

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Figure 2-9 • Efficient Long-Line Resources

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-14 indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel Fusion Devices* application note.



Figure 2-14 • Clock Aggregation Tree Architecture

1.5 V Voltage Regulator

The 1.5 V voltage regulator uses an external pass transistor to generate 1.5 V from a 3.3 V supply. The base of the pass transistor is tied to PTBASE, the collector is tied to 3.3 V, and an emitter is tied to PTBASE and the 1.5 V supplies of the Fusion device. Figure 2-27 on page 2-31 shows the hook-up of the 1.5 V voltage regulator to an external pass transistor.

Microsemi recommends using a PN2222A or 2N2222A transistor. The gain of such a transistor is approximately 25, with a maximum base current of 20 mA. The maximum current that can be supported is 0.5 A. Transistors with different gain can also be used for different current requirements.

Table 2-18 • Electrical Characteristics

Symbol	Parameter	Condition		Min	Typical	Max	Units
VOUT	Output Voltage	Tj = 25°C		1.425	1.5	1.575	V
ICC33A	Operation Current	Tj = 25°C	ILOAD = 1 mA		11		mA
			ILOAD = 100 mA		11		mA
			ILOAD = 0.5 A		30		mA
∆VOUT	Load Regulation	Tj = 25°C	ILOAD = 1 mA to 0.5 A		90		mV
	Line Regulation	Tj = 25°C	VCC33A = 2.97 V to 3.63 V				
			ILOAD = 1 mA		10.6		mV/V
			VCC33A = 2.97 V to 3.63 V				
			ILOAD = 100 mA		12.1		mV/V
∆VOUT			VCC33A = 2.97 V to 3.63 V		10.0		
			ILOAD = 500 mA		10.6		mV/V
	Dropout Voltage*	Tj = 25⁰C	ILOAD = 1 mA		0.63		V
			ILOAD = 100 mA		0.84		V
			ILOAD = 0.5 A		1.35		V
IPTBASE	PTBase Current	Tj = 25°C	ILOAD = 1 mA		48		μA
			ILOAD = 100 mA		736		μA
			ILOAD = 0.5 A		12	20	mA

VCC33A = 3.3 V

Note: *Data collected with 2N2222A.



RAM512X18 exhibits slightly different behavior from RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-30).

Table 2-30 • Aspect Ratio Settings for WW[1:0]

WW[1:0]	RW[1:0]	D×W
01	01	512×9
10	10	256×18
00, 11	00, 11	Reserved

WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, then RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They are both active high.

WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

RESET

This active low signal resets the output to zero, disables reads and/or writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

PIPE

This signal is used to specify pipelined read on the output. A Low on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge or by separate clocks, by port.

Fusion devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the Fusion development tools, without performance penalty.



To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least t_{CMSLO} in order to discharge the previous measurement. Then CMSTB must be asserted high for at least t_{CMSET} prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is de-asserted by the AB macro. Note that the minimum sample time cannot be less than t_{CMSHI} . Figure 2-71 shows the timing diagram of CMSTB in relationship with the ADC control signals.



Figure 2-71 • Timing Diagram for Current Monitor Strobe

Figure 2-72 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050 Ω sense resistor, The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$||| = (ADC \times V_{AREF}) / (10 \times 2^{N} \times R_{sense})$$

EQ 3

where

I is the current flowing through the sense resistor

ADC is the result from the ADC

VAREF is the Reference voltage

N is the number of bits

Rsense is the resistance of the sense resistor

		Tot Er	al Cha ror (LS	nnel SB)	Chann E	el Inpu rror (LS	t Offset SB)	Chani	nel Input Error (m\	Offset /)	Channel Gain Erro (%FSR)		
Analog Pad	Prescaler Range (V)	Neg. Max.	Med.	Pos. Max.	Neg Max	Med.	Pos. Max.	Neg. Max.	Med.	Pos. Max.	Min.	Тур.	Max.
Positi	ve Range						ADC in	10-Bit N	lode				
AV, AC	16	-22	-2	12	-11	-2	14	-169	-32	224	3	0	-3
	8	-40	-5	17	-11	-5	21	-87	-40	166	2	0	-4
	4	-45	-9	24	-16	-11	36	-63	-43	144	2	0	-4
	2	-70	-19	33	-33	-20	66	-66	-39	131	2	0	-4
	1	-25	-7	5	-11	-3	26	-11	-3	26	3	-1	-3
	0.5	-41	-12	8	-12	-7	38	-6	-4	19	3	-1	-3
	0.25	-53	-14	19	-20	-14	40	-5	-3	10	5	0	-4
	0.125	-89	-29	24	-40	-28	88	-5	-4	11	7	0	-5
AT	16	-3	9	15	-4	0	4	-64	5	64	1	0	-1
	4	-10	2	15	-11	-2	11	-44	-8	44	1	0	-1
Negati	ve Range						ADC in	10-Bit N	lode				
AV, AC	16	-35	-10	9	-24	-6	9	-383	-96	148	5	-1	-6
	8	-65	-19	12	-34	-12	9	-268	-99	75	5	-1	-5
	4	-86	-28	21	-64	-24	19	-254	-96	76	5	-1	-6
	2	-136	-53	37	-115	-42	39	-230	-83	78	6	-2	-7
	1	-98	-35	8	-39	-8	15	-39	-8	15	10	-3	-10
	0.5	-121	-46	7	-54	-14	18	-27	-7	9	10	-4	-11
	0.25	-149	-49	19	-72	-16	40	–18	-4	10	14	-4	-12
	0.125	-188	-67	38	-112	-27	56	-14	-3	7	16	-5	-14

Table 2-51 • Uncalibrated Analog Channel Accuracy*Worst-Case Industrial Conditions, TJ = 85°C

Note: *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.



Similarly,

Min. Output Voltage = (Max. Negative input offset) + (Input Voltage x Max. Negative Channel Gain) = $(-88 \text{ mV}) + (5 \text{ V} \times 0.96) = 4.712 \text{ V}$

Calculating Accuracy for a Calibrated Analog Channel

Formula

For a given prescaler range, EQ 31 gives the output voltage.

Output Voltage = Channel Error in V + Input Voltage

EQ 31

where

Channel Error in V = Total Channel Error in LSBs x Equivalent voltage per LSB

Example

Input Voltage = 5 VChosen Prescaler range = 8 V range Refer to Table 2-52 on page 2-123.

Max. Output Voltage = Max. Positive Channel Error in V + Input Voltage Max. Positive Channel Error in V = (6 LSB) × (8 mV per LSB in 10-bit mode) = 48 mV Max. Output Voltage = 48 mV + 5 V = **5.048 V**

Similarly,

Min. Output Voltage = Max. Negative Channel Error in V + Input Voltage = (-48 mV) + 5 V = 4.952 V

Calculating LSBs from a Given Error Budget

Formula

For a given prescaler range, LSB count = ± (Input Voltage × Required % error) / (Equivalent voltage per LSB)

Example

Input Voltage = $3.3 \vee$ Required error margin= 1% Refer to Table 2-52 on page 2-123. Equivalent voltage per LSB = 16 mV for a 16V prescaler, with ADC in 10-bit mode LSB Count = $\pm (5.0 \vee \times 1\%) / (0.016)$ LSB Count = ± 3.125 Equivalent voltage per LSB = 8 mV for an $8 \vee$ prescaler, with ADC in 10-bit mode LSB Count = $\pm (5.0 \vee \times 1\%) / (0.008)$ LSB Count = $\pm (5.0 \vee \times 1\%) / (0.008)$ LSB Count = ± 6.25 The $8 \vee$ prescaler satisfies the calculated LSB count accuracy requirement (see Table 2-52 on page 2-123).



Analog Quad ACM Description

Table 2-56 maps out the ACM space associated with configuration of the Analog Quads within the Analog Block. Table 2-56 shows the byte assignment within each quad and the function of each bit within each byte. Subsequent tables will explain each bit setting and how it corresponds to a particular configuration. After 3.3 V and 1.5 V are applied to Fusion, Analog Quad configuration registers are loaded with default settings until the initialization and configuration state machine changes them to user-defined settings.

Table	2-56 •	Analog	Quad	Bvte /	Assianme	nt
1 4010	200	Analog	auuu .		Rooiginno	

Byte	Bit	Signal (Bx)	Function	Default Setting
Byte 0	0	B0[0]	Scaling factor control – prescaler	Highest voltage range
(AV)	1	B0[1]		
	2	B0[2]	-	
	3	B0[3]	Analog MUX select	Prescaler
	4	B0[4]	Current monitor switch	Off
	5	B0[5]	Direct analog input switch	Off
	6	B0[6]	Selects V-pad polarity	Positive
	7	B0[7]	Prescaler op amp mode	Power-down
Byte 1	0	B1[0]	Scaling factor control – prescaler	Highest voltage range
(AC)	1	B1[1]		
	2	B1[2]		
	3	B1[3]	Analog MUX select	Prescaler
	4	B1[4]		
	5	B1[5]	Direct analog input switch	Off
	6	B1[6]	Selects C-pad polarity	Positive
	7	B1[7]	Prescaler op amp mode	Power-down
Byte 2	0	B2[0]	Internal chip temperature monitor *	Off
(AG)	1	B2[1]	Spare	-
	2	B2[2]	Current drive control	Lowest current
	3	B2[3]		
	4	B2[4]	Spare	-
	5	B2[5]	Spare	-
	6	B2[6]	Selects G-pad polarity	Positive
	7	B2[7]	Selects low/high drive	Low drive
Byte 3	0	B3[0]	Scaling factor control – prescaler	Highest voltage range
(AT)	1	B3[1]	-	
	2	B3[2]	-	
	3	B3[3]	Analog MUX select	Prescaler
	4	B3[4]		
	5	B3[5]	Direct analog input switch	Off
	6	B3[6]	_	-
	7	B3[7]	Prescaler op amp mode	Power-down

Note: *For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-100 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-100) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O register combining must satisfy some rules.



Note: Fusion I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-139 for more information).

Figure 2-100 • I/O Block Logical Representation



Table 2-115 • 2.5 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Advanced I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
4 mA	Std.	0.66	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	-1	0.56	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	-2	0.49	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
8 mA	Std.	0.66	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	-1	0.56	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	-2	0.49	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	-1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	-2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
16 mA	Std.	0.66	3.35	0.04	1.31	0.43	3.41	3.06	3.36	3.55	5.65	5.30	ns
	-1	0.56	2.85	0.04	1.11	0.36	2.90	2.60	2.86	3.02	4.81	4.51	ns
	-2	0.49	2.50	0.03	0.98	0.32	2.55	2.29	2.51	2.65	4.22	3.96	ns
24 mA	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	-1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	-2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-116 • 2.5 V LVCMOS Low Slew

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	-1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	-2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
4 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	-1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	-2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
6 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	-1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	-2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns
8 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	-1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	-2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns



1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.8 V applications. It uses a 1.8 V input buffer and push-pull output buffer.

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
Applicable	to Pro I/0) Banks										
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	16	16	74	91	10	10
Applicable	to Advar	nced I/O Banl	(S									
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	16	16	74	91	10	10
Applicable	to Stand	ard I/O Banks	5			•						
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4	22	17	10	10

Table 2-118 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-121 • AC Loading

Table 2-119 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input Low (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.8	0.9	-	35

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.



Table 2-121 • 1.8 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Applicable to Pro I/Os

Drive	Speed													
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	-1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	-2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	-1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	-2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
8 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	-1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	-2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
12 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	-1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	-2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	-1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	-2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Timing Characteristics

Table 2-128 • 1.5 V LVCMOS Low Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Pro I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	-1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	-2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	-1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	-2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
8 mA	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	-1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	-2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
12 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	-1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	-2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-129 • 1.5 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Pro I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOU} T	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	-1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	-2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	-1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	-2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
8 mA	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	-1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	-2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
12 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	-1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	-2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-147 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
33 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	-	33	33	124	169	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-127 • AC Loading

Table 2-148 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

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Table 2-149 • 2.5 V GTL+
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Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
-1	0.56	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
-2	0.49	1.65	0.03	1.13	0.32	1.68	1.57			3.35	4.34	ns



IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/Os" section on page 2-132 for more details.

Timing Characteristics

Table 2-186 • JTAG 1532

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{DISU}	Test Data Input Setup Time	0.50	0.57	0.67	ns
t _{DIHD}	Test Data Input Hold Time	1.00	1.13	1.33	ns
t _{TMSSU}	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t _{TMDHD}	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t _{TCK2Q}	Clock to Q (data out)	6.00	6.80	8.00	ns
t _{RSTB2Q}	Reset to Q (data out)	20.00	22.67	26.67	ns
F _{TCKMAX}	TCK Maximum Frequency	25.00	22.00	19.00	MHz
t _{TRSTREM}	ResetB Removal Time	0.00	0.00	0.00	ns
t _{TRSTREC}	ResetB Recovery Time	0.20	0.23	0.27	ns
t _{TRSTMPW}	ResetB Minimum Pulse	TBD	TBD	TBD	ns



 P_{S-CELL} = N_{S-CELL} * (PAC5 + (α_1 / 2) * PAC6) * F_{CLK}

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

 $P_{S-CELL} = 0 W$

Combinatorial Cells Dynamic Contribution—P_{C-CELL}

Operating Mode

 $P_{C-CELL} = N_{C-CELL} * (\alpha_1 / 2) * PAC7 * F_{CLK}$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

 $P_{C-CELL} = 0 W$

Routing Net Dynamic Contribution-PNET

Operating Mode

 $P_{NET} = (N_{S-CELL} + N_{C-CELL}) * (\alpha_1 / 2) * PAC8 * F_{CLK}$

N_{S-CELL} is the number VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

 $P_{NET} = 0 W$

I/O Input Buffer Dynamic Contribution—PINPUTS

Operating Mode

 $P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-16 on page 3-27.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

P_{INPUTS} = 0 W

I/O Output Buffer Dynamic Contribution—POUTPUTS

Operating Mode

 $\mathsf{P}_{\mathsf{OUTPUTS}} = \mathsf{N}_{\mathsf{OUTPUTS}} * (\alpha_2 / 2) * \beta_1 * \mathsf{PAC10} * \mathsf{F}_{\mathsf{CLK}}$

N_{OUTPUTS} is the number of I/O output buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-16 on page 3-27.

 β_1 is the I/O buffer enable rate—guidelines are provided in Table 3-17 on page 3-27.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

P_{OUTPUTS} = 0 W



Package Pin Assignments

	PQ208		PQ208				
Pin Number	AFS250 Function	AFS600 Function	Pin Number	AFS250 Function	AFS600 Function		
1	VCCPLA	VCCPLA	38	IO60NDB3V0	GEB0/IO62NDB4V0		
2	VCOMPLA	VCOMPLA	39	GND	GEA1/IO61PDB4V0		
3	GNDQ	GAA2/IO85PDB4V0	40	VCCIB3	GEA0/IO61NDB4V0		
4	VCCIB3	IO85NDB4V0	41	GEB2/IO59PDB3V0	GEC2/IO60PDB4V0		
5	GAA2/IO76PDB3V0	GAB2/IO84PDB4V0	42	IO59NDB3V0	IO60NDB4V0		
6	IO76NDB3V0	IO84NDB4V0	43	GEA2/IO58PDB3V0	VCCIB4		
7	GAB2/IO75PDB3V0	GAC2/IO83PDB4V0	44	IO58NDB3V0	GNDQ		
8	IO75NDB3V0	IO83NDB4V0	45	VCC	VCC		
9	NC	IO77PDB4V0	45	VCC	VCC		
10	NC	IO77NDB4V0	46	VCCNVM	VCCNVM		
11	VCC	IO76PDB4V0	47	GNDNVM	GNDNVM		
12	GND	IO76NDB4V0	48	GND	GND		
13	VCCIB3	VCC	49	VCC15A	VCC15A		
14	IO72PDB3V0	GND	50	PCAP	PCAP		
15	IO72NDB3V0	VCCIB4	51	NCAP	NCAP		
16	GFA2/IO71PDB3V0	GFA2/IO75PDB4V0	52	VCC33PMP	VCC33PMP		
17	IO71NDB3V0	IO75NDB4V0	53	VCC33N	VCC33N		
18	GFB2/IO70PDB3V0	GFC2/IO73PDB4V0	54	GNDA	GNDA		
19	IO70NDB3V0	IO73NDB4V0	55	GNDAQ	GNDAQ		
20	GFC2/IO69PDB3V0	VCCOSC	56	NC	AV0		
21	IO69NDB3V0	XTAL1	57	NC	AC0		
22	VCC	XTAL2	58	NC	AG0		
23	GND	GNDOSC	59	NC	AT0		
24	VCCIB3	GFC1/IO72PDB4V0	60	NC	ATRTN0		
25	GFC1/IO68PDB3V0	GFC0/IO72NDB4V0	61	NC	AT1		
26	GFC0/IO68NDB3V0	GFB1/IO71PDB4V0	62	NC	AG1		
27	GFB1/IO67PDB3V0	GFB0/IO71NDB4V0	63	NC	AC1		
28	GFB0/IO67NDB3V0	GFA1/IO70PDB4V0	64	NC	AV1		
29	VCCOSC	GFA0/IO70NDB4V0	65	AV0	AV2		
30	XTAL1	IO69PDB4V0	66	AC0	AC2		
31	XTAL2	IO69NDB4V0	67	AG0	AG2		
32	GNDOSC	VCC	68	AT0	AT2		
33	GEB1/IO62PDB3V0	GND	69	ATRTN0	ATRTN1		
34	GEB0/IO62NDB3V0	VCCIB4	70	AT1	AT3		
35	GEA1/IO61PDB3V0	GEC1/IO63PDB4V0	71	AG1	AG3		
36	GEA0/IO61NDB3V0	GEC0/IO63NDB4V0	72	AC1	AC3		
37	GEC2/IO60PDB3V0	GEB1/IO62PDB4V0	73	AV1	AV3		

	FG484		FG484				
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function		
H13	GND	GND	K4	IO75NDB4V0	IO110NDB4V0		
H14	VCCIB1	VCCIB1	K5	GND	GND		
H15	GND	GND	K6	NC	IO104NDB4V0		
H16	GND	GND	K7	NC	IO111NDB4V0		
H17	NC	IO53NDB2V0	K8	GND	GND		
H18	IO38PDB2V0	IO57PDB2V0	K9	VCC	VCC		
H19	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0	K10	GND	GND		
H20	VCCIB2	VCCIB2	K11	VCC	VCC		
H21	IO37NDB2V0	IO54NDB2V0	K12	GND	GND		
H22	IO37PDB2V0	IO54PDB2V0	K13	VCC	VCC		
J1	NC	IO112PPB4V0	K14	GND	GND		
J2	IO76NDB4V0	IO113NDB4V0	K15	GND	GND		
J3	GFB2/IO74PDB4V0	GFB2/IO109PDB4V0	K16	IO40NDB2V0	IO60NDB2V0		
J4	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0	K17	NC	IO58PDB2V0		
J5	NC	IO112NPB4V0	K18	GND	GND		
J6	NC	IO104PDB4V0	K19	NC	IO68NPB2V0		
J7	NC	IO111PDB4V0	K20	IO41NDB2V0	IO61NDB2V0		
J8	VCCIB4	VCCIB4	K21	GND	GND		
J9	GND	GND	K22	IO42NDB2V0	IO56NDB2V0		
J10	VCC	VCC	L1	IO73NDB4V0	IO108NDB4V0		
J11	GND	GND	L2	VCCOSC	VCCOSC		
J12	VCC	VCC	L3	VCCIB4	VCCIB4		
J13	GND	GND	L4	XTAL2	XTAL2		
J14	VCC	VCC	L5	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0		
J15	VCCIB2	VCCIB2	L6	VCCIB4	VCCIB4		
J16	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0	L7	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0		
J17	NC	IO58NDB2V0	L8	VCCIB4	VCCIB4		
J18	IO38NDB2V0	IO57NDB2V0	L9	GND	GND		
J19	IO39NDB2V0	IO59NDB2V0	L10	VCC	VCC		
J20	GCC2/IO41PDB2V0	GCC2/IO61PDB2V0	L11	GND	GND		
J21	NC	IO55PSB2V0	L12	VCC	VCC		
J22	IO42PDB2V0	IO56PDB2V0	L13	GND	GND		
K1	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0	L14	VCC	VCC		
K2	GND	GND	L15	VCCIB2	VCCIB2		
K3	IO74NDB4V0	IO109NDB4V0	L16	IO48PDB2V0	IO70PDB2V0		

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Package Pin Assignments

	FG676		FG676	FG676			
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	Pin Number	AFS1500 Function		
L17	VCCIB2	N1	NC	P11	VCC		
L18	GCB2/IO60PDB2V0	N2	NC	P12	GND		
L19	IO58NDB2V0	N3	IO108NDB4V0	P13	VCC		
L20	IO57NDB2V0	N4	VCCOSC	P14	GND		
L21	IO59NDB2V0	N5	VCCIB4	P15	VCC		
L22	GCC2/IO61PDB2V0	N6	XTAL2	P16	GND		
L23	IO55PPB2V0	N7	GFC1/IO107PDB4V0	P17	VCCIB2		
L24	IO56PDB2V0	N8	VCCIB4	P18	IO70NDB2V0		
L25	IO55NPB2V0	N9	GFB1/IO106PDB4V0	P19	VCCIB2		
L26	GND	N10	VCCIB4	P20	IO69NDB2V0		
M1	NC	N11	GND	P21	GCA0/IO64NDB2V0		
M2	VCCIB4	N12	VCC	P22	VCCIB2		
M3	GFC2/IO108PDB4V0	N13	GND	P23	GCB0/IO63NDB2V0		
M4	GND	N14	VCC	P24	GCB1/IO63PDB2V0		
M5	IO109NDB4V0	N15	GND	P25	IO66NDB2V0		
M6	IO110NDB4V0	N16	VCC	P26	IO67PDB2V0		
M7	GND	N17	VCCIB2	R1	NC		
M8	IO104NDB4V0	N18	IO70PDB2V0	R2	VCCIB4		
M9	IO111NDB4V0	N19	VCCIB2	R3	IO103NDB4V0		
M10	GND	N20	IO69PDB2V0	R4	GND		
M11	VCC	N21	GCA1/IO64PDB2V0	R5	IO101PDB4V0		
M12	GND	N22	VCCIB2	R6	IO100NPB4V0		
M13	VCC	N23	GCC0/IO62NDB2V0	R7	GND		
M14	GND	N24	GCC1/IO62PDB2V0	R8	IO99PDB4V0		
M15	VCC	N25	IO66PDB2V0	R9	IO97PDB4V0		
M16	GND	N26	IO65NDB2V0	R10	GND		
M17	GND	P1	NC	R11	GND		
M18	IO60NDB2V0	P2	NC	R12	VCC		
M19	IO58PDB2V0	P3	IO103PDB4V0	R13	GND		
M20	GND	P4	XTAL1	R14	VCC		
M21	IO68NPB2V0	P5	VCCIB4	R15	GND		
M22	IO61NDB2V0	P6	GNDOSC	R16	VCC		
M23	GND	P7	GFC0/IO107NDB4V0	R17	GND		
M24	IO56NDB2V0	P8	VCCIB4	R18	GDB2/IO83PDB2V0		
M25	VCCIB2	P9	GFB0/IO106NDB4V0	R19	IO78PDB2V0		
M26	IO65PDB2V0	P10	VCCIB4	R20	GND		

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

Revision	Changes	Page				
Revision 6 (March 2014)	Note added for the discontinuance of QN108 and QN180 packages to the "Package I/Os: Single-/Double-Ended (Analog)" table and the "Temperature Grade Offerings" table (SAR 55113, PDN 1306).	II and IV				
	Updated details about page programming time in the "Program Operation" section (SAR 49291).					
	ADC_START changed to ADCSTART in the "ADC Operation" section (SAR 44104).	2-104				
Revision 5 (January 2014)	Calibrated offset values (AFS090, AFS250) of the external temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 51464).	2-117				
	Specifications for the internal temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 50870).	2-117				
Revision 4 (January 2013)	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43177).	Ш				
	The note in Table 2-12 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42563).					
	Table 2-49 • Analog Channel Specifications was modified to update the uncalibrated offset values (AFS250) of the external and internal temperature monitors (SAR 43134).	2-117				
	In Table 2-57 • Prescaler Control Truth Table—AV ($x = 0$), AC ($x = 1$), and AT ($x = 3$), changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 20812).	2-130				
	The values for the Speed Grade (-1 and Std.) for FDDRIMAX (Table 2-180 • Input DDR Propagation Delays) and values for the Speed Grade (-2 and Std.) for FDDOMAX (Table 2-182 • Output DDR Propagation Delays) had been inadvertently interchanged. This has been rectified (SAR 38514).	2-220, 2-222				
	Added description about what happens if a user connects VAREF to an external 3.3 V on their board to the "VAREF Analog Reference Voltage" section (SAR 35188).	2-225				
	Added a note to Table 3-2 • Recommended Operating Conditions1 (SAR 43429): The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.	3-3				
	Added the Package Thermal details for AFS600-PQ208 and AFS250-PQ208 to Table 3-6 • Package Thermal Resistance (SAR 37816). Deleted the Die Size column from the table (SAR 43503).	3-7				
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 42495).	NA				
Devision 0	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	1 . 15.7				
Revision 3 (August 2012)	Microblade U1AFS250 and U1AFS1500 devices were added to the product tables.	I – IV				
(A sentence pertaining to the analog I/Os was added to the "Specifying I/O States During Programming" section (SAR 34831).	1-9				