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## Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

## Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs250-2fgg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Fusion Device Family Overview

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.



Figure 1-1 • Analog Quad



# **Array Coordinates**

During many place-and-route operations in the Microsemi Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

		Vers	saTiles		Memor	y Rows	All		
Device	Mi	n.	Max.		Bottom	Тор	Min.	Max.	
	x	У	x	У	(x, y)	(x, y)	(x, y)	(x, y)	
AFS090	3	2	98	25	None	(3, 26)	(0, 0)	(101, 29)	
AFS250	3	2	130	49	None	(3, 50)	(0, 0)	(133, 53)	
AFS600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)	
AFS1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 129)	

#### Table 2-3 • Array Coordinates



![](_page_2_Figure_9.jpeg)

![](_page_2_Figure_10.jpeg)

# Flash Memory Block Pin Names

# Table 2-19 • Flash Memory Block Pin Names

Interface Name	Width	Direction	Description
ADDR[17:0]	18	In	Byte offset into the FB. Byte-based address.
AUXBLOCK	1	In	When asserted, the page addressed is used to access the auxiliary block within that page.
BUSY	1	Out	When asserted, indicates that the FB is performing an operation.
CLK	1	In	User interface clock. All operations and status are synchronous to the rising edge of this clock.
DATAWIDTH[1:0]	2	In	Data width 00 = 1 byte in RD/WD[7:0] 01 = 2 bytes in RD/WD[15:0] 1x = 4 bytes in RD/WD[31:0]
DISCARDPAGE	1	In	When asserted, the contents of the Page Buffer are discarded so that a new page write can be started.
ERASEPAGE	1	In	When asserted, the address page is to be programmed with all zeros. ERASEPAGE must transition synchronously with the rising edge of CLK.
LOCKREQUEST	1	In	When asserted, indicates to the JTAG controller that the FPGA interface is accessing the FB.
OVERWRITEPAGE	1	In	When asserted, the page addressed is overwritten with the contents of the Page Buffer if the page is writable.
OVERWRITEPROTECT	1	In	When asserted, all program operations will set the overwrite protect bit of the page being programmed.
PAGESTATUS	1	In	When asserted with REN, initiates a read page status operation.
PAGELOSSPROTECT	1	In	When asserted, a modified Page Buffer must be programmed or discarded before accessing a new page.
PIPE	1	In	Adds a pipeline stage to the output for operation above 50 MHz.
PROGRAM	1	In	When asserted, writes the contents of the Page Buffer into the FB page addressed.
RD[31:0]	32	Out	Read data; data will be valid from the first non-busy cycle (BUSY = 0) after REN has been asserted.
READNEXT	1	In	When asserted with REN, initiates a read-next operation.
REN	1	In	When asserted, initiates a read operation.
RESET	1	In	When asserted, resets the state of the FB (active low).
SPAREPAGE	1	In	When asserted, the sector addressed is used to access the spare page within that sector.

![](_page_4_Picture_0.jpeg)

The following error indications are possible for Read operations:

- 1. STATUS = '01' when a single-bit data error was detected and corrected within the block addressed.
- 2. STATUS = '10' when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in Table 2-23, and the definition of the page status bits is shown in Table 2-24.

Table 2-23 • Page Status Read Data Format

31	8	7	4	3	2	1	0
Write (	Count	Rese	erved	Over Threshold	Read Protected	Write Protected	Overwrite Protected

## Table 2-24 • Page Status Bit Definition

Page Status Bit(s)	Definition
31–8	The number of times the page addressed has been programmed/erased
7–4	Reserved; read as 0
3	Over Threshold indicator (see the "Program Operation" section on page 2-46)
2	Read Protected; read protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
1	Write Protected; write protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
0	Overwrite Protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a Program operation. The page cannot be written without first performing an Unprotect Page operation.

![](_page_5_Picture_0.jpeg)

## **Unprotect Page Operation**

An Unprotect Page operation will clear the protection for a page addressed on the ADDR input. It is initiated by setting the UNPROTECTPAGE signal on the interface along with the page address on ADDR.

If the page is not in the Page Buffer, the Unprotect Page operation will copy the page into the Page Buffer. The Copy Page operation occurs only if the current page in the Page Buffer is not Page Loss Protected.

The waveform for an Unprotect Page operation is shown in Figure 2-42.

![](_page_5_Figure_5.jpeg)

## Figure 2-42 • FB Unprotected Page Waveform

The Unprotect Page operation can incur the following error conditions:

- 1. If the copy of the page to the Page Buffer determines that the page has a single-bit correctable error in the data, it will report a STATUS = '01'.
- 2. If the address on ADDR does not match the address of the Page Buffer, PAGELOSSPROTECT is asserted, and the Page Buffer has been modified, then STATUS = '11' and the addressed page is not loaded into the Page Buffer.
- 3. If the copy of the page to the Page Buffer determines that at least one block in the page has a double-bit uncorrectable error, STATUS = '10' and the Page Buffer will contain the corrupted data.

## **Discard Page Operation**

If the contents of the modified Page Buffer have to be discarded, the DISCARDPAGE signal should be asserted. This command results in the Page Buffer being marked as unmodified.

The timing for the operation is shown in Figure 2-43. The BUSY signal will remain asserted until the operation has completed.

![](_page_5_Figure_14.jpeg)

Figure 2-43 • FB Discard Page Waveform

![](_page_6_Picture_0.jpeg)

## *Table 2-32* • RAM512X18

# Commercial Temperature Range Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t <sub>AS</sub>	Address setup time	0.25	0.28	0.33	ns
t <sub>AH</sub>	Address hold time	0.00	0.00	0.00	ns
t <sub>ENS</sub>	REN, WEN setup time	0.09	0.10	0.12	ns
t <sub>ENH</sub>	REN, WEN hold time	0.06	0.07	0.08	ns
t <sub>DS</sub>	Input data (WD) setup time	0.18	0.21	0.25	ns
t <sub>DH</sub>	Input data (WD) hold time	0.00	0.00	0.00	ns
t <sub>CKQ1</sub>	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t <sub>CKQ2</sub>	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t <sub>C2CRWH</sub> 1	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t <sub>C2CWRH</sub> 1	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.59	0.50	0.44	ns
t 1	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
<b>'</b> RSTBQ	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
t <sub>REMRSTB</sub>	RESET removal	0.29	0.33	0.38	ns
t <sub>RECRSTB</sub>	RESET recovery	1.50	1.71	2.01	ns
t <sub>MPWRSTB</sub>	RESET minimum pulse width	0.21	0.24	0.29	ns
t <sub>CYC</sub>	Clock cycle time	3.23	3.68	4.32	ns
F <sub>MAX</sub>	Maximum frequency	310	272	231	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.

2. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

![](_page_7_Picture_0.jpeg)

# Table 2-36 • Analog Block Pin Description (continued)

Signal Name	Number of Bits	Direction	ection Function			
GDON0 to GDON9	10	Input	Control to power MOS – 1 per quad	Analog Quad		
TMSTB0 to TMSTB9	10	Input	Temperature monitor strobe – 1 per quad; active high	Analog Quad		
DAVOUTO, DACOUTO, DATOUTO	30	Output	Digital outputs – 3 per quad	Analog Quad		
to DAVOUT9, DACOUT9, DATOUT9						
DENAV0, DENAC0, DENAT0 to DENAV9, DENAC9, DENAT9	30	Input	Digital input enables – 3 per quad	Analog Quad		
AV0	1	Input	Analog Quad 0	Analog Quad		
AC0	1	Input		Analog Quad		
AG0	1	Output		Analog Quad		
AT0	1	Input		Analog Quad		
ATRETURN01	1	Input	Temperature monitor return shared by Analog Quads 0 and 1	Analog Quad		
AV1	1	Input	Analog Quad 1	Analog Quad		
AC1	1	Input		Analog Quad		
AG1	1	Output		Analog Quad		
AT1	1	Input		Analog Quad		
AV2	1	Input	Analog Quad 2	Analog Quad		
AC2	1	Input		Analog Quad		
AG2	1	Output		Analog Quad		
AT2	1	Input		Analog Quad		
ATRETURN23	1	Input	Temperature monitor return shared by Analog Quads 2 and 3	Analog Quad		
AV3	1	Input	Analog Quad 3	Analog Quad		
AC3	1	Input		Analog Quad		
AG3	1	Output		Analog Quad		
AT3	1	Input		Analog Quad		
AV4	1	Input	Analog Quad 4	Analog Quad		
AC4	1	Input		Analog Quad		
AG4	1	Output		Analog Quad		
AT4	1	Input		Analog Quad		
ATRETURN45	1	Input	Temperature monitor return shared by Analog Quads 4 and 5	Analog Quad		
AV5	1	Input	Analog Quad 5	Analog Quad		
AC5	1	Input		Analog Quad		
AG5	1	Output		Analog Quad		
AT5	1	Input		Analog Quad		
AV6	1	Input	Analog Quad 6	Analog Quad		
AC6	1	Input		Analog Quad		

The diode's voltage is measured at each current level and the temperature is calculated based on EQ 7.

$$V_{\text{TMSLO}} - V_{\text{TMSHI}} = n \frac{kT}{q} \left( \ln \frac{I_{\text{TMSLO}}}{I_{\text{TMSHI}}} \right)$$

EQ 7

where

 $\textit{I}_{\textit{TMSLO}}$  is the current when the Temperature Strobe is Low, typically 100  $\mu A$ 

 $I_{TMSHI}$  is the current when the Temperature Strobe is High, typically 10  $\mu A$ 

*V<sub>TMSLO</sub>* is diode voltage while Temperature Strobe is Low

 $V_{TMSHI}$  is diode voltage while Temperature Strobe is High

n is the non-ideality factor of the diode-connected transistor. It is typically 1.004 for the Microsemirecommended transistor type 2N3904.

- $K = 1.3806 \text{ x } 10^{-23} \text{ J/K}$  is the Boltzman constant
- $Q = 1.602 \times 10^{-19} C$  is the charge of a proton

When  $I_{TMSLO} / I_{TMSHI} = 10$ , the equation can be simplified as shown in EQ 8.

$$\Delta V = V_{\text{TMSLO}} - V_{\text{TMSHI}} = 1.986 \times 10^{-4} nT$$

EQ 8

In the Fusion TMB, the ideality factor *n* for 2N3904 is 1.004 and  $\Delta V$  is amplified 12.5 times by an internal amplifier; hence the voltage before entering the ADC is as given in EQ 9.

$$V_{ADC} = \Delta V \times 12.5 = 2.5 \text{ mV}/(K \times T)$$

EQ 9

This means the temperature to voltage relationship is 2.5 mV per degree Kelvin. The unique design of Fusion has made the Temperature Monitor System simple for the user. When the 10-bit mode ADC is used, each LSB represents 1 degree Kelvin, as shown in EQ 10. That is, e. 25°C is equal to 293°K and is represented by decimal 293 counts from the ADC.

$$1K = 2.5 \text{ mV} \times \frac{2^{10}}{2.56 \text{ V}} = 1 \text{ LSB}$$

EQ 10

If 8-bit mode is used for the ADC resolution, each LSB represents 4 degrees Kelvin; however, the resolution remains as 1 degree Kelvin per LSB, even for 12-bit mode, due to the Temperature Monitor design. An example of the temperature data format for 10-bit mode is shown in Table 2-38.

Temperature	Temperature (K)	Digital Output (ADC 10-bit mode)
-40°C	233	00 1110 1001
–20°C	253	00 1111 1101
0°C	273	01 0001 0001
1°C	274	01 0001 0010
10 °C	283	01 0001 1011
25°C	298	01 0010 1010
50 °C	323	01 0100 0011
85 °C	358	01 0110 0110

Table 2-38 • Temperature Data Format

![](_page_9_Picture_0.jpeg)

# Terminology

# Resolution

Resolution defines the smallest temperature change Fusion Temperature Monitor can resolve. For ADC configured as 8-bit mode, each LSB represents 4°C, and 1°C per LSB for 10-bit mode. With 12-bit mode, the Temperature Monitor can still only resolve 1°C due to Temperature Monitor design.

## Offset

The Fusion Temperature Monitor has a systematic offset (Table 2-49 on page 2-117), excluding error due to board resistance and ideality factor of the external diode. Microsemi provides an IP block (CalibIP) that is required in order to mitigate the systematic temperature offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.

![](_page_10_Picture_0.jpeg)

# Table 2-71 • Fusion Standard and Advanced I/O Features

I/O Bank Voltage (typical)	Minibank Voltage (typical)	LVTTL/LVCMOS 3.3 V	LVCMOS 2.5 V	LVCMOS 1.8 V	LVCMOS 1.5 V	3.3 V PCI / PCI-X	GTL + (3.3 V)	GTL + (2.5 V)	GTL (3.3 V)	GTL (2.5 V)	HSTL Class I and II (1.5 V)	SSTL2 Class I and II (2.5 V)	SSTL3 Class I and II (3.3 V)	LVDS (2.5 V ± 5%)	LVPECL (3.3 V)
3.3 V	-														
	0.80 V														
	1.00 V														
	1.50 V														
2.5 V	-														
	0.80 V														
	1.00 V														
	1.25 V														
1.8 V	-														
1.5 V	-														
	0.75 V														

Note: White box: Allowable I/O standard combinations Gray box: Illegal I/O standard combinations

![](_page_11_Picture_0.jpeg)

# **Hot-Swap Support**

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-74. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

Table 2-74 • Levels of Hot-Swap Support

Hot Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain Fusion Devices	Compliance of Fusion Devices
1	Cold-swap	No	-	_	_	System and card with Microsemi FPGA chip are powered down, then card gets plugged into system, then power supplies are turned on for system but not for FPGA on card.	Compliant I/Os can but do not have to be set to hot insertion mode.
2	Hot-swap while reset	Yes	Held in reset state	Must be made and maintained for 1 ms before, during, and after insertion/ removal	_	In PCI hot plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant I/Os can but do not have to be set to hot insertion mode.
3	Hot-swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/re moval)	Same as Level 2	Mustremain glitch-free during power-up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on bus. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.
4	Hot-swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle.	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.

![](_page_12_Picture_0.jpeg)

![](_page_12_Figure_1.jpeg)

*Figure 2-118* • Tristate Output Buffer Timing Model and Delays (example)

# 2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-147 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
33 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	_	33	33	124	169	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

![](_page_13_Figure_10.jpeg)

## Figure 2-127 • AC Loading

## Table 2-148 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

#### Timing Characteristics

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Table 2-149 • 2.5 V GTL+
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# Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
Std.	0.66	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
-1	0.56	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
-2	0.49	1.65	0.03	1.13	0.32	1.68	1.57			3.35	4.34	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

#### ATRTNx Temperature Monitor Return

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The x in the ATRTNx designator indicates the quad pairing (x = 0 for AQ1 and AQ2, x = 1 for AQ2 and AQ3, ..., x = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURNxy in the software (where x and y refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

#### GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-22.

Refer to the "User I/O Naming Convention" section on page 2-158 for a description of naming of global pins.

# JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

#### TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pullup/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500  $\Omega$  to 1 k $\Omega$  will satisfy the requirements. Refer to Table 2-183 for more information.

VJTAG	Tie-Off Resistance <sup>2, 3</sup>
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Table 2-183 • Recommended Tie-Off Values for the TCK and TRST Pins

Notes:

- 1. Equivalent parallel resistance if more than one device is on JTAG chain.
- 2. The TCK pin can be pulled up/down.
- 3. The TRST pin can only be pulled down.

#### TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

#### TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

# Theta-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

Maximum Power Allowed = 
$$\frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

 $\theta_{JA}$  = 19.00°C/W (taken from Table 3-6 on page 3-7).

 $T_A = 75.00^{\circ}C$ 

Maximum Power Allowed = 
$$\frac{100.00^{\circ}C - 75.00^{\circ}C}{19.00^{\circ}C/W} = 1.3 W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

# Theta-JB

Junction-to-board thermal resistance ( $\theta_{JB}$ ) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

# Theta-JC

Junction-to-case thermal resistance ( $\theta_{JC}$ ) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

# Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent  $T_a$  and  $T_j$  are given as follows:

 $T_{J} = 100.00^{\circ}C$ 

 $T_A = 70.00^{\circ}C$ 

From the datasheet:

 $\theta_{JA} = 17.00^{\circ}C/W$  $\theta_{JC} = 8.28^{\circ}C/W$ 

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^{\circ}C - 70^{\circ}C}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6

![](_page_16_Picture_0.jpeg)

# Table 3-12 • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings (continued)

	VCCI (V)	Static Power PDC7 (mW) <sup>1</sup>	Dynamic Power PAC9 (µW/MHz) <sup>2</sup>
Applicable to Advanced I/O Banks			
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	_	16.69
2.5 V LVCMOS	2.5	_	5.12
1.8 V LVCMOS	1.8	_	2.13
1.5 V LVCMOS (JESD8-11)	1.5	_	1.45
3.3 V PCI	3.3	_	18.11
3.3 V PCI-X	3.3	_	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87
Applicable to Standard I/O Banks			
3.3 V LVTTL/LVCMOS	3.3	-	16.79
2.5 V LVCMOS	2.5	_	5.19
1.8 V LVCMOS	1.8	_	2.18
1.5 V LVCMOS (JESD8-11)	1.5	_	1.52

Notes:

1. PDC7 is the static power (where applicable) measured on VCCI.

2. PAC9 is the total dynamic power measured on VCC and VCCI.

![](_page_17_Picture_0.jpeg)

 $P_{S-CELL} = 0 W$  $P_{C-CELL} = 0 W$  $P_{NET} = 0 W$  $P_{LOGIC} = 0 W$ 

# I/O Input and Output Buffer Contribution—P<sub>I/O</sub>

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

 $F_{CLK} = 50 \text{ MHz}$ Number of input pins used: N<sub>INPUTS</sub> = 30 Number of output pins used: N<sub>OUTPUTS</sub> = 40 Estimated I/O buffer toggle rate:  $\alpha_2$  = 0.1 (10%) Estimated IO buffer enable rate:  $\beta_1$  = 1 (100%)

## **Operating Mode**

$$\begin{split} \mathsf{P}_{\mathsf{INPUTS}} &= \mathsf{N}_{\mathsf{INPUTS}} * (\alpha_2 \,/\, 2) * \mathsf{PAC9} * \mathsf{F}_{\mathsf{CLK}} \\ \mathsf{P}_{\mathsf{INPUTS}} &= 30 * (0.1 \,/\, 2) * 0.01739 * 50 \\ \mathsf{P}_{\mathsf{INPUTS}} &= 1.30 \text{ mW} \end{split}$$

$$\begin{split} \mathsf{P}_{\text{OUTPUTS}} &= \mathsf{N}_{\text{OUTPUTS}} * (\alpha_2 / 2) * \beta_1 * \mathsf{PAC10} * \mathsf{F}_{\text{CLK}} \\ \mathsf{P}_{\text{OUTPUTS}} &= 40 * (0.1 / 2) * 1 * 0.4747 * 50 \\ \mathsf{P}_{\text{OUTPUTS}} &= 47.47 \text{ mW} \end{split}$$

 $P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$  $P_{I/O} = 1.30 \text{ mW} + 47.47 \text{ mW}$ 

P<sub>I/O</sub> = 48.77 mW

## Standby Mode and Sleep Mode

 $P_{INPUTS} = 0 W$ 

 $P_{OUTPUTS} = 0 W$  $P_{I/O} = 0 W$ 

# RAM Contribution—P<sub>MEMORY</sub>

Frequency of Read Clock:  $F_{READ-CLOCK} = 10 \text{ MHz}$ Frequency of Write Clock:  $F_{WRITE-CLOCK} = 10 \text{ MHz}$ Number of RAM blocks:  $N_{BLOCKS} = 20$ Estimated RAM Read Enable Rate:  $\beta_2 = 0.125 (12.5\%)$ Estimated RAM Write Enable Rate:  $\beta_3 = 0.125 (12.5\%)$ 

## **Operating Mode**

$$\begin{split} \mathsf{P}_{\mathsf{MEMORY}} &= (\mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{PAC11} * \beta_2 * \mathsf{F}_{\mathsf{READ-CLOCK}}) + (\mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{PAC12} * \beta_3 * \mathsf{F}_{\mathsf{WRITE-CLOCK}}) \\ \mathsf{P}_{\mathsf{MEMORY}} &= (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10) \\ \mathsf{P}_{\mathsf{MEMORY}} &= 1.38 \text{ mW} \end{split}$$

# Standby Mode and Sleep Mode

P<sub>MEMORY</sub> = 0 W

![](_page_18_Picture_0.jpeg)

Package Pin Assignments

	FG484		FG484				
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function		
L17	VCCIB2	VCCIB2	N8	GND	GND		
L18	IO46PDB2V0	IO69PDB2V0	N9	GND	GND		
L19	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0	N10	VCC	VCC		
L20	VCCIB2	VCCIB2	N11	GND	GND		
L21	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0	N12	VCC	VCC		
L22	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0	N13	GND	GND		
M1	NC	IO103PDB4V0	N14	VCC	VCC		
M2	XTAL1	XTAL1	N15	GND	GND		
M3	VCCIB4	VCCIB4	N16	GDB2/IO56PDB2V0	GDB2/IO83PDB2V0		
M4	GNDOSC	GNDOSC	N17	NC	IO78PDB2V0		
M5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0	N18	GND	GND		
M6	VCCIB4	VCCIB4	N19	IO47NDB2V0	IO72NDB2V0		
M7	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0	N20	IO47PDB2V0	IO72PDB2V0		
M8	VCCIB4	VCCIB4	N21	GND	GND		
M9	VCC	VCC	N22	IO49PDB2V0	IO71PDB2V0		
M10	GND	GND	P1	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0		
M11	VCC	VCC	P2	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0		
M12	GND	GND	P3	IO68NDB4V0	IO101NDB4V0		
M13	VCC	VCC	P4	IO65PDB4V0	IO96PDB4V0		
M14	GND	GND	P5	IO65NDB4V0	IO96NDB4V0		
M15	VCCIB2	VCCIB2	P6	NC	IO99NDB4V0		
M16	IO48NDB2V0	IO70NDB2V0	P7	NC	IO97NDB4V0		
M17	VCCIB2	VCCIB2	P8	VCCIB4	VCCIB4		
M18	IO46NDB2V0	IO69NDB2V0	P9	VCC	VCC		
M19	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0	P10	GND	GND		
M20	VCCIB2	VCCIB2	P11	VCC	VCC		
M21	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0	P12	GND	GND		
M22	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0	P13	VCC	VCC		
N1	NC	IO103NDB4V0	P14	GND	GND		
N2	GND	GND	P15	VCCIB2	VCCIB2		
N3	IO68PDB4V0	IO101PDB4V0	P16	IO56NDB2V0	IO83NDB2V0		
N4	NC	IO100NPB4V0	P17	NC	IO78NDB2V0		
N5	GND	GND	P18	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0		
N6	NC	IO99PDB4V0	P19	GDB1/IO53PDB2V0	GDB1/IO80PDB2V0		
N7	NC	IO97PDB4V0	P20	IO51NDB2V0	IO73NDB2V0		

![](_page_19_Picture_0.jpeg)

Datasheet Information

Revision	Changes			
v2.0, Revision 1 (July 2009)	The MicroBlade and Fusion datasheets have been combined. Pigeon Point information is new.			
	CoreMP7 support was removed since it is no longer offered.			
	-F was removed from the datasheet since it is no longer offered.			
	The operating temperature was changed from ambient to junction to better reflect actual conditions of operations.			
	Commercial: 0°C to 85°C			
	Industrial: –40°C to 100°C			
	The version number category was changed from Preliminary to Production, which means the datasheet contains information based on final characterization. The version number changed from Preliminary v1.7 to v2.0.			
	The "Integrated Analog Blocks and Analog I/Os" section was updated to include a reference to the "Analog System Characteristics" section in the <i>Device Architecture</i> chapter of the datasheet, which includes Table 2-46 • Analog Channel Specifications and specific voltage data.	1-4		
	The phrase "Commercial-Case Conditions" in timing table titles was changed to "Commercial Temperature Range Conditions."	N/A		
	The "Crystal Oscillator" section was updated significantly. Please review carefully.	2-20		
	The "Real-Time Counter (part of AB macro)" section was updated significantly. Please review carefully.	2-33		
	There was a typo in Table 2-19 • Flash Memory Block Pin Names for the ERASEPAGE description; it was the same as DISCARDPAGE. As as a result, the ERASEPAGE description was updated.	2-40		
	The $t_{\mbox{FMAXCLKNVM}}$ parameter was updated in Table 2-25 $\bullet$ Flash Memory Block Timing.	2-52		
	Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated.	2-66		
	In Table 2-36 • Analog Block Pin Description, the Function description for PWRDWN was changed from "Comparator power-down if 1"	2-78		
	to "ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin."			
	Figure 2-75 • Gate Driver Example was updated.	2-91		
	The "ADC Operation" section was updated. Please review carefully.	2-104		
	Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram are new.	2-113		
	The "Typical Performance Characteristics" section is new.	2-115		
	Table 2-49 • Analog Channel Specifications was significantly updated.	2-117		
	Table 2-50 • ADC Characteristics in Direct Input Mode was significantly updated.	2-120		
	In Table 2-52 • Calibrated Analog Channel Accuracy 1,2,3, note 2 was updated.	2-123		
	In Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages, note 1 was updated.	2-124		
	In Table 2-54 • ACM Address Decode Table for Analog Quad, bit 89 was removed.	2-126		

![](_page_20_Picture_0.jpeg)

Datasheet Information

Revision	Changes	Page
Advance v1.0 (continued)	This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to $V_{CC33A}$ .	3-8
Advance v0.9 (October 2007)	In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126	II
	In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pin: B25	3-2
	In the "180-Pin QFN" table, the function changed from V <sub>CC33ACAP</sub> to V <sub>CC33A</sub> for the following pins: AFS090: B29 AFS250: B29	3-4
	In the "208-Pin PQFP" table, the function changed from V <sub>CC33ACAP</sub> to V <sub>CC33A</sub> for the following pins: AFS090: 102 AFS250: 102	3-8
	In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14	3-12
Advance v0.9 (continued)	In the "484-Pin FBGA" table, the function changed from V <sub>CC33ACAP</sub> to V <sub>CC33A</sub> for the following pins: AFS600: AB18 AFS1500: AB18	3-20
	In the "676-Pin FBGA" table, the function changed from V <sub>CC33ACAP</sub> to V <sub>CC33A</sub> for the following pins: AFS1500: AD20	3-28
Advance v0.8 (June 2007)	Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC.	2-20, 2-21
	Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added.	2-25
	The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator.	2-22
	Table 2-11 $\cdot$ Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of I <sub>DYNXTAL</sub> for 0.032–0.2 MHz to 0.19.	2-24
	The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR.	2-41
	The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR.	2-41