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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs250-fgg256

Email: info@E-XFL.COM

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Global Resources (VersaNets)

Fusion devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has six CCCs. The west CCC also contains a PLL core. In the two larger devices (AFS600 and AFS1500), the west and the east CCCs each contain a PLL. The PLLs include delay lines, a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six lines total). The CCCs at the four corners each have access to three quadrant global lines on each quadrant of the chip.

Advantages of the VersaNet Approach

One of the architectural benefits of Fusion is the set of powerful and low-delay VersaNet global networks. Fusion offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-11). In addition, Fusion devices have three regional globals (quadrant globals) in each of the four chip quadrants. Each core VersaTile has access to nine global networks on the device. Each of these networks contains spines and ribs that reach all VersaTiles in all quadrants (Figure 2-12 on page 2-12). This flexible VersaNet global network architecture allows users to map up to 180 different internal/external clocks in a Fusion device. Details on the VersaNet networks are given in Table 2-4 on page 2-12. The flexibility of the Fusion VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.



Figure 2-11 • Overview of Fusion VersaNet Global Network



Figure 2-	-12 •	Global	Network	Architecture
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Table 2-4 • Globals/Spines/Rows by Device

	AFS090	AFS250	AFS600	AFS1500
Global VersaNets (trees)*	9	9	9	9
VersaNet Spines/Tree	4	8	12	20
Total Spines	36	72	108	180
VersaTiles in Each Top or Bottom Spine	384	768	1,152	1,920
Total VersaTiles	2,304	6,144	13,824	38,400

Note: *There are six chip (main) globals and three globals per quadrant.



Embedded Memories

Fusion devices include four types of embedded memory: flash block, FlashROM, SRAM, and FIFO.

Flash Memory Block

Fusion is the first FPGA that offers a flash memory block (FB). Each FB block stores 2 Mbits of data. The flash memory block macro is illustrated in Figure 2-32. The port pin name and descriptions are detailed on Table 2-19 on page 2-40. All flash memory block signals are active high, except for CLK and active low RESET. All flash memory operations are synchronous to the rising edge of CLK.



Figure 2-32 • Flash Memory Block



RAM4K9 Description



Figure 2-48 • RAM4K9

Channel Input Offset Error

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to $\frac{1}{2}$ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

Total Channel Error

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.



Figure 2-68 • Total Channel Error Example



Device Architecture

Integrated Voltage Reference

The Fusion device has an integrated on-chip 2.56 V reference voltage for the ADC. The value of this reference voltage was chosen to make the prescaling and postscaling factors for the prescaler blocks change in a binary fashion. However, if desired, an external reference voltage of up to 3.3 V can be connected between the VAREF and ADCGNDREF pins. The VAREFSEL control pin is used to select the reference voltage.

Table 2-42 • VAREF Bit Function

Name	Bit	Function
VAREF	0	Reference voltage selection
		0 – Internal voltage reference selected. VAREF pin outputs 2.56 V.
		1 – Input external voltage reference from VAREF and ADCGNDREF

ADC Clock

The speed of the ADC depends on its internal clock, ADCCLK, which is not accessible to users. The ADCCLK is derived from SYSCLK. Input signal TVC[7:0], Time Divider Control, determines the speed of the ADCCLK in relationship to SYSCLK, based on EQ 15.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK}$$

EQ 15

TVC: Time Divider Control (0-255)

 t_{ADCCLK} is the period of ADCCLK, and must be between 0.5 MHz and 10 MHz t_{SYSCLK} is the period of SYSCLK

Table 2-43 • TVC Bits Function

Name	Bits	Function		
TVC	[7:0]	SYSCLK divider control		

The frequency of ADCCLK, f_{ADCCLK}, must be within 0.5 Hz to 10 MHz.

The inputs to the ADC are synchronized to SYSCLK. A conversion is initiated by asserting the ADCSTART signal on a rising edge of SYSCLK. Figure 2-90 on page 2-112 and Figure 2-91 on page 2-112 show the timing diagram for the ADC.

Acquisition Time or Sample Time Control

Acquisition time (t_{SAMPLE}) specifies how long an analog input signal has to charge the internal capacitor array. Figure 2-88 shows a simplified internal input sampling mechanism of a SAR ADC.



Figure 2-88 • Simplified Sample and Hold Circuitry

The internal impedance (Z_{INAD}), external source resistance (R_{SOURCE}), and sample capacitor (C_{INAD}) form a simple RC network. As a result, the accuracy of the ADC can be affected if the ADC is given insufficient time to charge the capacitor. To resolve this problem, you can either reduce the source resistance or increase the sampling time by changing the acquisition time using the STC signal.



Device Architecture

Table 2-49 • Analog Channel Specifications (continued)

Commercial Temperature Range Conditions, $T_J = 85^{\circ}C$ (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Digital Input usi	ing Analog Pads AV, AC	and AT		1 1		
VIND ^{2,3}	Input Voltage	Refer to Table 3-2 on page 3-3				
VHYSDIN	Hysteresis			0.3		V
VIHDIN	Input High			1.2		V
VILDIN	Input Low			0.9		V
VMPWDIN	Minimum Pulse With		50			ns
F _{DIN}	Maximum Frequency				10	MHz
ISTBDIN	Input Leakage Current			2		μA
IDYNDIN	Dynamic Current			20		μA
t _{INDIN}	Input Delay			10		ns
Gate Driver Out	put Using Analog Pad A	G	•			
VG	Voltage Range	Refer to Table 3-2 on page 3-3				
IG	Output Current Drive	High Current Mode ⁶ at 1.0 V			±20	mA
		Low Current Mode: ±1 µA	0.8	1.0	1.3	μA
		Low Current Mode: ±3 µA	2.0	2.7	3.3	μA
		Low Current Mode: ± 10 µA	7.4	9.0	11.5	μA
		Low Current Mode: ± 30 µA	21.0	27.0	32.0	μA
IOFFG	Maximum Off Current				100	nA
F _G	Maximum switching rate	High Current Mode ⁶ at 1.0 V, 1 k Ω resistive load		1.3		MHz
		Low Current Mode: ±1 μA, 3 MΩ resistive load		3		KHz
		Low Current Mode: ±3 μA, 1 MΩ resistive load		7		KHz
		Low Current Mode: $\pm 10 \ \mu$ A, 300 k Ω resistive load		25		KHz
		Low Current Mode: $\pm 30 \ \mu$ A, 105 k Ω resistive load		78		KHz

Notes:

1. VRSM is the maximum voltage drop across the current sense resistor.

2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.

3. VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.

4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.

- 5. The temperature offset is a fixed positive value.
- 6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
- 7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.



Device Architecture

Similarly,

Min. Output Voltage = (Max. Negative input offset) + (Input Voltage x Max. Negative Channel Gain) = $(-88 \text{ mV}) + (5 \text{ V} \times 0.96) = 4.712 \text{ V}$

Calculating Accuracy for a Calibrated Analog Channel

Formula

For a given prescaler range, EQ 31 gives the output voltage.

Output Voltage = Channel Error in V + Input Voltage

EQ 31

where

Channel Error in V = Total Channel Error in LSBs x Equivalent voltage per LSB

Example

Input Voltage = 5 VChosen Prescaler range = 8 V range Refer to Table 2-52 on page 2-123.

Max. Output Voltage = Max. Positive Channel Error in V + Input Voltage Max. Positive Channel Error in V = (6 LSB) × (8 mV per LSB in 10-bit mode) = 48 mV Max. Output Voltage = 48 mV + 5 V = **5.048 V**

Similarly,

Min. Output Voltage = Max. Negative Channel Error in V + Input Voltage = (-48 mV) + 5 V = 4.952 V

Calculating LSBs from a Given Error Budget

Formula

For a given prescaler range, LSB count = ± (Input Voltage × Required % error) / (Equivalent voltage per LSB)

Example

Input Voltage = $3.3 \vee$ Required error margin= 1% Refer to Table 2-52 on page 2-123. Equivalent voltage per LSB = 16 mV for a 16V prescaler, with ADC in 10-bit mode LSB Count = $\pm (5.0 \vee \times 1\%) / (0.016)$ LSB Count = ± 3.125 Equivalent voltage per LSB = 8 mV for an $8 \vee$ prescaler, with ADC in 10-bit mode LSB Count = $\pm (5.0 \vee \times 1\%) / (0.008)$ LSB Count = $\pm (5.0 \vee \times 1\%) / (0.008)$ LSB Count = ± 6.25 The $8 \vee$ prescaler satisfies the calculated LSB count accuracy requirement (see Table 2-52 on page 2-123).

Table 2-82 • Advanced I/O Default Attributes

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	Refer to the following	Refer to the following tables	Off	None	35 pF	-
LVCMOS 2.5 V	information:	Table 2-78 on page 2-152	Off	None	35 pF	-
LVCMOS 2.5/5.0 V	Table 2-78 on page 2-152	Table 2-79 on page 2-152	Off	None	35 pF	-
LVCMOS 1.8 V	Table 2-79 on page 2-152	Table 2-80 on page 2-152	Off	None	35 pF	-
LVCMOS 1.5 V	Table 2-80 on page 2-152		Off	None	35 pF	-
PCI (3.3 V)			Off	None	10 pF	-
PCI-X (3.3 V)			Off	None	10 pF	-
LVDS, BLVDS, M-LVDS			Off	None	_	_
LVPECL			Off	None	-	-

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-90 • Summary of AC Measuring Points Applicable to All I/O Bank Types

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	_	-	1.4 V
2.5 V LVCMOS	_	-	1.2 V
1.8 V LVCMOS	-	-	0.90 V
1.5 V LVCMOS	-	-	0.75 V
3.3 V PCI	_	_	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	-	_	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	-	-	Cross point
LVPECL	-	-	Cross point

Table 2-91 • I/O AC Parameter Definitions

Parameter	Definition
t _{DP}	Data to Pad delay through the Output Buffer
t _{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t _{DOUT}	Data to Output Buffer delay through the I/O interface
t _{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t _{DIN}	Input Buffer to Data delay through the I/O interface
t _{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t _{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t _{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t _{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t _{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t _{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t _{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

HSTL Class II		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
15 mA ³	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15	55	66	10	10

Note:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Output drive strength is below JEDEC specification.



Figure 2-129 • AC Loading

Table 2-154 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-155 • HSTL Class II

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Commercial Temperature Range Conditions: T_J = 70^{\circ}C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V
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Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
-1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
-2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Pin Descriptions

Supply Pins

GND Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF Analog Reference Ground

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA Ground (analog)

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ Ground (analog quiet)

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM Flash Memory Ground

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC Oscillator Ground

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A Analog Power Supply (1.5 V)

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A Analog Power Supply (3.3 V)

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N Negative 3.3 V Output

This is the -3.3 V output from the voltage converter. A 2.2 μ F capacitor must be connected from this pin to ground.

VCC33PMP Analog Power Supply (3.3 V)

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM Flash Memory Block Power Supply (1.5 V)

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC Oscillator Power Supply (3.3 V)

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33 pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

ATRTNx Temperature Monitor Return

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The x in the ATRTNx designator indicates the quad pairing (x = 0 for AQ1 and AQ2, x = 1 for AQ2 and AQ3, ..., x = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURNxy in the software (where x and y refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-22.

Refer to the "User I/O Naming Convention" section on page 2-158 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pullup/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to Table 2-183 for more information.

VJTAG	Tie-Off Resistance ^{2, 3}
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Table 2-183 • Recommended Tie-Off Values for the TCK and TRST Pins

Notes:

- 1. Equivalent parallel resistance if more than one device is on JTAG chain.
- 2. The TCK pin can be pulled up/down.
- 3. The TRST pin can only be pulled down.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.





connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Figure 2-146 • Boundary Scan Chain in Fusion

Table 2-185 • Boundary Scan Opcodes

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF



Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{\mathsf{J}\mathsf{A}} = \frac{\mathsf{T}_{\mathsf{J}} - \theta_{\mathsf{A}}}{\mathsf{P}}$$

EQ 1

$$\theta_{\mathsf{JB}} = \frac{\mathsf{T}_{\mathsf{J}} - \mathsf{T}_{\mathsf{B}}}{\mathsf{P}}$$

EQ 2

EQ 3

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

where

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JB} = Junction-to-board thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 3-6 • Package Thermal Resistance

	Θ_{JA}					
Product	Still Air	1.0 m/s	2.5 m/s	θ JC	θ_{JB}	Units
AFS090-QN108	34.5	30.0	27.7	8.1	16.7	°C/W
AFS090-QN180	33.3	27.6	25.7	9.2	21.2	°C/W
AFS250-QN180	32.2	26.5	24.7	5.7	15.0	°C/W
AFS250-PQ208	42.1	38.4	37	20.5	36.3	°C/W
AFS600-PQ208	23.9	21.3	20.48	6.1	16.5	°C/W
AFS090-FG256	37.7	33.9	32.2	11.5	29.7	°C/W
AFS250-FG256	33.7	30.0	28.3	9.3	24.8	°C/W
AFS600-FG256	28.9	25.2	23.5	6.8	19.9	°C/W
AFS1500-FG256	23.3	19.6	18.0	4.3	14.2	°C/W
AFS600-FG484	21.8	18.2	16.7	7.7	16.8	°C/W
AFS1500-FG484	21.6	16.8	15.2	5.6	14.9	°C/W
AFS1500-FG676	TBD	TBD	TBD	TBD	TBD	°C/W

Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³
Applicable to Pro I/O Banks				
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	-	474.70
2.5 V LVCMOS	35	2.5	-	270.73
1.8 V LVCMOS	35	1.8	-	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	-	104.55
3.3 V PCI	10	3.3	-	204.61
3.3 V PCI-X	10	3.3	-	204.61
Voltage-Referenced	•	•		
3.3 V GTL	10	3.3	-	24.08
2.5 V GTL	10	2.5	-	13.52
3.3 V GTL+	10	3.3	-	24.10
2.5 V GTL+	10	2.5	-	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential	•	•		
LVDS	-	2.5	7.70	89.62
LVPECL	-	3.3	19.42	168.02
Applicable to Advanced I/O Ban	ks	•		
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	468.67
2.5 V LVCMOS	35	2.5	-	267.48
1.8 V LVCMOS	35	1.8	-	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	-	103.12
3.3 V PCI	10	3.3	-	201.02
3.3 V PCI-X	10	3.3	-	201.02

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.

2. PDC8 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.

FG256							
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function			
R5	AV0	AV0	AV2	AV2			
R6	AT0	AT0	AT2	AT2			
R7	AV1	AV1	AV3	AV3			
R8	AT3	AT3	AT5	AT5			
R9	AV4	AV4	AV6	AV6			
R10	NC	AT5	AT7	AT7			
R11	NC	AV5	AV7	AV7			
R12	NC	NC	AT9	AT9			
R13	NC	NC	AG9	AG9			
R14	NC	NC	AC9	AC9			
R15	PUB	PUB	PUB	PUB			
R16	VCCIB1	VCCIB1	VCCIB2	VCCIB2			
T1	GND	GND	GND	GND			
T2	NCAP	NCAP	NCAP	NCAP			
Т3	VCC33N	VCC33N	VCC33N	VCC33N			
T4	NC	NC	ATRTN0	ATRTN0			
T5	AT1	AT1	AT3	AT3			
Т6	ATRTN0	ATRTN0	ATRTN1	ATRTN1			
Τ7	AT2	AT2	AT4	AT4			
Т8	ATRTN1	ATRTN1	ATRTN2	ATRTN2			
Т9	AT4	AT4	AT6	AT6			
T10	ATRTN2	ATRTN2	ATRTN3	ATRTN3			
T11	NC	NC	AT8	AT8			
T12	NC	NC	ATRTN4	ATRTN4			
T13	GNDA	GNDA	GNDA	GNDA			
T14	VCC33A	VCC33A	VCC33A	VCC33A			
T15	VAREF	VAREF	VAREF	VAREF			
T16	GND	GND	GND	GND			

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Package Pin Assignments

	FG676		FG676	FG676		
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	
C9	IO07PDB0V1	D19	GBC1/IO40PDB1V2	F3	IO121NDB4V0	
C10	IO09PDB0V1	D20	GBA1/IO42PDB1V2	F4	GND	
C11	IO13NDB0V2	D21	GND	F5	IO123NDB4V0	
C12	IO13PDB0V2	D22	VCCPLB	F6	GAC2/IO123PDB4V0	
C13	IO24PDB1V0	D23	GND	F7	GAA2/IO125PDB4V0	
C14	IO26PDB1V0	D24	NC	F8	GAC0/IO03NDB0V0	
C15	IO27NDB1V1	D25	NC	F9	GAC1/IO03PDB0V0	
C16	IO27PDB1V1	D26	NC	F10	IO10NDB0V1	
C17	IO35NDB1V2	E1	GND	F11	IO10PDB0V1	
C18	IO35PDB1V2	E2	IO122NPB4V0	F12	IO14NDB0V2	
C19	GBC0/IO40NDB1V2	E3	IO121PDB4V0	F13	IO23NDB1V0	
C20	GBA0/IO42NDB1V2	E4	IO122PPB4V0	F14	IO23PDB1V0	
C21	IO43NDB1V2	E5	IO00NDB0V0	F15	IO32NPB1V1	
C22	IO43PDB1V2	E6	IO00PDB0V0	F16	IO34NDB1V1	
C23	NC	E7	VCCIB0	F17	IO34PDB1V1	
C24	GND	E8	IO05NDB0V1	F18	IO37PDB1V2	
C25	NC	E9	IO05PDB0V1	F19	GBB1/IO41PDB1V2	
C26	NC	E10	VCCIB0	F20	VCCIB2	
D1	NC	E11	IO11NDB0V1	F21	IO47PPB2V0	
D2	NC	E12	IO14PDB0V2	F22	IO44NDB2V0	
D3	NC	E13	VCCIB0	F23	GND	
D4	GND	E14	VCCIB1	F24	IO45NDB2V0	
D5	GAA0/IO01NDB0V0	E15	IO29NDB1V1	F25	VCCIB2	
D6	GND	E16	IO29PDB1V1	F26	NC	
D7	IO04NDB0V0	E17	VCCIB1	G1	NC	
D8	IO04PDB0V0	E18	IO37NDB1V2	G2	IO119PPB4V0	
D9	GND	E19	GBB0/IO41NDB1V2	G3	IO120NDB4V0	
D10	IO09NDB0V1	E20	VCCIB1	G4	IO120PDB4V0	
D11	IO11PDB0V1	E21	VCOMPLB	G5	VCCIB4	
D12	GND	E22	GBA2/IO44PDB2V0	G6	GAB2/IO124PDB4V0	
D13	IO24NDB1V0	E23	IO48PPB2V0	G7	IO125NDB4V0	
D14	IO26NDB1V0	E24	GBB2/IO45PDB2V0	G8	GND	
D15	GND	E25	NC	G9	VCCIB0	
D16	IO31NDB1V1	E26	GND	G10	IO08NDB0V1	
D17	IO31PDB1V1	F1	NC	G11	IO08PDB0V1	
D18	GND	F2	VCCIB4	G12	GND	

Fusion Family of Mixed Signal FPGAs

	FG676		FG676	FG676		
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	
G13	IO22NDB1V0	H23	IO50NDB2V0	K7	IO114PDB4V0	
G14	IO22PDB1V0	H24	IO51PDB2V0	K8	IO117NDB4V0	
G15	GND	H25	NC	K9	GND	
G16	IO32PPB1V1	H26	GND	K10	VCC	
G17	IO36NPB1V2	J1	NC	K11	VCCIB0	
G18	VCCIB1	J2	VCCIB4	K12	GND	
G19	GND	J3	IO115PDB4V0	K13	VCCIB0	
G20	IO47NPB2V0	J4	GND	K14	VCCIB1	
G21	IO49PDB2V0	J5	IO116NDB4V0	K15	GND	
G22	VCCIB2	J6	IO116PDB4V0	K16	VCCIB1	
G23	IO46NDB2V0	J7	VCCIB4	K17	GND	
G24	GBC2/IO46PDB2V0	J8	IO117PDB4V0	K18	GND	
G25	IO48NPB2V0	J9	VCCIB4	K19	IO53NDB2V0	
G26	NC	J10	GND	K20	IO57PDB2V0	
H1	GND	J11	IO06NDB0V1	K21	GCA2/IO59PDB2V0	
H2	NC	J12	IO06PDB0V1	K22	VCCIB2	
H3	IO118NDB4V0	J13	IO16NDB0V2	K23	IO54NDB2V0	
H4	IO118PDB4V0	J14	IO16PDB0V2	K24	IO54PDB2V0	
H5	IO119NPB4V0	J15	IO28NDB1V1	K25	NC	
H6	IO124NDB4V0	J16	IO28PDB1V1	K26	NC	
H7	GND	J17	GND	L1	GND	
H8	VCOMPLA	J18	IO38PPB1V2	L2	NC	
H9	VCCPLA	J19	IO53PDB2V0	L3	IO112PPB4V0	
H10	VCCIB0	J20	VCCIB2	L4	IO113NDB4V0	
H11	IO12NDB0V1	J21	IO52PDB2V0	L5	GFB2/IO109PDB4V0	
H12	IO12PDB0V1	J22	IO52NDB2V0	L6	GFA2/IO110PDB4V0	
H13	VCCIB0	J23	GND	L7	IO112NPB4V0	
H14	VCCIB1	J24	IO51NDB2V0	L8	IO104PDB4V0	
H15	IO30NDB1V1	J25	VCCIB2	L9	IO111PDB4V0	
H16	IO30PDB1V1	J26	NC	L10	VCCIB4	
H17	VCCIB1	K1	NC	L11	GND	
H18	IO36PPB1V2	K2	NC	L12	VCC	
H19	IO38NPB1V2	К3	IO115NDB4V0	L13	GND	
H20	GND	K4	IO113PDB4V0	L14	VCC	
H21	IO49NDB2V0	K5	VCCIB4	L15	GND	
H22	IO50PDB2V0	K6	IO114NDB4V0	L16	VCC	