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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-1fg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-14 indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel Fusion Devices* application note.



Figure 2-14 • Clock Aggregation Tree Architecture

1.5 V Voltage Regulator

The 1.5 V voltage regulator uses an external pass transistor to generate 1.5 V from a 3.3 V supply. The base of the pass transistor is tied to PTBASE, the collector is tied to 3.3 V, and an emitter is tied to PTBASE and the 1.5 V supplies of the Fusion device. Figure 2-27 on page 2-31 shows the hook-up of the 1.5 V voltage regulator to an external pass transistor.

Microsemi recommends using a PN2222A or 2N2222A transistor. The gain of such a transistor is approximately 25, with a maximum base current of 20 mA. The maximum current that can be supported is 0.5 A. Transistors with different gain can also be used for different current requirements.

Table 2-18 • Electrical Characteristics

Symbol	Parameter	Condition		Min	Typical	Max	Units
VOUT	Output Voltage	Tj = 25°C		1.425	1.5	1.575	V
ICC33A	Operation Current	Tj = 25°C	ILOAD = 1 mA		11		mA
			ILOAD = 100 mA		11		mA
			ILOAD = 0.5 A		30		mA
∆VOUT	Load Regulation	Tj = 25°C	ILOAD = 1 mA to 0.5 A		90		mV
	Line Regulation	Tj = 25°C	VCC33A = 2.97 V to 3.63 V				
			ILOAD = 1 mA		10.6		mV/V
			VCC33A = 2.97 V to 3.63 V				
			ILOAD = 100 mA		12.1		mV/V
∆VOUT			VCC33A = 2.97 V to 3.63 V		10.0		
			ILOAD = 500 mA		10.6		mV/V
	Dropout Voltage*	Tj = 25⁰C	ILOAD = 1 mA		0.63		V
			ILOAD = 100 mA		0.84		V
			ILOAD = 0.5 A		1.35		V
IPTBASE	PTBase Current	Tj = 25°C	ILOAD = 1 mA		48		μA
			ILOAD = 100 mA		736		μA
			ILOAD = 0.5 A		12	20	mA

VCC33A = 3.3 V

Note: *Data collected with 2N2222A.

Byte Number in Bank			c	4 LSB of ADDR (READ)													
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ba 3 N	7																
<u>N</u>	6																
0 of	5																
AD	4																
	3																
(R	2																
	1																
9	0																

Figure 2-45 • FlashROM Architecture

FlashROM Characteristics



Figure 2-46 • FlashROM Timing Diagram

Table 2-26 • FlashROM Access Time

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{SU}	Address Setup Time	0.53	0.61	0.71	ns
t _{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t _{CK2Q}	Clock to Out	21.42	24.40	28.68	ns
F _{MAX}	Maximum Clock frequency	15.00	15.00	15.00	MHz





Figure 2-57 • FIFO Read





Table 2-36 describes each pin in the Analog Block. Each function within the Analog Block will be explained in detail in the following sections.

Table 2-36 • Analog Block Pin Description

Signal Name	Number of Bits	Direction	Function	Location of Details
VAREF	1	Input/Output	Voltage reference for ADC	ADC
ADCGNDREF	1	Input	External ground reference	ADC
MODE[3:0]	4	Input	ADC operating mode	ADC
SYSCLK	1	Input	External system clock	
TVC[7:0]	8	Input	Clock divide control	ADC
STC[7:0]	8	Input	Sample time control	ADC
ADCSTART	1	Input	Start of conversion	ADC
PWRDWN	1	Input	ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin.	ADC
ADCRESET	1	Input	ADC resets and disables Analog Quad – active high	ADC
BUSY	1	Output	1 – Running conversion	ADC
CALIBRATE	1	Output	1 – Power-up calibration	ADC
DATAVALID	1	Output	1 – Valid conversion result	ADC
RESULT[11:0]	12	Output	Conversion result	ADC
TMSTBINT	1	Input	Internal temp. monitor strobe	ADC
SAMPLE	1	Output	 1 – An analog signal is actively being sampled (stays high during signal acquisition only) 0 – No analog signal is being sampled 	ADC
VAREFSEL	1	Input	0 = Output internal voltage reference (2.56 V) to VAREF 1 = Input external voltage reference	ADC
	_		from VAREF and ADCGNDREF	
CHNUMBER[4:0]	5	Input	Analog input channel select	Input multiplexer
ACMCLK	1	Input	ACM clock	ACM
ACMWEN	1	Input	ACM write enable – active high	ACM
ACMRESET	1	Input	ACM reset – active low	ACM
ACMWDATA[7:0]	8	Input	ACM write data	ACM
ACMRDATA[7:0]	8	Output	ACM read data	ACM
ACMADDR[7:0]	8	Input	ACM address	ACM
CMSTB0 to CMSTB9	10	Input	Current monitor strobe – 1 per quad, active high	Analog Quad



Analog System Characteristics

Table 2-49 • Analog Channel Specifications

Commercial Temperature Range Conditions, T_J = 85°C (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Voltage Monitor	Using Analog Pads AV,	AC and AT (using prescaler)			l	
	Input Voltage (Prescaler)	Refer to Table 3-2 on page 3-3				
VINAP	Uncalibrated Gain and Offset Errors	Refer to Table 2-51 on page 2-122				
	Calibrated Gain and Offset Errors	Refer to Table 2-52 on page 2-123				
	Bandwidth1				100	KHz
	Input Resistance	Refer to Table 3-3 on page 3-4				
	Scaling Factor	Prescaler modes (Table 2-57 on page 2-130)				
	Sample Time		10			μs
Current Monitor	Using Analog Pads AV	and AC		•		
VRSM ¹	Maximum Differential Input Voltage				VAREF / 10	mV
	Resolution	Refer to "Current Monitor" section				
	Common Mode Range				- 10.5 to +12	V
CMRR	Common Mode Rejection Ratio	DC – 1 KHz		60		dB
		1 KHz - 10 KHz		50		dB
		> 10 KHz		30		dB
t _{CMSHI}	Strobe High time		ADC conv. time		200	μs
t _{CMSHI}	Strobe Low time		5			μs
t _{CMSHI}	Settling time		0.02			μs
	Accuracy	Input differential voltage > 50 mV			-2 -(0.05 x VRSM) to +2 + (0.05 x VRSM)	mV

Notes:

1. VRSM is the maximum voltage drop across the current sense resistor.

2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.

- 3. VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.
- 4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
- 5. The temperature offset is a fixed positive value.
- 6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
- 7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.

Table 2-50 • ADC Characteristics in Direct Input ModeCommercial Temperature Range Conditions, TJ = 85°C (unless noted otherwise),Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Direct Input	using Analog Pad AV, AC, A	Г				
VINADC	Input Voltage (Direct Input)	Refer to Table 3-2 on page 3-3				
CINADC	Input Capacitance	Channel not selected		7		pF
		Channel selected but not sampling		8		pF
		Channel selected and sampling		18		pF
ZINADC	Input Impedance	8-bit mode		2		kΩ
		10-bit mode		2		kΩ
		12-bit mode		2		kΩ
Analog Refe	erence Voltage VAREF					
VAREF	Accuracy	T _J = 25°C	2.537	2.56	2.583	V
	Temperature Drift of Internal Reference			65		ppm / °C
	External Reference		2.527		VCC33A + 0.05	V
ADC Accura	acy (using external reference) 1,2				
DC Accurac	у					
TUE	Total Unadjusted Error	8-bit mode		0.2	29	LSB
		10-bit mode		0.7	72	LSB
		12-bit mode		1.	8	LSB
INL	Integral Non-Linearity	8-bit mode		0.20	0.25	LSB
		10-bit mode		0.32	0.43	LSB
		12-bit mode		1.71	1.80	LSB
DNL	Differential Non-Linearity (no missing code)	8-bit mode		0.20	0.24	LSB
		10-bit mode		0.60	0.65	LSB
		12-bit mode		2.40	2.48	LSB
	Offset Error	8-bit mode		0.01	0.17	LSB
		10-bit mode		0.05	0.20	LSB
		12-bit mode		0.20	0.40	LSB
	Gain Error	8-bit mode		0.0004	0.003	LSB
		10-bit mode		0.002	0.011	LSB
		12-bit mode		0.007	0.044	LSB
	Gain Error (with internal reference)	All modes		2		% FSR

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.



Device Architecture

Table 2-50 • ADC Characteristics in Direct Input Mode (continued)

Commercial Temperature Range Conditions, $T_J = 85^{\circ}C$ (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Dynamic Pe	erformance					
SNR	Signal-to-Noise Ratio	8-bit mode	48.0	49.5		dB
		10-bit mode	58.0	60.0		dB
		12-bit mode	62.9	64.5		dB
SINAD	Signal-to-Noise Distortion	8-bit mode	47.6	49.5		dB
		10-bit mode	57.4	59.8		dB
		12-bit mode	62.0	64.2		dB
THD	Total Harmonic Distortion	8-bit mode		-74.4	-63.0	dBc
		10-bit mode		-78.3	-63.0	dBc
		12-bit mode		-77.9	-64.4	dBc
ENOB	Effective Number of Bits	8-bit mode	7.6	7.9		bits
		10-bit mode	9.5	9.6		bits
		12-bit mode	10.0	10.4		bits
Conversion	Rate					
	Conversion Time	8-bit mode	1.7			μs
		10-bit mode	1.8			μs
		12-bit mode	2			μs
	Sample Rate	8-bit mode			600	Ksps
		10-bit mode			550	Ksps
		12-bit mode			500	Ksps

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.

Timing Characteristics

Table 2-55 • Analog Configuration Multiplexer (ACM) TimingCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{CLKQACM}	Clock-to-Q of the ACM	19.73	22.48	26.42	ns
t _{SUDACM}	Data Setup time for the ACM		5.00	5.88	ns
t _{HDACM}	Data Hold time for the ACM	0.00	0.00	0.00	ns
t _{SUAACM}	Address Setup time for the ACM	4.73	5.38	6.33	ns
t _{HAACM}	Address Hold time for the ACM	0.00	0.00	0.00	ns
t _{SUEACM}	Enable Setup time for the ACM	3.93	4.48	5.27	ns
t _{HEACM}	Enable Hold time for the ACM	0.00	0.00	0.00	ns
t _{MPWARACM}	Asynchronous Reset Minimum Pulse Width for the ACM	10.00	10.00	10.00	ns
t _{REMARACM}	Asynchronous Reset Removal time for the ACM	12.98	14.79	17.38	ns
t _{RECARACM}	Asynchronous Reset Recovery time for the ACM	12.98	14.79	17.38	ns
t _{MPWCLKACM}	Clock Minimum Pulse Width for the ACM	45.00	45.00	45.00	ns
t _{FMAXCLKACM}	lock Maximum Frequency for the ACM	10.00	10.00	10.00	MHz

User I/Os

Introduction

Fusion devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-68, Table 2-69, Table 2-70, and Table 2-71 on page 2-135 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V–tolerant. See the "5 V Input Tolerance" section on page 2-144 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-5 for more information. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, digital inputs are tristated, digital outputs are tristated, and digital bibufs (input/output) are tristated.

I/O Tile

The Fusion I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-99 on page 2-133). The registers can also be used to support the JESD-79C DDR standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-139 for more information).

As depicted in Figure 2-100 on page 2-138, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-138 for more information.

I/O Banks and I/O Standards Compatibility

The digital I/Os are grouped into I/O voltage banks. There are three digital I/O banks on the AFS090 and AFS250 devices and four digital I/O banks on the AFS600 and AFS1500 devices. Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159 show the bank configuration by device. The north side of the I/O in the AFS600 and AFS1500 devices comprises two banks of Pro I/Os. The Pro I/Os support a wide number of voltage-referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all Microsemi digital I/Os. Each I/O voltage bank has dedicated I/O supply and ground voltages (VCCI/GNDQ for input buffers and VCCI/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-69 and Table 2-70 on page 2-134 show the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Package Pin Assignments" on page 4-1 and the "User I/O Naming Convention" section on page 2-158.

Each Pro I/O bank is divided into minibanks. Any user I/O in a VREF minibank (a minibank is the region of scope of a VREF pin) can be configured as a VREF pin (Figure 2-99 on page 2-133). Only one VREF pin is needed to control the entire VREF minibank. The location and scope of the VREF minibanks can be determined by the I/O name. For details, see the "User I/O Naming Convention" section on page 2-158.

Table 2-70 on page 2-134 shows the I/O standards supported by Fusion devices and the corresponding voltage levels.

I/O standards are compatible if the following are true:

- Their VCCI values are identical.
- If both of the standards need a VREF, their VREF values must be identical (Pro I/O only).





Figure 2-99 • Fusion Pro I/O Bank Detail Showing VREF Minibanks (north side of AFS600 and AFS1500)

Table 2-67 • I/O Standards	Supported by	Bank Type
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I/O Bank	Single-Ended I/O Standards	Differential I/O Standards	Voltage-Referenced	Hot- Swap
Standard I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V	-	_	Yes
Advanced I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X	LVPECL and LVDS	-	-
Pro I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X	LVPECL and LVDS	GTL+2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II	Yes



At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 2-110 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-111 shows how bus contention is created, and Figure 2-112 on page 2-151 shows how it can be avoided with the skew circuit.







Figure 2-111 • Timing Diagram (bypasses skew circuit)





Figure 2-116 • Input Buffer Timing Model and Delays (example)

Table 2-169 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	put Low (V) Input High (V)		VREF (typ.) (V)
1.075	1.325	Cross point	_

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-170 • LVDS

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Pro I/Os

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	0.66	2.10	0.04	1.82	ns
-1	0.56	1.79	0.04	1.55	ns
-2	0.49	1.57	0.03	1.36	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations can contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus, since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-135. The input and output buffer delays are available in the LVDS section in Table 2-171.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case industrial operating conditions at the farthest receiver: $R_S = 60 \Omega$ and $R_T = 70 \Omega$, given $Z_0 = 50 \Omega$ (2") and $Z_{stub} = 50 \Omega$ (~1.5").



Figure 2-135 • BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers



Device Architecture

Output DDR



Figure 2-144 • Output DDR Timing Model

Table 2-181 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
t _{DDROCLKQ}	Clock-to-Out	B, E
t _{DDROCLR2Q}	Asynchronous Clear-to-Out	C, E
t _{DDROREMCLR}	Clear Removal	С, В
t _{DDRORECCLR}	Clear Recovery	С, В
t _{DDROSUD1}	Data Setup Data_F	А, В
t _{DDROSUD2}	Data Setup Data_R	D, B
t _{DDROHD1}	Data Hold Data_F	А, В
t _{DDROHD2}	Data Hold Data_R	D, B

ATRTNx Temperature Monitor Return

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The x in the ATRTNx designator indicates the quad pairing (x = 0 for AQ1 and AQ2, x = 1 for AQ2 and AQ3, ..., x = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURNxy in the software (where x and y refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-22.

Refer to the "User I/O Naming Convention" section on page 2-158 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pullup/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to Table 2-183 for more information.

VJTAG	Tie-Off Resistance ^{2, 3}
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Table 2-183 • Recommended Tie-Off Values for the TCK and TRST Pins

Notes:

- 1. Equivalent parallel resistance if more than one device is on JTAG chain.
- 2. The TCK pin can be pulled up/down.
- 3. The TRST pin can only be pulled down.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the *Fusion Security* application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4 × 10³⁸ possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note *Fusion Security* for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T _J = 0°C	FPGA/FlashROM	500	20 years
	Max. T _J = 85°C	Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years
Industrial	Min. T _J = –40°C	FPGA/FlashROM	500	20 years
	Max. T _J = 100°C	Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

Table 3-5 • FPGA Programming, Storage, and Operating Limits

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every Fusion device. These circuits ensure easy transition from the powered off state to the powered up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1 on page 3-6.

There are five regions to consider during power-up.

Fusion I/Os are activated only if ALL of the following three conditions are met:

- 1. VCC and VCCI are above the minimum specified trip points (Figure 3-1).
- 2. VCCI > VCC 0.75 V (typical).
- 3. Chip is in the operating mode.

V_{CCI} Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

- 1. Core
- 2. Input buffers
- 3. Output buffers, after 200 ns delay from input buffer activation

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper powerup behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels. The V_{CC} activation level is specified as 1.1 V worst-case (see Figure 3-1 on page 3-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V \pm 0.25 V), the PLL output lock signal goes low and/or the output clock is lost.



FG256				
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function
C7	IO09RSB0V0	IO12RSB0V0	IO06NDB0V0	IO09NDB0V1
C8	IO14RSB0V0	IO22RSB0V0	IO16PDB1V0	IO23PDB1V0
C9	IO15RSB0V0	IO23RSB0V0	IO16NDB1V0	IO23NDB1V0
C10	IO22RSB0V0	IO30RSB0V0	IO25NDB1V1	IO31NDB1V1
C11	IO20RSB0V0	IO31RSB0V0	IO25PDB1V1	IO31PDB1V1
C12	VCCIB0	VCCIB0	VCCIB1	VCCIB1
C13	GBB1/IO28RSB0V0	GBC1/IO35RSB0V0	GBC1/IO26PPB1V1	GBC1/IO40PPB1V2
C14	VCCIB1	VCCIB1	VCCIB2	VCCIB2
C15	GND	GND	GND	GND
C16	VCCIB1	VCCIB1	VCCIB2	VCCIB2
D1	GFC2/IO50NPB3V0	IO75NDB3V0	IO84NDB4V0	IO124NDB4V0
D2	GFA2/IO51NDB3V0	GAB2/IO75PDB3V0	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
D3	GAC2/IO51PDB3V0	IO76NDB3V0	IO85NDB4V0	IO125NDB4V0
D4	GAA2/IO52PDB3V0	GAA2/IO76PDB3V0	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D5	GAB2/IO52NDB3V0	GAB0/IO02RSB0V0	GAB0/IO02NPB0V0	GAB0/IO02NPB0V0
D6	GAC0/IO04RSB0V0	GAC0/IO04RSB0V0	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	IO08RSB0V0	IO13RSB0V0	IO06PDB0V0	IO09PDB0V1
D8	NC	IO20RSB0V0	IO14NDB0V1	IO15NDB0V2
D9	NC	IO21RSB0V0	IO14PDB0V1	IO15PDB0V2
D10	IO21RSB0V0	IO28RSB0V0	IO23PDB1V1	IO37PDB1V2
D11	IO23RSB0V0	GBB0/IO36RSB0V0	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2
D12	NC	NC	VCCIB1	VCCIB1
D13	GBA2/IO31PDB1V0	GBA2/IO40PDB1V0	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
D14	GBB2/IO31NDB1V0	IO40NDB1V0	IO30NDB2V0	IO44NDB2V0
D15	GBC2/IO32PDB1V0	GBB2/IO41PDB1V0	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D16	GCA2/IO32NDB1V0	IO41NDB1V0	IO31NDB2V0	IO45NDB2V0
E1	GND	GND	GND	GND
E2	GFB0/IO48NPB3V0	IO73NDB3V0	IO81NDB4V0	IO118NDB4V0
E3	GFB2/IO50PPB3V0	IO73PDB3V0	IO81PDB4V0	IO118PDB4V0
E4	VCCIB3	VCCIB3	VCCIB4	VCCIB4
E5	NC	IO74NPB3V0	IO83NPB4V0	IO123NPB4V0
E6	NC	IO08RSB0V0	IO04NPB0V0	IO05NPB0V1
E7	GND	GND	GND	GND
E8	NC	IO18RSB0V0	IO08PDB0V1	IO11PDB0V1
E9	NC	NC	IO20NDB1V0	IO27NDB1V1
E10	GND	GND	GND	GND
E11	IO24RSB0V0	GBB1/IO37RSB0V0	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
E12	NC	IO50PPB1V0	IO33PSB2V0	IO48PSB2V0



Datasheet Information

Revision	Changes	Page
Revision 2 (continued)	A note was added to Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro) stating that the user is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off (SAR 21773).	2-31
	VPUMP was incorrectly represented as VPP in several places. This was corrected to VPUMP in the "Standby and Sleep Mode Circuit Implementation" section and Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics (21963).	2-32, 3-10
	Additional information was added to the Flash Memory Block "Write Operation" section, including an explanation of the fact that a copy-page operation takes no less than 55 cycles (SAR 26338).	2-45
	The "FlashROM" section was revised to refer to Figure 2-46 • FlashROM Timing Diagram and Table 2-26 • FlashROM Access Time rather than stating 20 MHz as the maximum FlashROM access clock and 10 ns as the time interval for D0 to become valid or invalid (SAR 22105).	2-53, 2-54
	The following figures were deleted (SAR 29991). Reference was made to a new application note, <i>Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs</i> , which covers these cases in detail (SAR 34862).	
	Figure 2-55 • Write Access after Write onto Same Address	
	Figure 2-56 • Read Access after Write onto Same Address	
	Figure 2-57 • Write Access after Read onto Same Address	
	The port names in the SRAM "Timing Waveforms", "Timing Characteristics", SRAM tables, Figure 2-55 • RAM Reset. Applicable to both RAM4K9 and RAM512x18., and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35753).	2-63, 2-66, 2-65, 2-75
	In several places throughout the datasheet, GNDREF was corrected to ADCGNDREF (SAR 20783):	
	Figure 2-64 • Analog Block Macro	2-77
	Table 2-36 • Analog Block Pin Description	2-78
	"ADC Operation" section	2-104
	The following note was added below Figure 2-78 • Timing Diagram for the Temperature Monitor Strobe Signal:	2-93
	When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a $1 \mu A$ sink into the Fusion device. (SAR 24796).	
	The "Analog-to-Digital Converter Block" section was extensively revised, reorganizing the information and adding the "ADC Theory of Operation" section and "Acquisition Time or Sample Time Control" section. The "ADC Example" section was reworked and corrected (SAR 20577).	2-96
	Table 2-49 • Analog Channel Specifications was modified to include calibrated and uncalibrated values for offset (AFS090 and AFS250) for the external and internal temperature monitors. The "Offset" section was revised accordingly and now references Table 2-49 • Analog Channel Specifications (SARs 22647, 27015).	2-95, 2-117
	The "Intra-Conversion" section and "Injected Conversion" section had definitions incorrectly interchanged and have been corrected. Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram were also incorrectly interchanged and have been replaced correctly. Reference in the figure notes to EQ 10 has been corrected to EQ 23 (SAR 20547).	2-110, 2-113, 2-113