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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	·
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-1fg256i

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Clocking Resources

The Fusion family has a robust collection of clocking peripherals, as shown in the block diagram in Figure 2-16. These on-chip resources enable the creation, manipulation, and distribution of many clock signals. The Fusion integrated RC oscillator produces a 100 MHz clock source with no external components. For systems requiring more precise clock signals, the Fusion family supports an on-chip crystal oscillator circuit. The integrated PLLs in each Fusion device can use the RC oscillator, crystal oscillator, or another on-chip clock signal as a source. These PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay). Utilizing the CCC found in the popular ProASIC3 family, Fusion incorporates six CCC blocks. The CCCs allow access to Fusion global and local clock distribution nets, as described in the "Global Resources (VersaNets)" section on page 2-11.



Figure 2-16 • Fusion Clocking Options

CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- · 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • PLL Block

Voltage Regulator and Power System Monitor (VRPSM)

The VRPSM macro controls the power-up state of the FPGA. The power-up bar (PUB) pin can turn on the voltage regulator when set to 0. TRST can enable the voltage regulator when deasserted, allowing the FPGA to power-up when user want access to JTAG ports. The inputs VRINITSTATE and RTCPSMMATCH come from the flash bits and RTC, and can also power up the FPGA.



Note: *Signals are hardwired internally and do not exist in the macro core.

Figure 2-30 • VRPSM Macro

Table 2-17 • VRPSM Signal Descriptions

Signal Name	Width	Direction	Function
VRPU	1	In	Voltage Regulator Power-Up
			0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator.
			1 – Voltage regulator enabled
VRINITSTATE	1	In	Voltage Regulator Initial State
			Defines the voltage Regulator status upon power-up of the 3.3 V. The signal is configured by Libero SoC when the VRPSM macro is generated.
			Tie off to 1 – Voltage regulator enables when 3.3 V is powered.
			Tie off to 0 – Voltage regulator disables when 3.3 V is powered.
RTCPSMMATCH	1	In	RTC Power System Management Match
			Connect from RTCPSMATCH signal from RTC in AB
			0 transition to 1 turns on the voltage regulator
PUB	1	In	External pin, built-in weak pull-up
			Power-Up Bar
			0 – Enables voltage regulator at all times
TRST*	1	In	External pin, JTAG Test Reset
			1 – Enables voltage regulator at all times
FPGAGOOD	1	Out	Indicator that the FPGA is powered and functional
			No need to connect if it is not used.
			1 – Indicates that the FPGA is powered up and functional.
			0 – Not possible to read by FPGA since it has already powered off.
PUCORE	1	Out	Power-Up Core
			Inverted signal of PUB. No need to connect if it is not used.
VREN*	1	Out	Voltage Regulator Enable
			Connected to 1.5 V voltage regulator in Fusion device internally.
			0 – Voltage regulator disables
			1 – Voltage regulator enables
Note: *Signals a	re hard	wired interr	ally and do not exist in the macro core.



Flash Memory Block Addressing

Figure 2-34 shows a graphical representation of the flash memory block.



Figure 2-34 • Flash Memory Block Organization

Each FB is partitioned into sectors, pages, blocks, and bytes. There are 64 sectors in an FB, and each sector contains 32 pages and 1 spare page. Each page contains 8 data blocks and 1 auxiliary block. Each data block contains 16 bytes of user data, and the auxiliary block contains 4 bytes of user data. Addressing for the FB is shown in Table 2-20.

Table 2-20 • FB Address Bit Allocation ADDR[17:0]

17	12	11	7	6	4	3	0
Sec	ctor	Pa	ge	Blo	ock	Ву	/te

When the spare page of a sector is addressed (SPAREPAGE active), ADDR[11:7] are ignored.

When the Auxiliary block is addressed (AUXBLOCK active), ADDR[6:2] are ignored.

Note: The spare page of sector 0 is unavailable for any user data. Writes to this page will return an error, and reads will return all zeroes.



Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-35 on page 2-45 illustrates the multiple Write operations.



Figure 2-35 • FB Write Waveform

When a Write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. A Copy Page operation takes no less than 55 cycles and could take more if a Write or Unprotect Page operation is started while the NVM is busy pre-fetching a block. The basic operation is to read a block from the array into the block register (5 cycles) and then write the block register to the page buffer (1 cycle) and if necessary, when the copy is complete, reading the block being written from the page buffer into the block buffer (1 cycle). A page contains 9 blocks, so 9 blocks multiplied by 6 cycles to read/write each block, plus 1 is 55 cycles total. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates that an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky"; it is unchanged until another operation is started.

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

- 1. Attempting to write a page that is Overwrite Protected (STATUS = '01'). The write is not performed.
- 2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = '11'). The write is not performed.



SRAM Characteristics

Timing Waveforms







Figure 2-51 • RAM Read for Pipelined Output. Applicable to both RAM4K9 and RAM512x18.

Fusion Family of Mixed Signal FPGAs









Device Architecture

Timing Characteristics

Table 2-35 • FIFO

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ENS}	REN, WEN Setup time	1.34	1.52	1.79	ns
t _{ENH}	REN, WEN Hold time	0.00	0.00	0.00	ns
t _{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t _{вкн}	BLK Hold time	0.00	0.00	0.00	ns
t _{DS}	Input data (WD) Setup time	0.18	0.21	0.25	ns
t _{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t _{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t _{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t _{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t _{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t _{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t _{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.13	6.98	8.20	ns
+	RESET Low to Data out Low on RD (flow-through)	0.92	1.05	1.23	ns
^I RSTBQ	RESET Low to Data out Low on RD (pipelined)	0.92	1.05	1.23	ns
t _{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t _{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t _{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t _{CYC}	Clock Cycle time	3.23	3.68	4.32	ns
F _{MAX}	Maximum Frequency for FIFO	310	272	231	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Device Architecture

Intra-Conversion



Note: **t*_{CONV} represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, *t*_{CONV}.

Figure 2-92 • Intra-Conversion Timing Diagram



Injected Conversion

Note: *See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.

Figure 2-93 • Injected Conversion Timing Diagram

Table 2-96 • I/O Output Buffer Maximum Resistances ¹ (continued)

Standard	Drive Strength	R _{PULL-DOWN} (ohms) ²	R _{PULL-UP} (ohms) ³
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	17 mA	27	31
SSTL2 (II)	21 mA	13	15
SSTL3 (I)	16 mA	44	69
SSTL3 (II)	24 mA	18	32
Applicable to Advanced I/O Ba	nks		•
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

 These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.

2. R_(PULL-DOWN-MAX) = VOLspec / I_{OLspec}

3. R_(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec



Device Architecture

Table 2-98 • I/O Short Currents IOSH/IOSL (continued)

	Drive Strength	IOSH (mA)*	IOSL (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109
Applicable to Standard I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16

Note: $^{*}T_{J} = 100^{\circ}C$

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Microsemi.

Device Architecture

Table 2-130 • 1.5 V LVCMOS Low Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Advanced I/Os

Drive	Speed												
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	12.78	0.04	1.31	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	-1	0.56	10.87	0.04	1.11	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	-2	0.49	9.55	0.03	0.98	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.31	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	-1	0.56	8.51	0.04	1.11	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	-2	0.49	7.47	0.03	0.98	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
8 mA	Std.	0.66	9.33	0.04	1.31	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	-1	0.56	7.94	0.04	1.11	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	-2	0.49	6.97	0.03	0.98	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.31	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	-1	0.56	7.58	0.04	1.11	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	-2	0.49	6.65	0.03	0.98	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-131 • 1.5 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Advanced I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
2 mA	Std.	0.66	8.36	0.04	1.44	0.43	6.82	8.36	3.39	2.77	9.06	10.60	ns
	-1	0.56	7.11	0.04	1.22	0.36	5.80	7.11	2.88	2.35	7.71	9.02	ns
	-2	0.49	6.24	0.03	1.07	0.32	5.10	6.24	2.53	2.06	6.76	7.91	ns
4 mA	Std.	0.66	5.31	0.04	1.44	0.43	4.85	5.31	3.74	3.40	7.09	7.55	ns
	-1	0.56	4.52	0.04	1.22	0.36	4.13	4.52	3.18	2.89	6.03	6.42	ns
	-2	0.49	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns
8 mA	Std.	0.66	4.67	0.04	1.44	0.43	4.55	4.67	3.82	3.56	6.78	6.90	ns
	-1	0.56	3.97	0.04	1.22	0.36	3.87	3.97	3.25	3.03	5.77	5.87	ns
	-2	0.49	3.49	0.03	1.07	0.32	3.40	3.49	2.85	2.66	5.07	5.16	ns
12 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	-1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	-2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

SSTL3 Class II		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
21 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Table 2-165 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-133 • AC Loading

Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-167 • SSTL3- Class II Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
-1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
-2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



DDR Module Specifications

Input DDR Module



Figure 2-142 • Input DDR Timing Model

Table 2-179 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t _{DDRICLKQ1}	Clock-to-Out Out_QR	B, D
t _{DDRICLKQ2}	Clock-to-Out Out_QF	B, E
t _{DDRISUD}	Data Setup Time of DDR Input	А, В
t _{DDRIHD}	Data Hold Time of DDR Input	А, В
t _{DDRICLR2Q1}	Clear-to-Out Out_QR	C, D
t _{DDRICLR2Q2}	Clear-to-Out Out_QF	C, E
t _{DDRIREMCLR}	Clear Removal	С, В
t _{DDRIRECCLR}	Clear Recovery	С, В

VCC Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the Fusion device.

VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are either four (AFS090 and AFS250) or five (AFS600 and AFS1500) I/O banks on the Fusion devices plus a dedicated VJTAG bank.

Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VCCPLA/B PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V, where A and B refer to the PLL. AFS090 and AFS250 each have a single PLL. The AFS600 and AFS1500 devices each have two PLLs. Microsemi recommends tying VCCPLX to VCC and using proper filtering circuits to decouple VCC noise from PLL.

If unused, VCCPLA/B should be tied to GND.

VCOMPLA/B Ground for West and East PLL

VCOMPLA is the ground of the west PLL (CCC location F) and VCOMPLB is the ground of the east PLL (CCC location C).

VJTAG JTAG Supply Voltage

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a Fusion device is in a JTAG chain of interconnected boards and it is desired to power down the board containing the Fusion device, this may be done provided both VJTAG and VCC to the Fusion part remain powered; otherwise, JTAG signals will not be able to transition the Fusion device, even in bypass mode.

VPUMP Programming Supply Voltage

Fusion devices support single-voltage ISP programming of the configuration flash and FlashROM. For programming, VPUMP should be in the 3.3 V +/-5% range. During normal device operation, VPUMP can be left floating or can be tied to any voltage between 0 V and 3.6 V.

When the VPUMP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Power per I/O Pin

Table 3-12 • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings

	VCCI (V)	Static Power PDC7 (mW) ¹	Dynamic Power PAC9 (µW/MHz) ²
Applicable to Pro I/O Banks	<u> </u>		
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3		17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	_	25.51
2.5 V LVCMOS	2.5	_	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	_	7.16
1.8 V LVCMOS	1.8	_	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	_	2.80
1.5 V LVCMOS (JESD8-11)	1.5	_	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	_	2.00
3.3 V PCI	3.3	_	18.82
3.3 V PCI – Schmitt trigger	3.3	_	20.12
3.3 V PCI-X	3.3	_	18.82
3.3 V PCI-X – Schmitt trigger	3.3	_	20.12
Voltage-Referenced	<u></u>		
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential	<u>.</u>		•
LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. PDC7 is the static power (where applicable) measured on VCCI.

2. PAC9 is the total dynamic power measured on VCC and VCCI.



Total Static Power Consumption—PSTAT

Number of Quads used: $N_{QUADS} = 4$ Number of NVM blocks available (AFS600): $N_{NVM-BLOCKS} = 2$ Number of input pins used: $N_{INPUTS} = 30$ Number of output pins used: $N_{OUTPUTS} = 40$

Operating Mode

 $\mathsf{P}_{\mathsf{STAT}} = \mathsf{PDC1} + (\mathsf{N}_{\mathsf{NVM-BLOCKS}} * \mathsf{PDC4}) + \mathsf{PDC5} + (\mathsf{N}_{\mathsf{QUADS}} * \mathsf{PDC6}) + (\mathsf{N}_{\mathsf{INPUTS}} * \mathsf{PDC7}) + (\mathsf{N}_{\mathsf{OUTPUTS}} * \mathsf{PDC8})$

P_{STAT} = 7.50 mW + (2 * 1.19 mW) + 8.25 mW + (4 * 3.30 mW) + (30 * 0.00) + (40 * 0.00)

P_{STAT} = 31.33 mW

Standby Mode

P_{STAT} = PDC2

 $P_{STAT} = 0.03 \text{ mW}$

Sleep Mode

 $P_{STAT} = PDC3$

 $P_{STAT} = 0.03 \text{ mW}$

Total Power Consumption—PTOTAL

In operating mode, the total power consumption of the device is 174.39 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{TOTAL} = 143.06 mW + 31.33 mW

P_{TOTAL} = 174.39 mW

In standby mode, the total power consumption of the device is limited to 0.66 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

 $P_{TOTAL} = 0.03 \text{ mW} + 0.63 \text{ mW}$

 $P_{TOTAL} = 0.66 \text{ mW}$

In sleep mode, the total power consumption of the device drops as low as 0.03 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$ $P_{TOTAL} = 0.03 \text{ mW}$



Package Pin Assignments

FG256					
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function	
H3	XTAL2	XTAL2	XTAL2	XTAL2	
H4	XTAL1	XTAL1	XTAL1	XTAL1	
H5	GNDOSC	GNDOSC	GNDOSC	GNDOSC	
H6	VCCOSC	VCCOSC	VCCOSC	VCCOSC	
H7	VCC	VCC	VCC	VCC	
H8	GND	GND	GND	GND	
H9	VCC	VCC	VCC	VCC	
H10	GND	GND	GND	GND	
H11	GDC0/IO38NDB1V0	IO51NDB1V0	IO47NDB2V0	IO69NDB2V0	
H12	GDC1/IO38PDB1V0	IO51PDB1V0	IO47PDB2V0	IO69PDB2V0	
H13	GDB1/IO39PDB1V0	GCA1/IO49PDB1V0	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0	
H14	GDB0/IO39NDB1V0	GCA0/IO49NDB1V0	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0	
H15	GCA0/IO36NDB1V0	GCB0/IO48NDB1V0	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0	
H16	GCA1/IO36PDB1V0	GCB1/IO48PDB1V0	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0	
J1	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0	
J2	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0	
J3	IO43NDB3V0	GFB0/IO67NDB3V0	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0	
J4	GEC2/IO43PDB3V0	GFB1/IO67PDB3V0	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0	
J5	NC	GFC0/IO68NDB3V0	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0	
J6	NC	GFC1/IO68PDB3V0	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0	
J7	GND	GND	GND	GND	
J8	VCC	VCC	VCC	VCC	
J9	GND	GND	GND	GND	
J10	VCC	VCC	VCC	VCC	
J11	GDC2/IO41NPB1V0	IO56NPB1V0	IO56NPB2V0	IO83NPB2V0	
J12	NC	GDB0/IO53NPB1V0	GDB0/IO53NPB2V0	GDB0/IO80NPB2V0	
J13	NC	GDA1/IO54PDB1V0	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0	
J14	GDA0/IO40PDB1V0	GDC1/IO52PPB1V0	GDC1/IO52PPB2V0	GDC1/IO79PPB2V0	
J15	NC	IO50NPB1V0	IO51NSB2V0	IO77NSB2V0	
J16	GDA2/IO40NDB1V0	GDC0/IO52NPB1V0	GDC0/IO52NPB2V0	GDC0/IO79NPB2V0	
K1	NC	IO65NPB3V0	IO67NPB4V0	IO92NPB4V0	
K2	VCCIB3	VCCIB3	VCCIB4	VCCIB4	
K3	NC	IO65PPB3V0	IO67PPB4V0	IO92PPB4V0	
K4	NC	IO64PDB3V0	IO65PDB4V0	IO96PDB4V0	
K5	GND	GND	GND	GND	
K6	NC	IO64NDB3V0	IO65NDB4V0	IO96NDB4V0	
K7	VCC	VCC	VCC	VCC	
K8	GND	GND	GND	GND	

	FG484		FG484		
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
P21	IO51PDB2V0	IO73PDB2V0	T12	AV5	AV5
P22	IO49NDB2V0	IO71NDB2V0	T13	AC5	AC5
R1	IO69PDB4V0	IO102PDB4V0	T14	NC	NC
R2	IO69NDB4V0	IO102NDB4V0	T15	GNDA	GNDA
R3	VCCIB4	VCCIB4	T16	NC	IO77PPB2V0
R4	IO64PDB4V0	IO91PDB4V0	T17	NC	IO74PDB2V0
R5	IO64NDB4V0	IO91NDB4V0	T18	VCCIB2	VCCIB2
R6	NC	IO92PDB4V0	T19	IO55NDB2V0	IO82NDB2V0
R7	GND	GND	T20	GDA2/IO55PDB2V0	GDA2/IO82PDB2V0
R8	GND	GND	T21	GND	GND
R9	VCC33A	VCC33A	T22	GDC1/IO52PDB2V0	GDC1/IO79PDB2V0
R10	GNDA	GNDA	U1	IO67PDB4V0	IO98PDB4V0
R11	VCC33A	VCC33A	U2	IO67NDB4V0	IO98NDB4V0
R12	GNDA	GNDA	U3	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0
R13	VCC33A	VCC33A	U4	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0
R14	GNDA	GNDA	U5	GND	GND
R15	VCC	VCC	U6	VCCNVM	VCCNVM
R16	GND	GND	U7	VCCIB4	VCCIB4
R17	NC	IO74NDB2V0	U8	VCC15A	VCC15A
R18	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0	U9	GNDA	GNDA
R19	GDB0/IO53NDB2V0	GDB0/IO80NDB2V0	U10	AC4	AC4
R20	VCCIB2	VCCIB2	U11	VCC33A	VCC33A
R21	IO50NDB2V0	IO75NDB2V0	U12	GNDA	GNDA
R22	IO50PDB2V0	IO75PDB2V0	U13	AG5	AG5
T1	NC	IO100PPB4V0	U14	GNDA	GNDA
T2	GND	GND	U15	PUB	PUB
Т3	IO66PDB4V0	IO95PDB4V0	U16	VCCIB2	VCCIB2
T4	IO66NDB4V0	IO95NDB4V0	U17	TDI	TDI
T5	VCCIB4	VCCIB4	U18	GND	GND
Т6	NC	IO92NDB4V0	U19	IO57NDB2V0	IO84NDB2V0
T7	GNDNVM	GNDNVM	U20	GDC2/IO57PDB2V0	GDC2/IO84PDB2V0
Т8	GNDA	GNDA	U21	NC	IO77NPB2V0
Т9	NC	NC	U22	GDC0/IO52NDB2V0	GDC0/IO79NDB2V0
T10	AV4	AV4	V1	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0
T11	NC	NC	V2	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0

Revision	Changes	Page
Revision 3 (continued)	The "RC Oscillator" section was revised to correct a sentence that did not differentiate accuracy for commercial and industrial temperature ranges, which is given in Table 2-9 • Electrical Characteristics of RC Oscillator (SAR 33722).	2-19
	Figure 2-57 • FIFO Read and Figure 2-58 • FIFO Write are new (SAR 34840).	2-72
	The first paragraph of the "Offset" section was removed; it was intended to be replaced by the paragraph following it (SAR 22647).	2-95
	IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions (SAR 39813).	2-164
	The drive strength, IOL, and IOH for 3.3 V GTL and 2.5 V GTL were changed from 25 mA to 20 mA in the following tables (SAR 37373):	
	Table 2-86 Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions,	2-164
	Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings	2-167
	Table 2-96 • I/O Output Buffer Maximum Resistances 1	2-169
	Table 2-138 • Minimum and Maximum DC Input and Output Levels	2-199
	Table 2-141 • Minimum and Maximum DC Input and Output Levels	2-200
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34800): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-181
	Corrected the inadvertent error in maximum values for LVPECL VIH and VIL and revised them to "3.6" in Table 2-171 • Minimum and Maximum DC Input and Output Levels, making these consistent with Table 3-1 • Absolute Maximum Ratings, and Table 3-4 • Overshoot and Undershoot Limits 1 (SAR 37687).	2-211
	The maximum frequency for global clock parameter was removed from Table 2-5 • AFS1500 Global Resource Timing through Table 2-8 • AFS090 Global Resource Timing because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36955).	2-16 to 2-17
Revision 2 (March 2012)	The phrase "without debug" was removed from the "Soft ARM Cortex-M1 Fusion Devices (M1)" section (SAR 21390).	I
	The "In-System Programming (ISP) and Security" section, "Security" section, "Flash Advantages" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34679).	l, 1-2, 2-228
	The Y security option and Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34721).	III
	The "Specifying I/O States During Programming" section is new (SAR 34693).	1-9
	The following information was added before Figure 2-17 • XTLOSC Macro:	2-20
	In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating (SAR 24119).	
	Table 2-12 • Fusion CCC/PLL Specification was updated. A note was added indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34814).	2-28