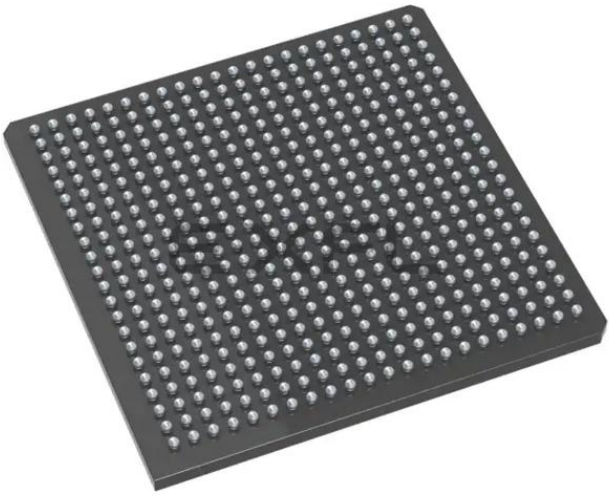
Microchip Technology - M1AFS600-1FG484 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-1fg484

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, hardwired together (Figure 2-20).

The CLKINT macro provides a global buffer function driven by the FPGA core.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by Fusion devices. The available CLKBUF macros are described in the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide*.

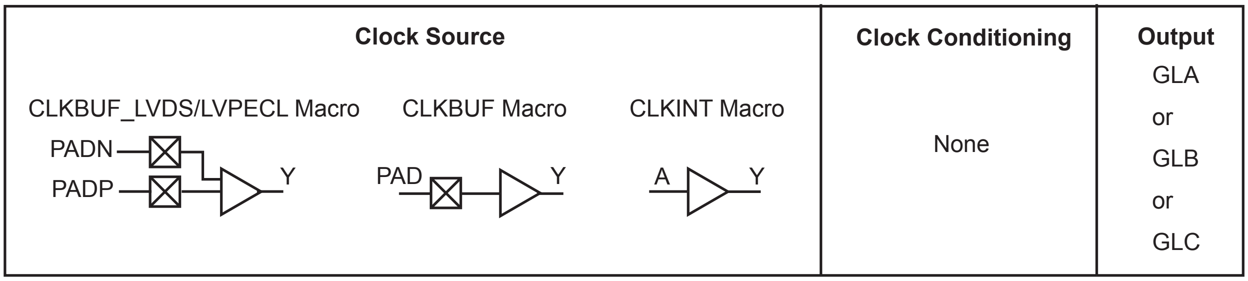

Figure 2-20 **• Global Buffers with No Programmable Delay**

Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21 on page 2-25). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide.*

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero SoC and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

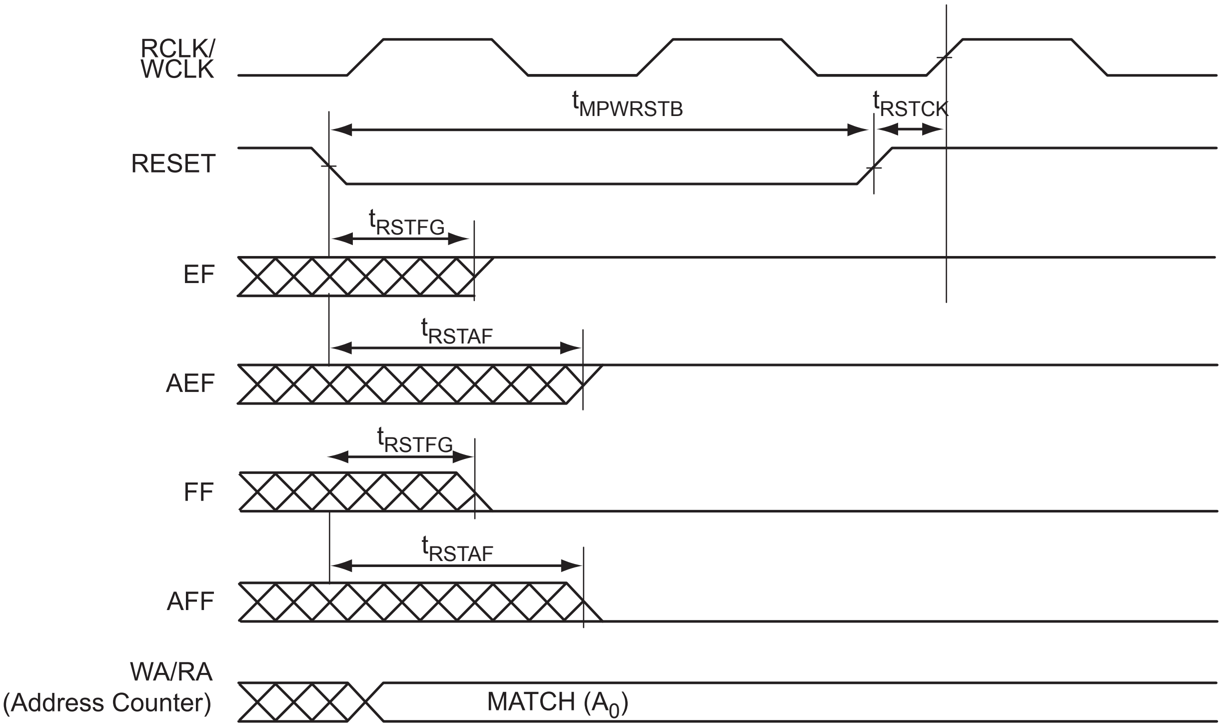

Figure 2-59 • **FIFO Reset**

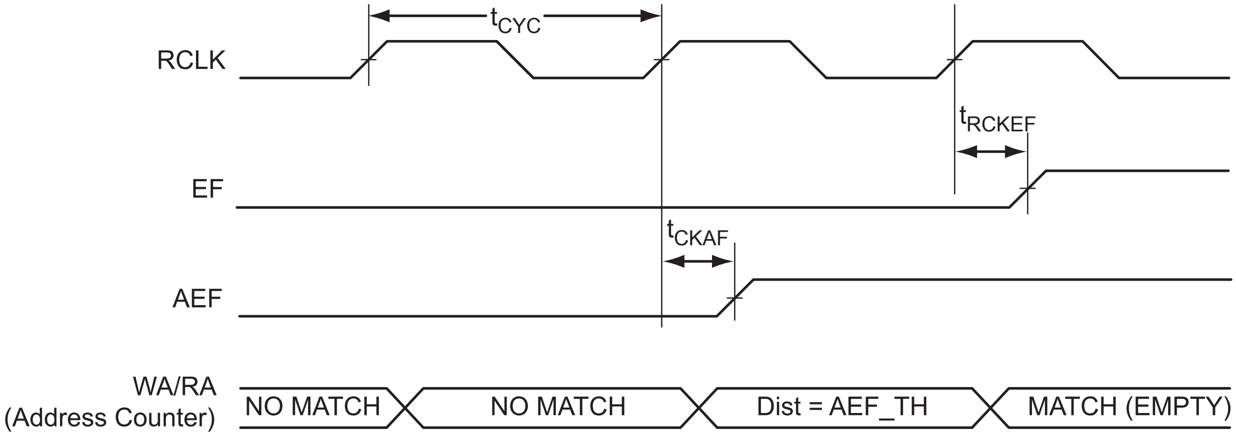

Figure 2-60 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

INL – Integral Non-Linearity

INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the end points of the transfer function (Figure 2-85).

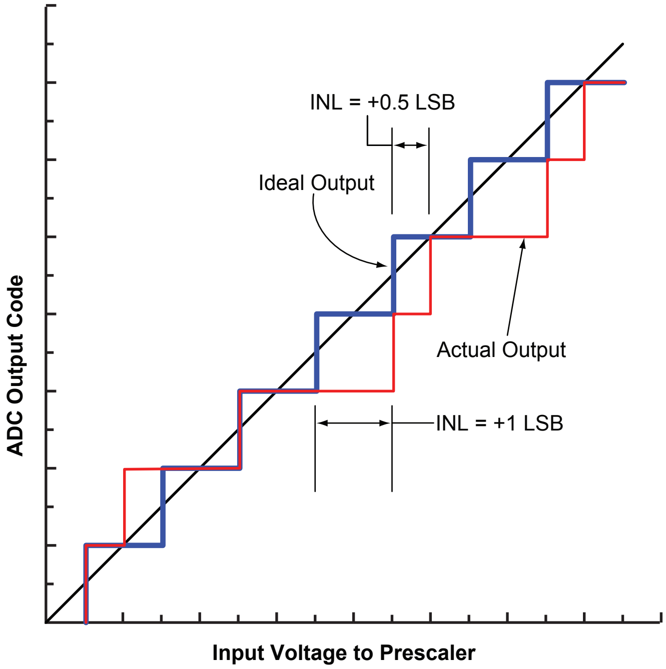

***Figure 2-85* • Integral Non-Linearity (INL)**

LSB – Least Significant Bit

In a binary number, the LSB is the least weighted bit in the group. Typically, the LSB is the furthest right bit. For an ADC, the weight of an LSB equals the full-scale voltage range of the converter divided by 2^N, where N is the converter's resolution.

EQ 13 shows the calculation for a 10-bit ADC with a unipolar full-scale voltage of 2.56 V:

$$1 \text{ LSB} = (2.56 \text{ V} / 2^{10}) = 2.5 \text{ mV}$$

EQ 13

No Missing Codes

An ADC has no missing codes if it produces all possible digital codes in response to a ramp signal applied to the analog input.

Table 2-81 **• Fusion Pro I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: Table 2-78 on page 2-152 Table 2-79 on page 2-152 Table 2-80 on page 2-152	Refer to the following tables for more information: Table 2-78 on page 2-152 Table 2-79 on page 2-152 Table 2-80 on page 2-152	Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5/5.0 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.8 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.5 V			Off	None	35 pF	–	Off	0	Off
PCI (3.3 V)			Off	None	10 pF	–	Off	0	Off
PCI-X (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (2.5 V)			Off	None	10 pF	–	Off	0	Off
GTL (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL (2.5 V)			Off	None	10 pF	–	Off	0	Off
HSTL Class I			Off	None	20 pF	–	Off	0	Off
HSTL Class II			Off	None	20 pF	–	Off	0	Off
SSTL2 Class I and II			Off	None	30 pF	–	Off	0	Off
SSTL3 Class I and II			Off	None	30 pF	–	Off	0	Off
LVDS, BLVDS, M-LVDS			Off	None	0 pF	–	Off	0	Off
LVPECL			Off	None	0 pF	–	Off	0	Off

***Table 2-82* • Advanced I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: Table 2-78 on page 2-152 Table 2-79 on page 2-152 Table 2-80 on page 2-152	Refer to the following tables for more information: Table 2-78 on page 2-152 Table 2-79 on page 2-152 Table 2-80 on page 2-152	Off	None	35 pF	–
LVCMOS 2.5 V			Off	None	35 pF	–
LVCMOS 2.5/5.0 V			Off	None	35 pF	–
LVCMOS 1.8 V			Off	None	35 pF	–
LVCMOS 1.5 V			Off	None	35 pF	–
PCI (3.3 V)			Off	None	10 pF	–
PCI-X (3.3 V)			Off	None	10 pF	–
LVDS, BLVDS, M-LVDS			Off	None	–	–
LVPECL			Off	None	–	–

Table 2-93 • **Summary of I/O Timing Characteristics – Software Default Settings**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = I/O Standard Dependent
Applicable to Advanced I/Os

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35 pF	–	0.49	2.64	0.03	0.90	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
1.8 V LVCMOS	12 mA	High	35 pF	–	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
1.5 V LVCMOS	12 mA	High	35 pF	–	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
3.3 V PCI	Per PCI spec	High	10 pF	25 [2]	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25 [2]	0.49	2.00	0.03	0.62	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
LVDS	24 mA	High	–	–	0.49	1.37	0.03	1.20	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	24 mA	High	–	–	0.49	1.34	0.03	1.05	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Notes:

1. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-123 on page 2-197 for connectivity. This resistor is not required during normal operation.*

Table 2-94 • **Summary of I/O Timing Characteristics – Software Default Settings**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = I/O Standard Dependent
Applicable to Standard I/Os

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	8 mA	High	35 pF	–	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
2.5 V LVCMOS	8 mA	High	35pF	–	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
1.8 V LVCMOS	4 mA	High	35pF	–	0.49	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns
1.5 V LVCMOS	2 mA	High	35pF	–	0.49	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-7 for derating values.*

Table 2-98 **• I/O Short Currents IOSH/IOSL**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181

Note: *T_J = 100°C

Table 2-98 • I/O Short Currents IOSH/IOSL (continued)

	Drive Strength	IOSH (mA)*	IOSL (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109
Applicable to Standard I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16

Note: *T_J = 100°C*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-113* • 2.5 V LVCMOS High Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.51	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.45	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8 mA	Std.	0.60	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.51	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.45	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12 mA	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16 mA	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24 mA	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-132 • **1.5 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	12.33	0.04	1.42	0.43	11.79	12.33	2.45	2.32	ns
	–1	0.56	10.49	0.04	1.21	0.36	10.03	10.49	2.08	1.98	ns
	–2	0.49	9.21	0.03	1.06	0.32	8.81	9.21	1.83	1.73	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-133 • **1.5 V LVCMOS High Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	7.65	0.04	1.42	0.43	6.31	7.65	2.45	2.45	ns
	–1	0.56	6.50	0.04	1.21	0.36	5.37	6.50	2.08	2.08	ns
	–2	0.49	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-159 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

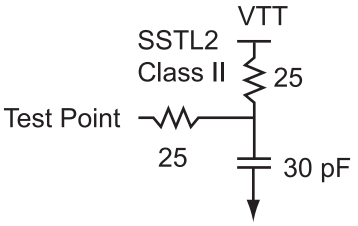

Figure 2-131 • AC Loading

Table 2-160 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-161 • SSTL 2 Class II
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	4.01	ns
–1	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	3.41	ns
–2	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	2.99	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Output DDR

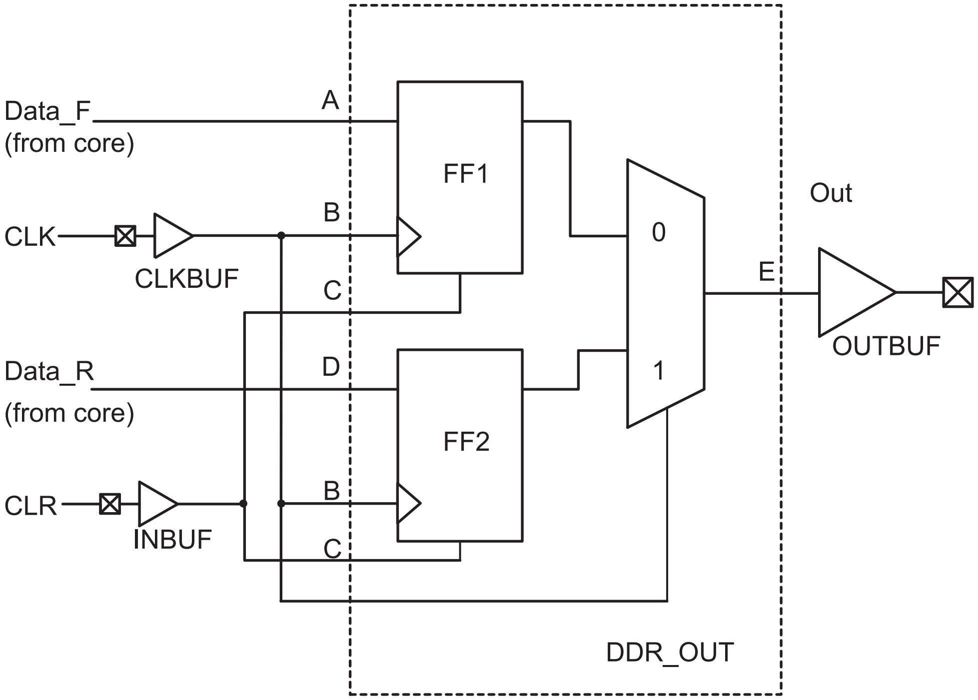

Figure 2-144 • Output DDR Timing Model

Table 2-181 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

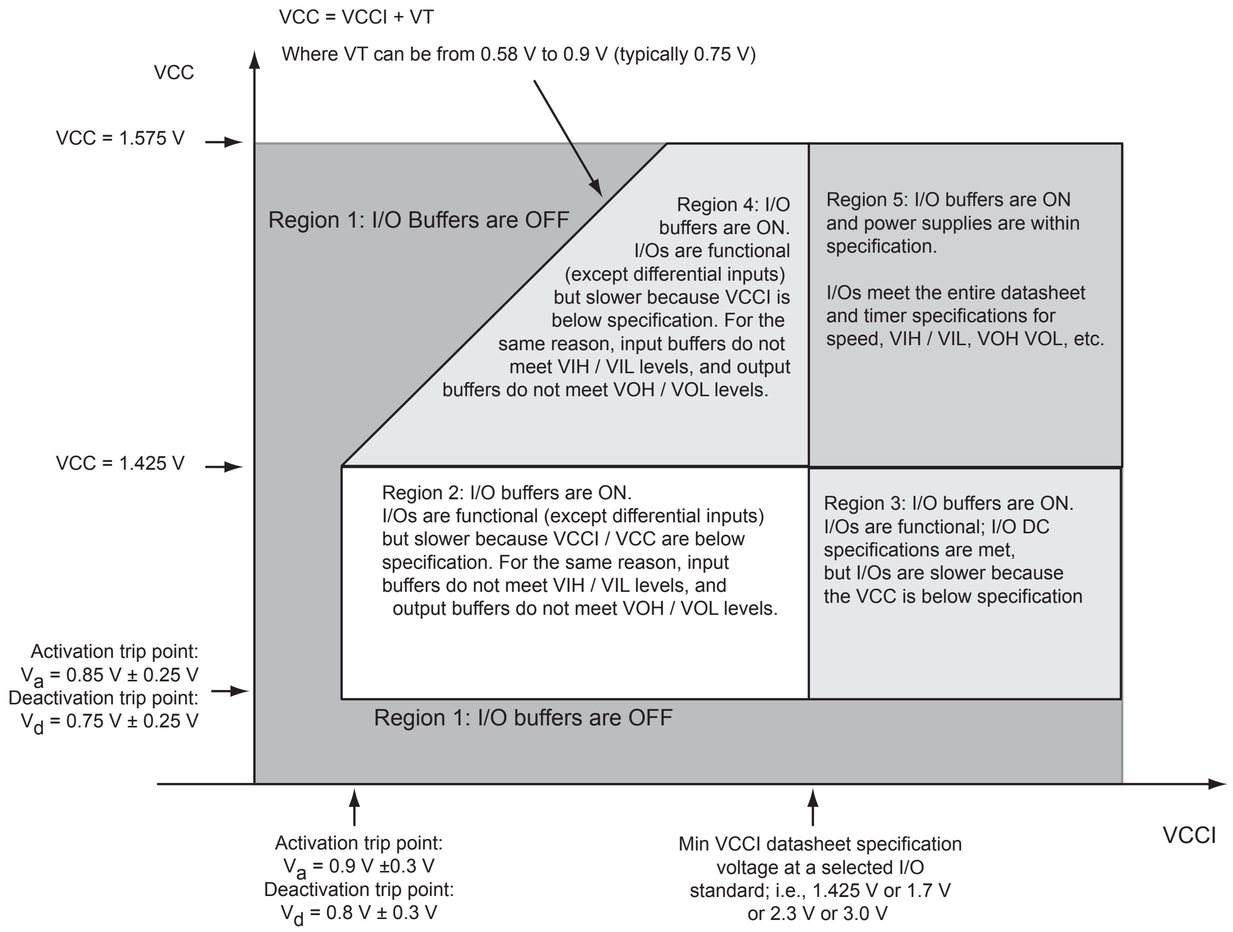

Figure 3-1 • **I/O State as a Function of VCCI and VCC Voltage Levels**

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • **AFS1500 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min.	Typ.	Max.	Unit
ICC[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		20	40	mA
			T_J = 85°C		32	65	mA
			T_J = 100°C		59	120	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
ICC33[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		10.7	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.31	2	mA
			T_J = 85°C		0.35	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.9	3.6	mA
			T_J = 85°C		2.9	4	mA
			T_J = 100°C		3.3	6	mA
		Sleep mode[6], VCC33 = 3.63 V	T_J = 25°C		17	19	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
ICCI[3]	I/O quiescent current	Operational standby[4], Standby mode, and Sleep Mode[6], VCCIx = 3.63 V	T_J = 25°C		417	649	µA
			T_J = 85°C		417	649	µA
			T_J = 100°C		417	649	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

$P_{S\text{-}CELL} = 0\ W$

$P_{C\text{-}CELL} = 0\ W$

$P_{NET} = 0\ W$

$P_{LOGIC} = 0\ W$

I/O Input and Output Buffer Contribution—$P_{I/O}$

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

$F_{CLK} = 50\ MHz$

Number of input pins used: $N_{INPUTS} = 30$

Number of output pins used: $N_{OUTPUTS} = 40$

Estimated I/O buffer toggle rate: $\alpha_2 = 0.1$ (10%)

Estimated IO buffer enable rate: $\beta_1 = 1$ (100%)

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$

$P_{INPUTS} = 30 * (0.1 / 2) * 0.01739 * 50$

$P_{INPUTS} = 1.30\ mW$

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$

$P_{OUTPUTS} = 40 * (0.1 / 2) * 1 * 0.4747 * 50$

$P_{OUTPUTS} = 47.47\ mW$

$P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$

$P_{I/O} = 1.30\ mW + 47.47\ mW$

$P_{I/O} = 48.77\ mW$

Standby Mode and Sleep Mode

$P_{INPUTS} = 0\ W$

$P_{OUTPUTS} = 0\ W$

$P_{I/O} = 0\ W$

RAM Contribution—P_{MEMORY}

Frequency of Read Clock: $F_{READ\text{-}CLOCK} = 10\ MHz$

Frequency of Write Clock: $F_{WRITE\text{-}CLOCK} = 10\ MHz$

Number of RAM blocks: $N_{BLOCKS} = 20$

Estimated RAM Read Enable Rate: $\beta_2 = 0.125$ (12.5%)

Estimated RAM Write Enable Rate: $\beta_3 = 0.125$ (12.5%)

Operating Mode

$P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE\text{-}CLOCK})$

$P_{MEMORY} = (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10)$

$P_{MEMORY} = 1.38\ mW$

Standby Mode and Sleep Mode

$P_{MEMORY} = 0\ W$

PLL/CCC Contribution—P_{PLL}

PLL is not used in this application.

P_{PLL} = 0 W

Nonvolatile Memory—P_{NVM}

Nonvolatile memory is not used in this application.

P_{NVM} = 0 W

Crystal Oscillator—$P_{XTL\text{-}OSC}$

The application utilizes standby mode. The crystal oscillator is assumed to be active.

Operating Mode

$P_{XTL\text{-}OSC}$ = PAC18

$P_{XTL\text{-}OSC}$ = 0.63 mW

Standby Mode

$P_{XTL\text{-}OSC}$ = PAC18

$P_{XTL\text{-}OSC}$ = 0.63 mW

Sleep Mode

$P_{XTL\text{-}OSC}$ = 0 W

RC Oscillator—$P_{RC\text{-}OSC}$

Operating Mode

$P_{RC\text{-}OSC}$ = PAC19

$P_{RC\text{-}OSC}$ = 3.30 mW

Standby Mode and Sleep Mode

$P_{RC\text{-}OSC}$ = 0 W

Analog System—P_{AB}

Number of Quads used: N_{QUADS} = 4

Operating Mode

P_{AB} = PAC20

P_{AB} = 3.00 mW

Standby Mode and Sleep Mode

P_{AB} = 0 W

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

P_{DYN} = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P_{DYN} = 143.06 mW

Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

P_{DYN} = 0.63 mW

Sleep Mode

P_{DYN} = 0 W

QN108	
Pin Number	**AFS090 Function**
A1	NC
A2	GNDQ
A3	GAA2/IO52PDB3V0
A4	GND
A5	GFA1/IO47PDB3V0
A6	GEB1/IO45PDB3V0
A7	VCCOSC
A8	XTAL2
A9	GEA1/IO44PPB3V0
A10	GEA0/IO44NPB3V0
A11	GEB2/IO42PDB3V0
A12	VCCNVM
A13	VCC15A
A14	PCAP
A15	NC
A16	GNDA
A17	AV0
A18	AG0
A19	ATRTN0
A20	AT1
A21	AC1
A22	AV2
A23	AG2
A24	AT2
A25	AT3
A26	AC3
A27	GNDAQ
A28	ADCGNDREF
A29	NC
A30	GNDA
A31	PTEM
A32	GNDNVM
A33	VPUMP
A34	TCK
A35	TMS
A36	TRST
A37	GDB1/IO39PSB1V0
A38	GDC1/IO38PDB1V0
A39	GND
A40	GCB1/IO35PDB1V0
A41	GCB2/IO33PDB1V0
A42	GBA2/IO31PDB1V0
A43	NC
A44	GBA1/IO30RSB0V0
A45	GBB1/IO28RSB0V0
A46	GND
A47	VCC
A48	GBC1/IO26RSB0V0
A49	IO21RSB0V0
A50	IO19RSB0V0
A51	IO09RSB0V0
A52	GAC0/IO04RSB0V0
A53	VCCIB0
A54	GND
A55	GAB0/IO02RSB0V0
A56	GAA0/IO00RSB0V0
B1	VCOMPLA
B2	VCCIB3
B3	GAB2/IO52NDB3V0
B4	VCCIB3
B5	GFA0/IO47NDB3V0
B6	GEB0/IO45NDB3V0
B7	XTAL1
B8	GNDOSC
B9	GEC2/IO43PSB3V0
B10	GEA2/IO42NDB3V0
B11	VCC
B12	GNDNVM
B13	NCAP
B14	VCC33PMP
B15	VCC33N
B16	GNDAQ
B17	AC0
B18	AT0
B19	AG1
B20	AV1
B21	AC2
B22	ATRTN1
B23	AG3
B24	AV3
B25	VCC33A
B26	VAREF
B27	PUB
B28	VCC33A
B29	PTBASE
B30	VCCNVM
B31	VCC
B32	TDI
B33	TDO
B34	VJTAG
B35	GDC0/IO38NDB1V0
B36	VCCIB1
B37	GCB0/IO35NDB1V0
B38	GCC2/IO33NDB1V0
B39	GBB2/IO31NDB1V0
B40	VCCIB1
B41	GNDQ
B42	GBA0/IO29RSB0V0
B43	VCCIB0
B44	GBB0/IO27RSB0V0
B45	GBC0/IO25RSB0V0
B46	IO20RSB0V0
B47	IO10RSB0V0
B48	GAC1/IO05RSB0V0
B49	GAB1/IO03RSB0V0
B50	VCC
B51	GAA1/IO01RSB0V0
B52	VCCPLA

FG484		
Pin Number	**AFS600 Function**	**AFS1500 Function**
B5	IO05NDB0V0	IO04NDB0V0
B6	IO05PDB0V0	IO04PDB0V0
B7	GND	GND
B8	IO10NDB0V1	IO09NDB0V1
B9	IO13PDB0V1	IO11PDB0V1
B10	GND	GND
B11	IO17NDB1V0	IO24NDB1V0
B12	IO18NDB1V0	IO26NDB1V0
B13	GND	GND
B14	IO21NDB1V0	IO31NDB1V1
B15	IO21PDB1V0	IO31PDB1V1
B16	GND	GND
B17	GBC1/IO26PDB1V1	GBC1/IO40PDB1V2
B18	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B19	GND	GND
B20	VCCPLB	VCCPLB
B21	GND	GND
B22	VCC	NC
C1	IO82PDB4V0	IO121PDB4V0
C2	NC	IO122PSB4V0
C3	IO00NDB0V0	IO00NDB0V0
C4	IO00PDB0V0	IO00PDB0V0
C5	VCCIB0	VCCIB0
C6	IO06NDB0V0	IO05NDB0V1
C7	IO06PDB0V0	IO05PDB0V1
C8	VCCIB0	VCCIB0
C9	IO13NDB0V1	IO11NDB0V1
C10	IO11PDB0V1	IO14PDB0V2
C11	VCCIB0	VCCIB0
C12	VCCIB1	VCCIB1
C13	IO20NDB1V0	IO29NDB1V1
C14	IO20PDB1V0	IO29PDB1V1
C15	VCCIB1	VCCIB1
C16	IO25NDB1V1	IO37NDB1V2
C17	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2
C18	VCCIB1	VCCIB1
C19	VCOMPLB	VCOMPLB
C20	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
C21	NC	IO48PSB2V0
C22	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D1	IO82NDB4V0	IO121NDB4V0
D2	GND	GND
D3	IO83NDB4V0	IO123NDB4V0
D4	GAC2/IO83PDB4V0	GAC2/IO123PDB4V0
D5	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D6	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0
D8	IO09NDB0V1	IO10NDB0V1
D9	IO09PDB0V1	IO10PDB0V1
D10	IO11NDB0V1	IO14NDB0V2
D11	IO16NDB1V0	IO23NDB1V0
D12	IO16PDB1V0	IO23PDB1V0
D13	NC	IO32NPB1V1
D14	IO23NDB1V1	IO34NDB1V1
D15	IO23PDB1V1	IO34PDB1V1
D16	IO25PDB1V1	IO37PDB1V2
D17	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
D18	VCCIB2	VCCIB2
D19	NC	IO47PPB2V0
D20	IO30NDB2V0	IO44NDB2V0
D21	GND	GND
D22	IO31NDB2V0	IO45NDB2V0
E1	IO81NDB4V0	IO120NDB4V0
E2	IO81PDB4V0	IO120PDB4V0
E3	VCCIB4	VCCIB4
E4	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
E5	IO85NDB4V0	IO125NDB4V0
E6	GND	GND
E7	VCCIB0	VCCIB0
E8	NC	IO08NDB0V1

FG676	
Pin Number	**AFS1500 Function**
W25	NC
W26	GND
Y1	NC
Y2	NC
Y3	GEB1/IO89PDB4V0
Y4	GEB0/IO89NDB4V0
Y5	VCCIB4
Y6	GEA1/IO88PDB4V0
Y7	GEA0/IO88NDB4V0
Y8	GND
Y9	VCC33PMP
Y10	NC
Y11	VCC33A
Y12	AG4
Y13	AT4
Y14	ATRTN2
Y15	AT5
Y16	VCC33A
Y17	NC
Y18	VCC33A
Y19	GND
Y20	TMS
Y21	VJTAG
Y22	VCCIB2
Y23	TRST
Y24	TDO
Y25	NC
Y26	NC