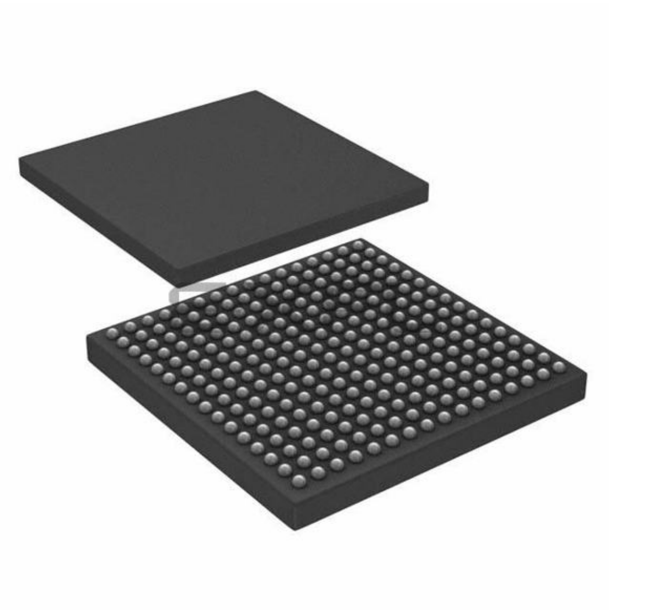

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-2fg256i

Instant On

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design.
Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.

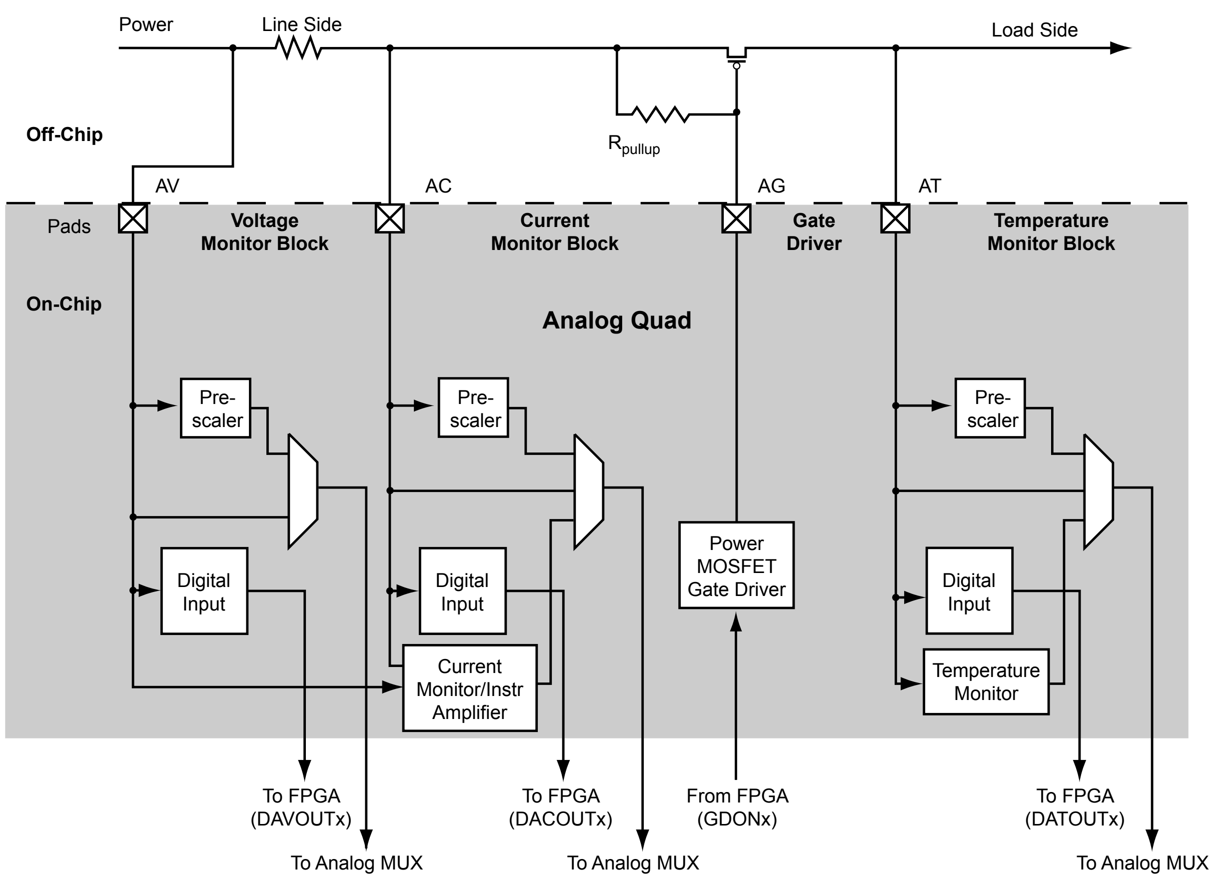

Figure 1-1 • **Analog Quad**

VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, Table 2-7, and Table 2-8 on page 2-17 present minimum and maximum global clock delays within the device Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

Table 2-5 • AFS1500 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.53	1.75	1.74	1.99	2.05	2.34	ns
t_{RCKH}	Input High Delay for Global Clock	1.53	1.79	1.75	2.04	2.05	2.40	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

Table 2-6 • AFS600 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.27	1.49	1.44	1.70	1.69	2.00	ns
t_{RCKH}	Input High Delay for Global Clock	1.26	1.54	1.44	1.75	1.69	2.06	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.36	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

The NGMUX macro is simplified to show the two clock options that have been selected by the GLMUXCFG[1:0] bits. Figure 2-25 illustrates the NGMUX macro. During design, the two clock sources are connected to CLK0 and CLK1 and are controlled by GLMUXSEL[1:0] to determine which signal is to be passed through the MUX.

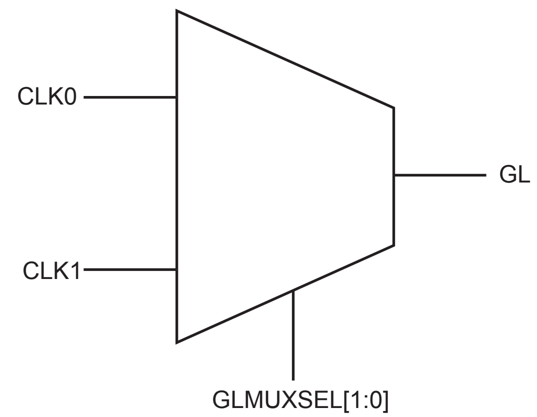

Figure 2-25 • **NGMUX Macro**

The sequence of switching between two clock sources (from CLK0 to CLK1) is as follows (Figure 2-26):

- GLMUXSEL[1:0] transitions to initiate a switch.
- GL drives one last complete CLK0 positive pulse (i.e., one rising edge followed by one falling edge).
- From that point, GL stays Low until the second rising edge of CLK1 occurs.
- At the second CLK1 rising edge, GL will begin to continuously deliver the CLK1 signal.
- Minimum t_{sw} = 0.05 ns at 25°C (typical conditions)

For examples of NGMUX operation, refer to the *Fusion FPGA Fabric User Guide*.

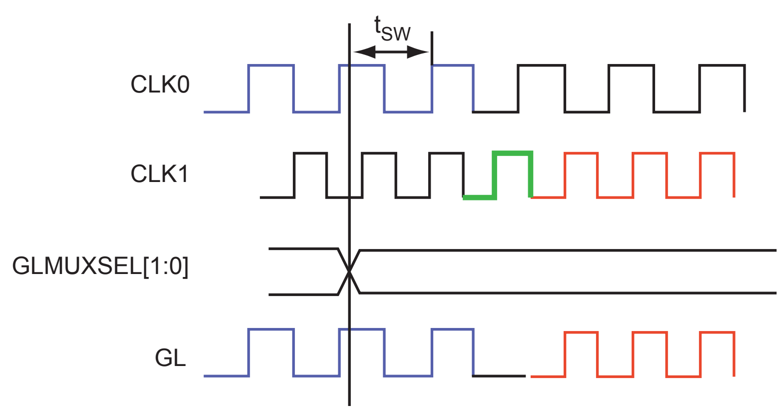

Figure 2-26 • **NGMUX Waveform**

ADC Description

The Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of features for different use models. Figure 2-80 shows a block diagram of the Fusion ADC.

- Configurable resolution: 8-bit, 10-bit, and 12-bit mode
- DNL: 0.6 LSB for 10-bit mode
- INL: 0.4 LSB for 10-bit mode
- No missing code
- Internal VAREF = 2.56 V
- Maximum Sample Rate = 600 Ksps
- Power-up calibration and dynamic calibration after every sample to compensate for temperature drift over time

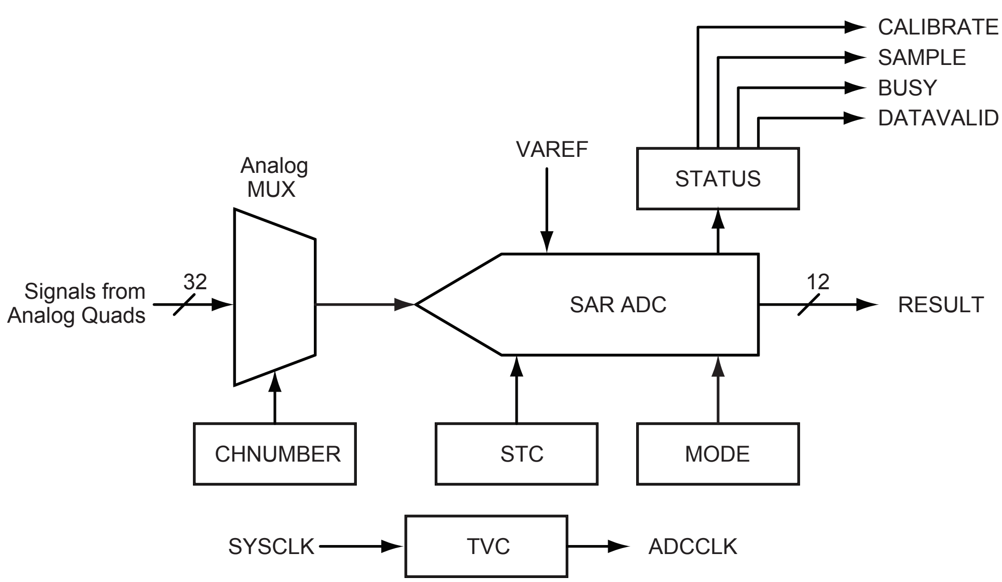

***Figure 2-80* • ADC Simplified Block Diagram**

ADC Theory of Operation

An analog-to-digital converter is used to capture discrete samples of a continuous analog voltage and provide a discrete binary representation of the signal. Analog-to-digital converters are generally characterized in three ways:

- Input voltage range
- Resolution
- Bandwidth or conversion rate

The input voltage range of an ADC is determined by its reference voltage (VREF). Fusion devices include an internal 2.56 V reference, or the user can supply an external reference of up to 3.3 V. The following examples use the internal 2.56 V reference, so the full-scale input range of the ADC is 0 to 2.56 V.

The resolution (LSB) of the ADC is a function of the number of binary bits in the converter. The ADC approximates the value of the input voltage using 2n steps, where n is the number of bits in the converter. Each step therefore represents VREF÷ 2n volts. In the case of the Fusion ADC configured for 12-bit operation, the LSB is 2.56 V / 4096 = 0.625 mV.

Finally, bandwidth is an indication of the maximum number of conversions the ADC can perform each second. The bandwidth of an ADC is constrained by its architecture and several key performance characteristics.

Timing Characteristics

Table 2-55 • Analog Configuration Multiplexer (ACM) Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{CLKQACM}$	Clock-to-Q of the ACM	19.73	22.48	26.42	ns
t_{SUDACM}	Data Setup time for the ACM	4.39	5.00	5.88	ns
t_{HDACM}	Data Hold time for the ACM	0.00	0.00	0.00	ns
t_{SUAACM}	Address Setup time for the ACM	4.73	5.38	6.33	ns
t_{HAACM}	Address Hold time for the ACM	0.00	0.00	0.00	ns
t_{SUEACM}	Enable Setup time for the ACM	3.93	4.48	5.27	ns
t_{HEACM}	Enable Hold time for the ACM	0.00	0.00	0.00	ns
$t_{MPWARACM}$	Asynchronous Reset Minimum Pulse Width for the ACM	10.00	10.00	10.00	ns
$t_{REMARACM}$	Asynchronous Reset Removal time for the ACM	12.98	14.79	17.38	ns
$t_{RECARACM}$	Asynchronous Reset Recovery time for the ACM	12.98	14.79	17.38	ns
$t_{MPWCLKACM}$	Clock Minimum Pulse Width for the ACM	45.00	45.00	45.00	ns
$t_{FMAXCLKACM}$	lock Maximum Frequency for the ACM	10.00	10.00	10.00	MHz

Double Data Rate (DDR) Support

Fusion Pro I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-101. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on Fusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-102 on page 2-140. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the application note *Using DDR for Fusion Devices* for more information.

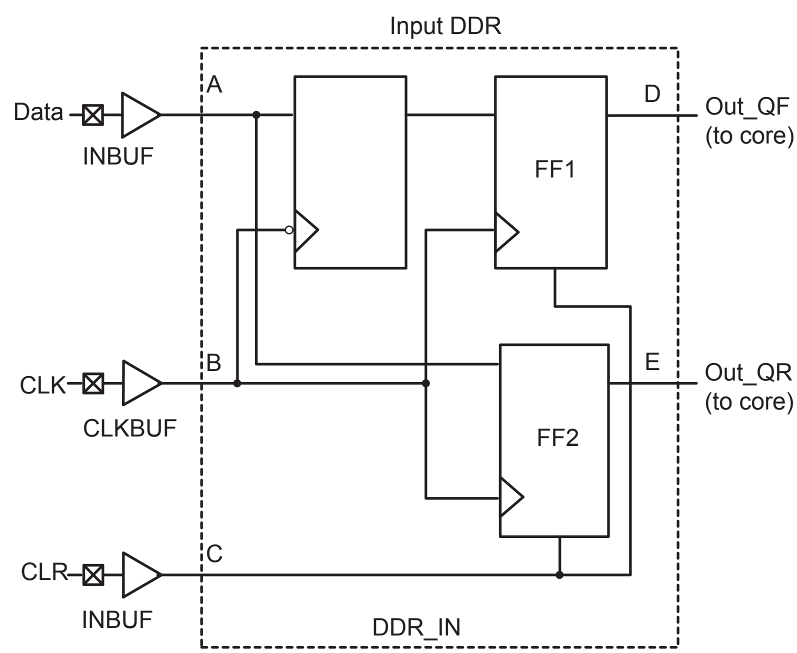

Figure 2-101 **• DDR Input Register Support in Fusion Devices**

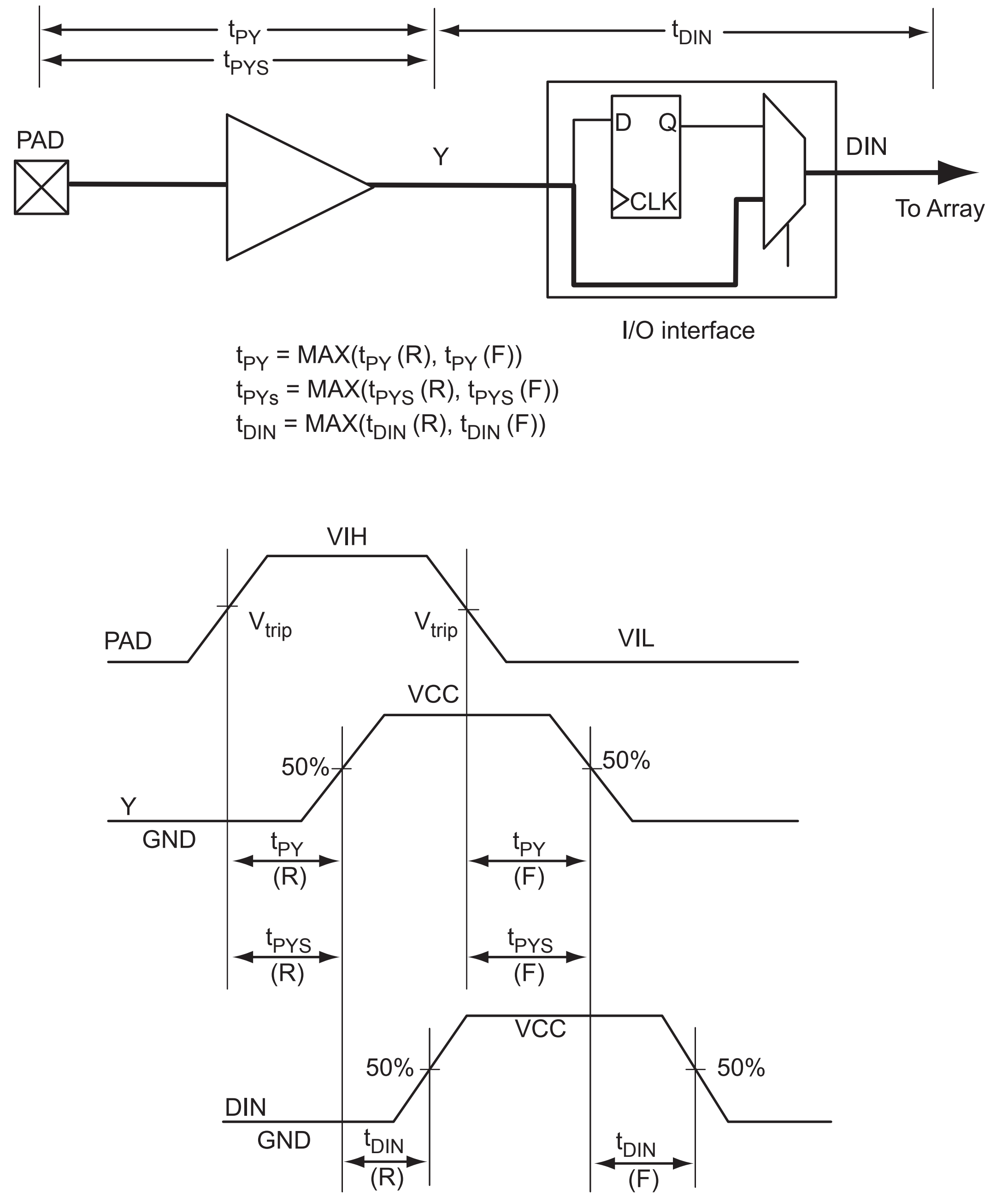

Figure 2-116 • **Input Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Pro I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output slew rate can be extracted by the IBIS models.*

Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Advanced I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 85°C junction temperature.

Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Standard I/Os

I/O Standard	Drive Strength	Slew Rate	VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	VOL Max. V	VOH Min. V	IOL mA	IOH mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Note: Currents are measured at 85°C junction temperature.

Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions
Applicable to All I/O Bank Types

DC I/O Standards	Commercial[1] IIL[3] µA	Commercial[1] IIH[4] µA	Industrial[2] IIL[3] µA	Industrial[2] IIH[4] µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_J < 85°C)*
2. *Industrial range (–40°C < T_J < 100°C)*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

***Table 2-90* • Summary of AC Measuring Points Applicable to All I/O Bank Types**

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

***Table 2-91* • I/O AC Parameter Definitions**

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-98 • I/O Short Currents IOSH/IOSL (continued)

	Drive Strength	IOSH (mA)*	IOSL (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109
Applicable to Standard I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16

Note: *T_J = 100°C*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-99* • Short Current Event Duration before Failure**

Temperature	Time Before Failure
–40°C	>20 years
0°C	>20 years
25°C	>20 years
70°C	5 years
85°C	2 years
100°C	6 months

***Table 2-100* • Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

***Table 2-101* • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/BLVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

*Note: * The maximum input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.*

Table 2-103 **• AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-104 **• 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	–1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	–2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
8 mA	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	–1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	–2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns
12 mA	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	–1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	–2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16 mA	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	–1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	–2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24 mA	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	–1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	–2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-122 **• 1.8 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.53	0.04	1.31	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	–1	0.56	13.21	0.04	1.11	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	–2[2]	0.49	11.60	0.03	0.98	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns
4 mA	Std.	0.66	10.48	0.04	1.31	0.43	10.41	10.48	3.23	2.73	12.65	12.71	ns
	–1	0.56	8.91	0.04	1.11	0.36	8.86	8.91	2.75	2.33	10.76	10.81	ns
	–2	0.49	7.82	0.03	0.98	0.32	7.77	7.82	2.41	2.04	9.44	9.49	ns
8 mA	Std.	0.66	8.05	0.04	1.31	0.43	8.20	7.84	3.54	3.27	10.43	10.08	ns
	–1	0.56	6.85	0.04	1.11	0.36	6.97	6.67	3.01	2.78	8.88	8.57	ns
	–2	0.49	6.01	0.03	0.98	0.32	6.12	5.86	2.64	2.44	7.79	7.53	ns
12 mA	Std.	0.66	7.50	0.04	1.31	0.43	7.64	7.30	3.61	3.41	9.88	9.53	ns
	–1	0.56	6.38	0.04	1.11	0.36	6.50	6.21	3.07	2.90	8.40	8.11	ns
	–2	0.49	5.60	0.03	0.98	0.32	5.71	5.45	2.69	2.55	7.38	7.12	ns
16 mA	Std.	0.66	7.29	0.04	1.31	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	–1	0.56	6.20	0.04	1.11	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	–2	0.49	5.45	0.03	0.98	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-132 • 1.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	12.33	0.04	1.42	0.43	11.79	12.33	2.45	2.32	ns
	–1	0.56	10.49	0.04	1.21	0.36	10.03	10.49	2.08	1.98	ns
	–2	0.49	9.21	0.03	1.06	0.32	8.81	9.21	1.83	1.73	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-133 • 1.5 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	7.65	0.04	1.42	0.43	6.31	7.65	2.45	2.45	ns
	–1	0.56	6.50	0.04	1.21	0.36	5.37	6.50	2.08	2.08	ns
	–2	0.49	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 3-9 • AFS600 Quiescent Supply Current Characteristics (continued)

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
IPP	Programming supply current	Non-programming mode, VPUMP = 3.63 V	T_J = 25°C		36	80	µA
			T_J = 85°C		36	80	µA
			T_J = 100°C		36	80	µA
		Standby mode[5] or Sleep mode[6], VPUMP = 0 V			0	0	µA
ICCNVM	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T_J = 25°C		22	80	µA
			T_J = 85°C		24	80	µA
			T_J = 100°C		25	80	µA
ICCPLL	1.5 V PLL quiescent current	Operational standby, VCCPLL = 1.575 V	T_J = 25°C		130	200	µA
			T_J = 85°C		130	200	µA
			T_J = 100°C		130	200	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

QN108	
Pin Number	AFS090 Function
A1	NC
A2	GNDQ
A3	GAA2/IO52PDB3V0
A4	GND
A5	GFA1/IO47PDB3V0
A6	GEB1/IO45PDB3V0
A7	VCCOSC
A8	XTAL2
A9	GEA1/IO44PPB3V0
A10	GEA0/IO44NPB3V0
A11	GEB2/IO42PDB3V0
A12	VCCNVM
A13	VCC15A
A14	PCAP
A15	NC
A16	GNDA
A17	AV0
A18	AG0
A19	ATRTN0
A20	AT1
A21	AC1
A22	AV2
A23	AG2
A24	AT2
A25	AT3
A26	AC3
A27	GNDAQ
A28	ADCGNDREF
A29	NC
A30	GNDA
A31	PTEM
A32	GNDNVM
A33	VPUMP
A34	TCK
A35	TMS
A36	TRST
A37	GDB1/IO39PSB1V0
A38	GDC1/IO38PDB1V0

QN108	
Pin Number	AFS090 Function
A39	GND
A40	GCB1/IO35PDB1V0
A41	GCB2/IO33PDB1V0
A42	GBA2/IO31PDB1V0
A43	NC
A44	GBA1/IO30RSB0V0
A45	GBB1/IO28RSB0V0
A46	GND
A47	VCC
A48	GBC1/IO26RSB0V0
A49	IO21RSB0V0
A50	IO19RSB0V0
A51	IO09RSB0V0
A52	GAC0/IO04RSB0V0
A53	VCCIB0
A54	GND
A55	GAB0/IO02RSB0V0
A56	GAA0/IO00RSB0V0
B1	VCOMPLA
B2	VCCIB3
B3	GAB2/IO52NDB3V0
B4	VCCIB3
B5	GFA0/IO47NDB3V0
B6	GEB0/IO45NDB3V0
B7	XTAL1
B8	GNDOSC
B9	GEC2/IO43PSB3V0
B10	GEA2/IO42NDB3V0
B11	VCC
B12	GNDNVM
B13	NCAP
B14	VCC33PMP
B15	VCC33N
B16	GNDAQ
B17	AC0
B18	AT0
B19	AG1
B20	AV1

QN108	
Pin Number	AFS090 Function
B21	AC2
B22	ATRTN1
B23	AG3
B24	AV3
B25	VCC33A
B26	VAREF
B27	PUB
B28	VCC33A
B29	PTBASE
B30	VCCNVM
B31	VCC
B32	TDI
B33	TDO
B34	VJTAG
B35	GDC0/IO38NDB1V0
B36	VCCIB1
B37	GCB0/IO35NDB1V0
B38	GCC2/IO33NDB1V0
B39	GBB2/IO31NDB1V0
B40	VCCIB1
B41	GNDQ
B42	GBA0/IO29RSB0V0
B43	VCCIB0
B44	GBB0/IO27RSB0V0
B45	GBC0/IO25RSB0V0
B46	IO20RSB0V0
B47	IO10RSB0V0
B48	GAC1/IO05RSB0V0
B49	GAB1/IO03RSB0V0
B50	VCC
B51	GAA1/IO01RSB0V0
B52	VCCPLA

FG676	
Pin Number	**AFS1500 Function**
W25	NC
W26	GND
Y1	NC
Y2	NC
Y3	GEB1/IO89PDB4V0
Y4	GEB0/IO89NDB4V0
Y5	VCCIB4
Y6	GEA1/IO88PDB4V0
Y7	GEA0/IO88NDB4V0
Y8	GND
Y9	VCC33PMP
Y10	NC
Y11	VCC33A
Y12	AG4
Y13	AT4
Y14	ATRTN2
Y15	AT5
Y16	VCC33A
Y17	NC
Y18	VCC33A
Y19	GND
Y20	TMS
Y21	VJTAG
Y22	VCCIB2
Y23	TRST
Y24	TDO
Y25	NC
Y26	NC

Revision	Changes	Page
Advance v1.0 (continued)	This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to V_{CC33A}.	3-8
Advance v0.9 (October 2007)	In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126	II
	In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pin: B25	3-2
	In the "180-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: B29 AFS250: B29	3-4
	In the "208-Pin PQFP" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: 102 AFS250: 102	3-8
	In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14	3-12
Advance v0.9 (continued)	In the "484-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS600: AB18 AFS1500: AB18	3-20
	In the "676-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS1500: AD20	3-28
Advance v0.8 (June 2007)	Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC.	2-20, 2-21
	Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added.	2-25
	The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator.	2-22
	Table 2-11 · Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of $I_{DYNXTAL}$ for 0.032–0.2 MHz to 0.19.	2-24
	The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR.	2-41
	The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR.	2-41