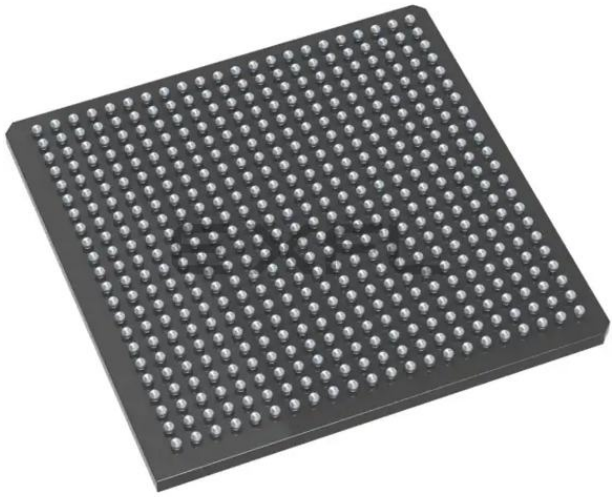


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-2fg484i

Timing Characteristics

Table 2-1 • Combinatorial Cell Propagation Delays
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	Units
INV	Y = !A	t_{PD}	0.40	0.46	0.54	ns
AND2	Y = A · B	t_{PD}	0.47	0.54	0.63	ns
NAND2	Y = !(A · B)	t_{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t_{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t_{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.70	0.79	0.93	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.58	0.68	ns
AND3	Y = A · B · C	t_{PD}	0.56	0.64	0.75	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library (Figure 2-5). For more details, refer to the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide*.

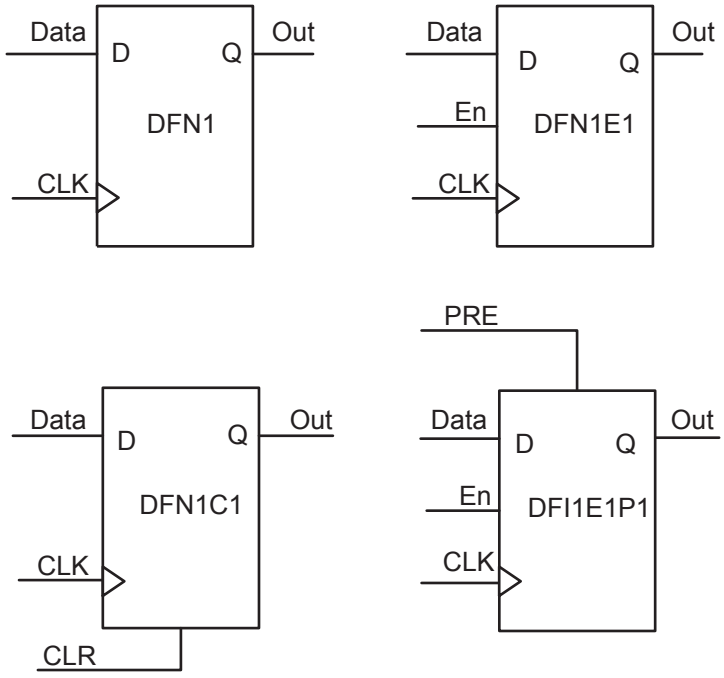


Figure 2-5 • Sample of Sequential Cells

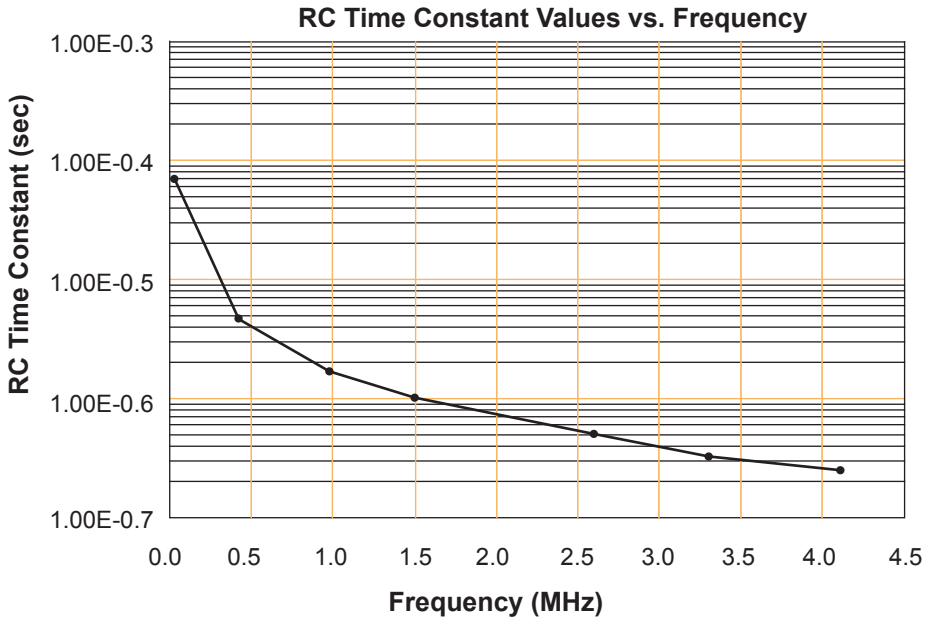


Figure 2-18 • **Crystal Oscillator: RC Time Constant Values vs. Frequency (typical)**

Table 2-10 • **XTLOSC Signals Descriptions**

Signal Name	Width	Direction	Function		
XTL_EN*	1		Enables the crystal. Active high.		
XTL_MODE*	2		Settings for the crystal clock for different frequency.		
			Value	**Modes**	**Frequency Range**
			b'00	RC network	32 KHz to 4 MHz
			b'01	Low gain	32 to 200 KHz
			b'10	Medium gain	0.20 to 2.0 MHz
			b'11	High gain	2.0 to 20.0 MHz
SELMODE	1	IN	Selects the source of XTL_MODE and also enables the XTL_EN. Connect from RTCXTLSEL from AB.		
			0	For normal operation or sleep mode, XTL_EN depends on FPGA_EN, XTL_MODE depends on MODE	
			1	For Standby mode, XTL_EN is enabled, XTL_MODE depends on RTC_MODE	
RTC_MODE[1:0]	2	IN	Settings for the crystal clock for different frequency ranges. XTL_MODE uses RTC_MODE when SELMODE is '1'.		
MODE[1:0]	2	IN	Settings for the crystal clock for different frequency ranges. XTL_MODE uses MODE when SELMODE is '0'. In Standby, MODE inputs will be 0's.		
FPGA_EN*	1	IN	0 when 1.5 V is not present for VCC 1 when 1.5 V is present for VCC		
XTL	1	IN	Crystal Clock source		
CLKOUT	1	OUT	Crystal Clock output		

*Note: *Internal signal—does not exist in macro.*

Modes of Operation

Standby Mode

Standby mode allows periodic power-up and power-down of the FPGA fabric. In standby mode, the real-time counter and crystal block are ON. The FPGA is not powered by disabling the 1.5 V voltage regulator. The 1.5 V voltage regulator can be enabled when the preset count is matched. Refer to the "Real-Time Counter (part of AB macro)" section for details. To enter standby mode, the RTC must be first configured and enabled. Then VRPSM is shut off by deasserting the VRPU signal. The 1.5 V voltage regulator is then disabled, and shuts off the 1.5 V output.

Sleep Mode

In sleep mode, the real-time counter and crystal blocks are OFF. The 1.5 V voltage regulator inside the VRPSM can only be enabled by the PUB or TRST pin. Refer to the "Voltage Regulator and Power System Monitor (VRPSM)" section on page 2-36 for details on power-up and power-down of the 1.5 V voltage regulator.

Standby and Sleep Mode Circuit Implementation

For extra power savings, VJTAG and VPUMP should be at the same voltage as VCC, floated or ground, during standby and sleep modes. Note that when VJTAG is not powered, the 1.5 V voltage regulator cannot be enabled through TRST.

VPUMP and VJTAG can be controlled through an external switch. Microsemi recommends ADG839, ADG849, or ADG841 as possible switches. Figure 2-28 shows the implementation for controlling VPUMP. The IN signal of the switch can be connected to PTBASE of the Fusion device. VJTAG can be controlled in same manner.

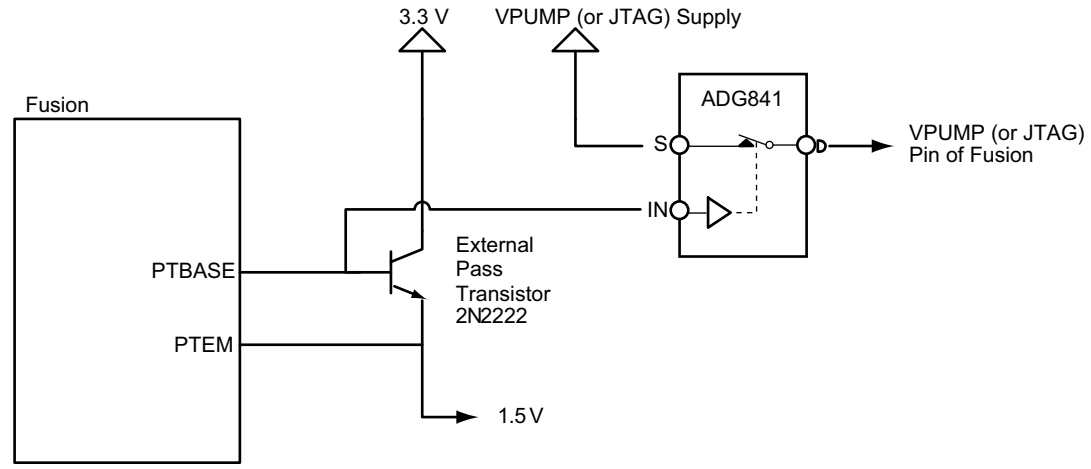


Figure 2-28 • **Implementation to Control VPUMP**

To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least t_{CMSLO} in order to discharge the previous measurement. Then CMSTB must be asserted high for at least t_{CMSET} prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is de-asserted by the AB macro. Note that the minimum sample time cannot be less than t_{CMSHI}. Figure 2-71 shows the timing diagram of CMSTB in relationship with the ADC control signals.

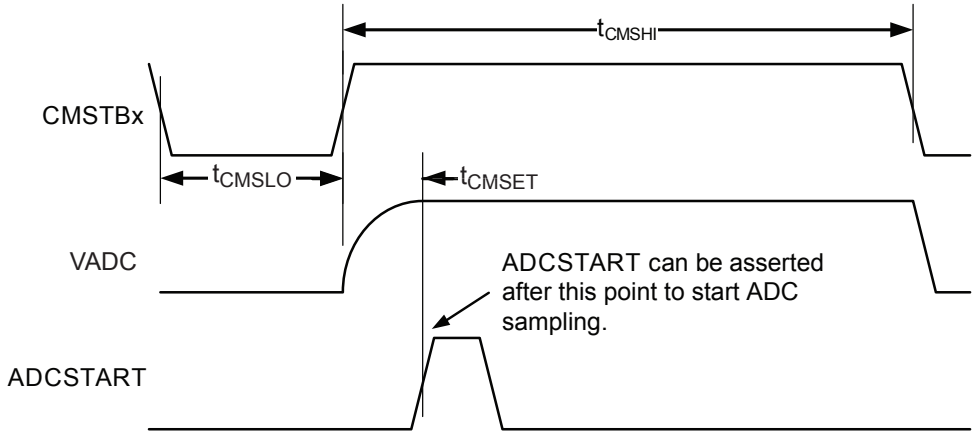


Figure 2-71 • **Timing Diagram for Current Monitor Strobe**

Figure 2-72 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050 Ω sense resistor, The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$|I| = (ADC \times V_{AREF}) / (10 \times 2^{N} \times R_{sense})$$

EQ 3

where

I is the current flowing through the sense resistor

ADC is the result from the ADC

VAREF is the Reference voltage

N is the number of bits

Rsense is the resistance of the sense resistor

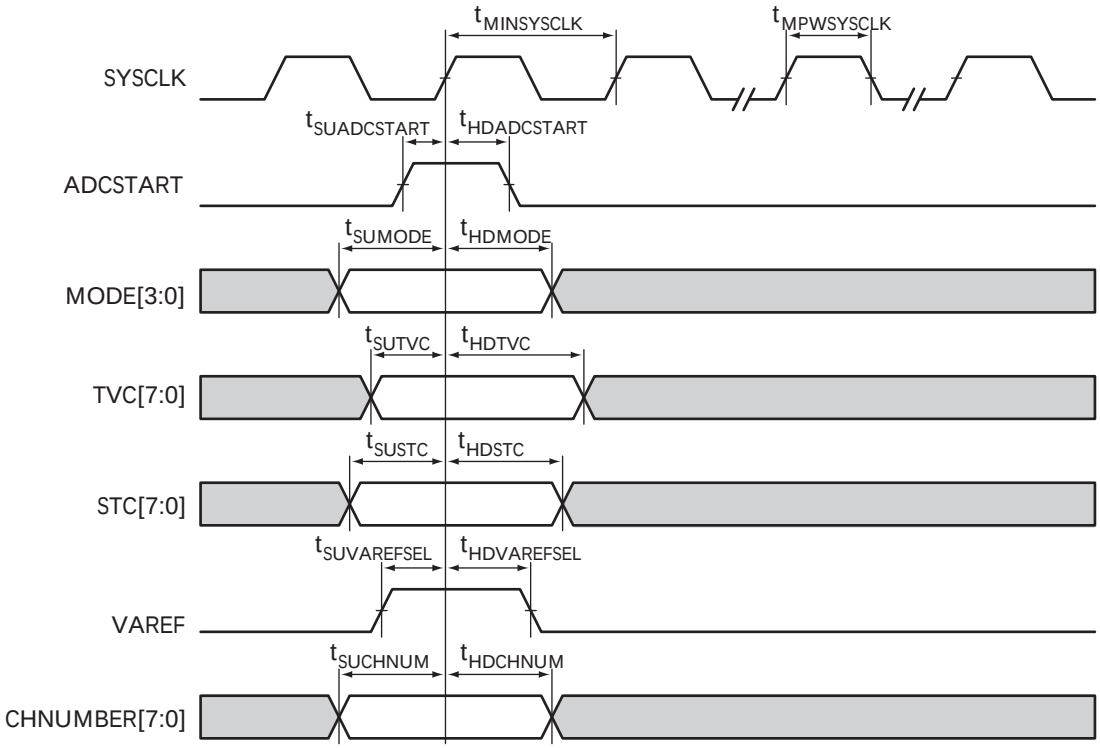
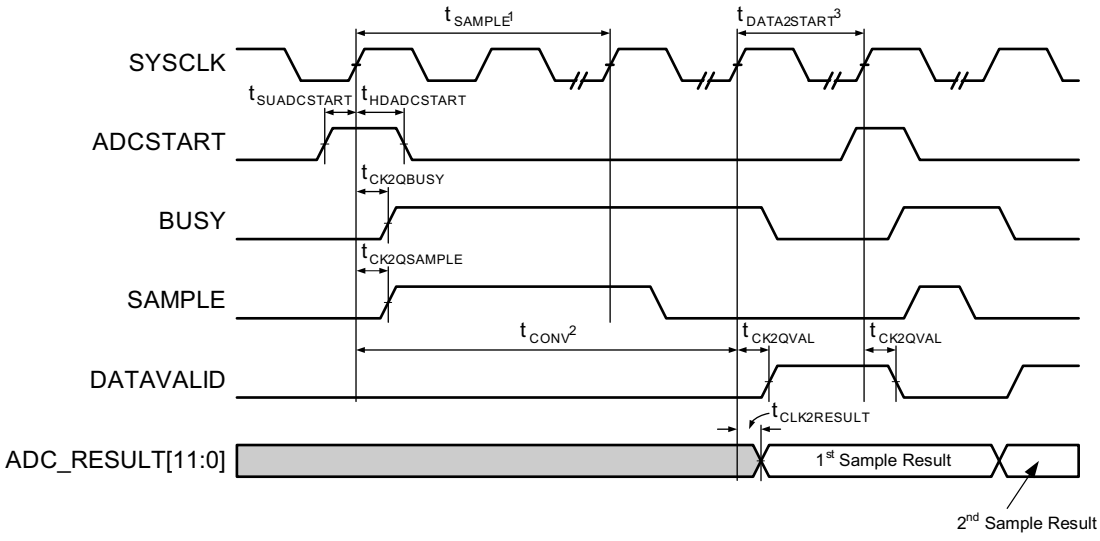


Figure 2-90 • **Input Setup Time**

Standard Conversion

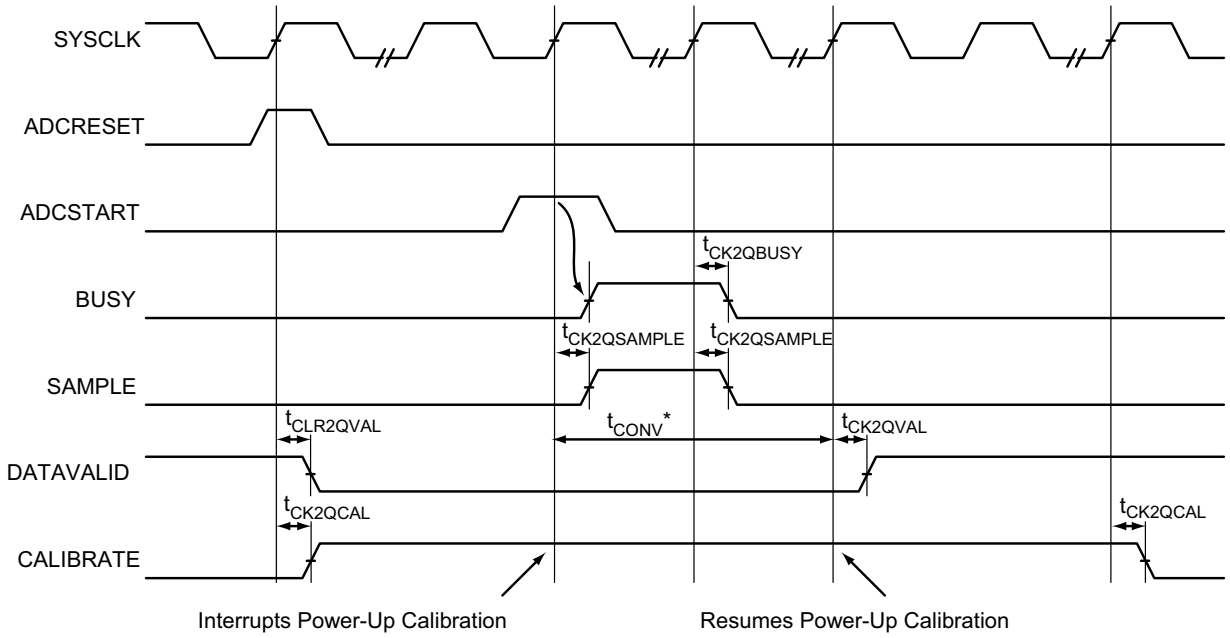


Notes:

1. *Refer to EQ 20 on page 2-109 for the calculation on the sample time, t_{SAMPLE}.*
2. *See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV}.*
3. *Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period*

Figure 2-91 • **Standard Conversion Status Signal Timing Diagram**

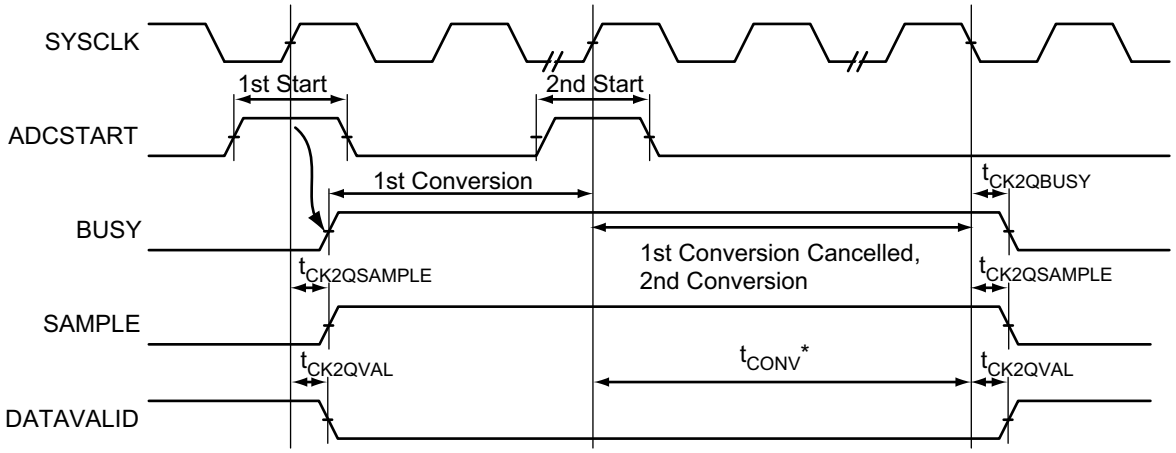
Intra-Conversion



*Note: *t_{CONV} represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV}.*

Figure 2-92 • **Intra-Conversion Timing Diagram**

Injected Conversion



*Note: *See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.*

Figure 2-93 • **Injected Conversion Timing Diagram**

Table 2-50 • ADC Characteristics in Direct Input Mode
Commercial Temperature Range Conditions, T_J = 85°C (unless noted otherwise),
Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Direct Input using Analog Pad AV, AC, AT						
VINADC	Input Voltage (Direct Input)	Refer to Table 3-2 on page 3-3				
CINADC	Input Capacitance	Channel not selected		7		pF
		Channel selected but not sampling		8		pF
		Channel selected and sampling		18		pF
ZINADC	Input Impedance	8-bit mode		2		kΩ
		10-bit mode		2		kΩ
		12-bit mode		2		kΩ
Analog Reference Voltage VAREF						
VAREF	Accuracy	T_J = 25°C	2.537	2.56	2.583	V
	Temperature Drift of Internal Reference			65		ppm / °C
	External Reference		2.527		VCC33A + 0.05	V
ADC Accuracy (using external reference) [1,2]						
DC Accuracy						
TUE	Total Unadjusted Error	8-bit mode		0.29		LSB
		10-bit mode		0.72		LSB
		12-bit mode		1.8		LSB
INL	Integral Non-Linearity	8-bit mode		0.20	0.25	LSB
		10-bit mode		0.32	0.43	LSB
		12-bit mode		1.71	1.80	LSB
DNL	Differential Non-Linearity (no missing code)	8-bit mode		0.20	0.24	LSB
		10-bit mode		0.60	0.65	LSB
		12-bit mode		2.40	2.48	LSB
	Offset Error	8-bit mode		0.01	0.17	LSB
		10-bit mode		0.05	0.20	LSB
		12-bit mode		0.20	0.40	LSB
	Gain Error	8-bit mode		0.0004	0.003	LSB
		10-bit mode		0.002	0.011	LSB
		12-bit mode		0.007	0.044	LSB
	Gain Error (with internal reference)	All modes		2		% FSR

Notes:

1. *Accuracy of the external reference is 2.56 V ± 4.6 mV.*
2. *Data is based on characterization.*
3. *The sample rate is time-shared among active analog inputs.*

Table 2-57 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

***Table 2-57* • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[2:0]	Scaling Factor, Pad to ADC Input	LSB for an 8-Bit Conversion[1] (mV)	LSB for a 10-Bit Conversion[1] (mV)	LSB for a 12-Bit Conversion[1] (mV)	Full-Scale Voltage in 10-Bit Mode[2]	Range Name
000 [3]	0.15625	64	16	4	16.368 V	16 V
001	0.3125	32	8	2	8.184 V	8 V
010 [3]	0.625	16	4	1	4.092 V	4 V
011	1.25	8	2	0.5	2.046 V	2 V
100	2.5	4	1	0.25	1.023 V	1 V
101	5.0	2	0.5	0.125	0.5115 V	0.5 V
110	10.0	1	0.25	0.0625	0.25575 V	0.25 V
111	20.0	0.5	0.125	0.03125	0.127875 V	0.125 V

Notes:

1. *LSB voltage equivalences assume VAREF = 2.56 V.*
2. *Full Scale voltage for n-bit mode: ((2^n) - 1) x (LSB for a n-bit Conversion)*
3. *These are the only valid ranges for the Temperature Monitor Block Prescaler.*

Table 2-58 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

***Table 2-58* • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[4]	Control Lines Bx[3]	ADC Connected To
0	0	Prescaler
0	1	Direct input
1	0	Current amplifier temperature monitor
1	1	Not valid

Table 2-59 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

***Table 2-59* • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[5]	Direct Input Switch
0	Off
1	On

Table 2-60 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-60* • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Control Lines Bx[6]	Input Signal Polarity
0	Positive
1	Negative

*Note: *The B3[6] signal for the AT pad should be kept at logic 0 to accept only positive voltages.*

Table 2-61 details the settings available to either power down or enable the prescaler associated with the analog inputs AV, AC, and AT.

***Table 2-61* • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[7]	Prescaler Op Amp
0	Power-down
1	Operational

Table 2-62 details the settings available to enable the Current Monitor Block associated with the AC pin.

***Table 2-62* • Current Monitor Input Switch Control Truth Table—AV (x = 0)**

Control Lines B0[4]	Current Monitor Input Switch
0	Off
1	On

Table 2-63 details the settings available to configure the drive strength of the gate drive when not in high-drive mode.

***Table 2-63* • Low-Drive Gate Driver Current Truth Table (AG)**

Control Lines B2[3]	Control Lines B2[2]	Current (µA)
0	0	1
0	1	3
1	0	10
1	1	30

Table 2-64 details the settings available to set the polarity of the gate driver (either p-channel- or n-channel-type devices).

***Table 2-64* • Gate Driver Polarity Truth Table (AG)**

Control Lines B2[6]	Gate Driver Polarity
0	Positive
1	Negative

Table 2-65 details the settings available to turn on the Gate Driver and set whether high-drive mode is on or off.

***Table 2-65* • Gate Driver Control Truth Table (AG)**

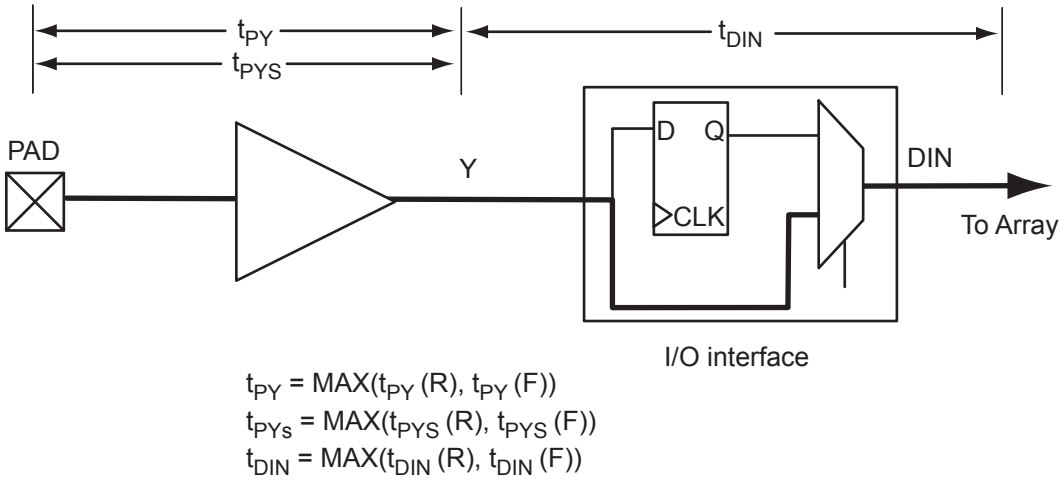
Control Lines B2[7]	GDON	Gate Driver
0	0	Off
0	1	Low drive on
1	0	Off
1	1	High drive on

Table 2-66 details the settings available to turn on and off the chip internal temperature monitor.

Note: For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

***Table 2-66* • Internal Temperature Monitor Control Truth Table**

Control Lines B2[0]	PDTMB	Chip Internal Temperature Monitor
0	0	Off
1	1	On



$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$
$t_{PYs} = MAX(t_{PYS}(R), t_{PYS}(F))$
$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$

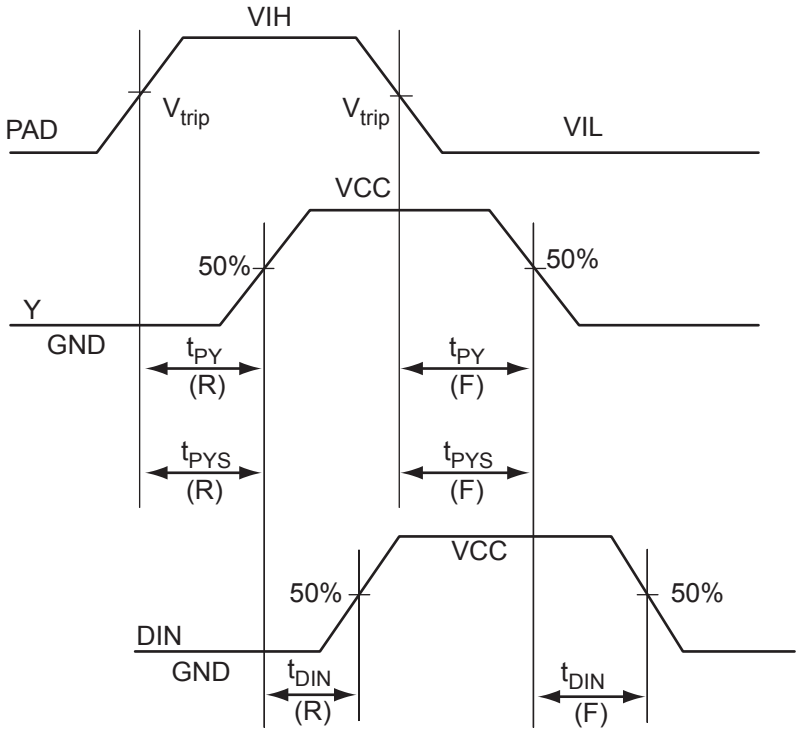


***Figure 2-116* • Input Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Pro I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output slew rate can be extracted by the IBIS models.*

Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Advanced I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 85°C junction temperature.

Table 2-106 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	10.26	0.04	1.20	0.43	10.45	8.90	2.64	2.46	12.68	11.13	ns
	–1	0.56	8.72	0.04	1.02	0.36	8.89	7.57	2.25	2.09	10.79	9.47	ns
	–2	0.49	7.66	0.03	0.90	0.32	7.80	6.64	1.98	1.83	9.47	8.31	ns
8 mA	Std.	0.66	7.27	0.04	1.20	0.43	7.41	6.28	2.98	3.04	9.65	8.52	ns
	–1	0.56	6.19	0.04	1.02	0.36	6.30	5.35	2.54	2.59	8.20	7.25	ns
	–2	0.49	5.43	0.03	0.90	0.32	5.53	4.69	2.23	2.27	7.20	6.36	ns
12 mA	Std.	0.66	5.58	0.04	1.20	0.43	5.68	4.87	3.21	3.42	7.92	7.11	ns
	–1	0.56	4.75	0.04	1.02	0.36	4.84	4.14	2.73	2.91	6.74	6.05	ns
	–2	0.49	4.17	0.03	0.90	0.32	4.24	3.64	2.39	2.55	5.91	5.31	ns
16 mA	Std.	0.66	5.21	0.04	1.20	0.43	5.30	4.56	3.26	3.51	7.54	6.80	ns
	–1	0.56	4.43	0.04	1.02	0.36	4.51	3.88	2.77	2.99	6.41	5.79	ns
	–2	0.49	3.89	0.03	0.90	0.32	3.96	3.41	2.43	2.62	5.63	5.08	ns
24 mA	Std.	0.66	4.85	0.04	1.20	0.43	4.94	4.54	3.32	3.88	7.18	6.78	ns
	–1	0.56	4.13	0.04	1.02	0.36	4.20	3.87	2.82	3.30	6.10	5.77	ns
	–2	0.49	3.62	0.03	0.90	0.32	3.69	3.39	2.48	2.90	5.36	5.06	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-125 • 1.8 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	11.21	0.04	1.20	0.43	8.53	11.21	1.99	1.21	ns
	–1	0.56	9.54	0.04	1.02	0.36	7.26	9.54	1.69	1.03	ns
	–2	0.49	8.37	0.03	0.90	0.32	6.37	8.37	1.49	0.90	ns
4 mA	Std.	0.66	6.34	0.04	1.20	0.43	5.38	6.34	2.41	2.48	ns
	–1	0.56	5.40	0.04	1.02	0.36	4.58	5.40	2.05	2.11	ns
	–2	0.49	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-144 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

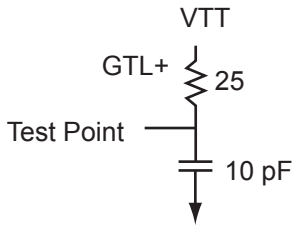


Figure 2-126 • AC Loading

Table 2-145 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-146 • 3.3 V GTL+
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.56	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.49	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-150 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	39	32	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

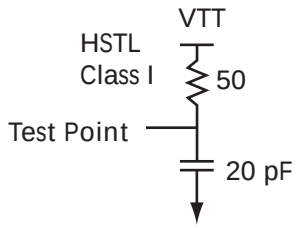


Figure 2-128 • AC Loading

Table 2-151 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-152 • HSTL Class I
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
–1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
–2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

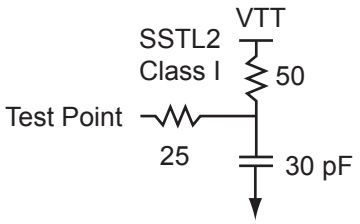


Figure 2-130 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-158 • SSTL 2 Class I
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 3-8 • **AFS1500 Quiescent Supply Current Characteristics (continued)**

Parameter	Description	Conditions	Temp.	Min.	Typ.	Max.	Unit
IJTAG	JTAG I/O quiescent current	Operational standby[4], VJTAG = 3.63 V	T_J = 25°C		80	100	µA
			T_J = 85°C		80	100	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VJTAG = 0 V			0	0	µA
IPP	Programming supply current	Non-programming mode, VPUMP = 3.63 V	T_J = 25°C		39	80	µA
			T_J = 85°C		40	80	µA
			T_J = 100°C		40	80	µA
		Standby mode[5] or Sleep mode[6], VPUMP = 0 V			0	0	µA
ICCNVM	Embedded NVM current	Reset asserted, V_{CCNVM} = 1.575 V	T_J = 25°C		50	150	µA
			T_J =85°C		50	150	µA
			T_J = 100°C		50	150	µA
ICCPLL	1.5 V PLL quiescent current	Operational standby , VCCPLL = 1.575 V	T_J = 25°C		130	200	µA
			T_J = 85°C		130	200	µA
			T_J = 100°C		130	200	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

Methodology

Total Power Consumption—P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Operating Mode

$P_{STAT} = PDC1 + (N_{NVM\text{-}BLOCKS} * PDC4) + PDC5+ (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLS} * PDC9)$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = PDC2$

Sleep Mode

$P_{STAT} = PDC3$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

Sleep Mode

$P_{DYN} = 0$ W

Global Clock Dynamic Contribution—P_{CLOCK}

Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Sleep Mode

$P_{CLOCK} = 0$ W

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

Operating Mode

Revision	Changes	Page
v2.0, Revision 1 (continued)	The data in the 2.5 V LCMOS and LVCMOS 2.5 V / 5.0 V rows were updated in Table 2-75 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities.	2-143
	In Table 2-78 • Fusion Standard I/O Standards—OUT_DRIVE Settings, LVCMOS 1.5 V, for OUT_DRIVE 2, was changed from a dash to a check mark.	2-152
	The "VCC15A Analog Power Supply (1.5 V)" definition was changed from "A 1.5 V analog power supply input should be used to provide this input" to "1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry."	2-223
	In the "VCC33PMP Analog Power Supply (3.3 V)" pin description, the following text was changed from "VCC33PMP should be powered up before or simultaneously with VCC33A" to "VCC33PMP should be powered up simultaneously with or after VCC33A."	2-223
	The "VCCOSC Oscillator Power Supply (3.3 V)" section was updated to include information about when to power the pin.	2-223
	In the "128-Bit AES Decryption" section, FIPS-192 was incorrect and changed to FIPS-197.	2-228
	The note in Table 2-84 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications was updated.	2-156
	For 1.5 V LVCMOS, the VIL and VIH parameters, 0.30 * VCCI was changed to 0.35 * VCCI and 0.70 * VCCI was changed to 0.65 * VCCI in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, and Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions. In Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, the VIH max column was updated.	2-164 to 2-165
	Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated to include notes 3 and 4. The temperature ranges were also updated in notes 1 and 2.	2-165
	The titles in Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings to Table 2-94 • Summary of I/O Timing Characteristics – Software Default Settings were updated to "VCCI = I/O Standard Dependent."	2-167 to 2-168
	Below Table 2-98 • I/O Short Currents IOSH/IOSL, the paragraph was updated to change 110°C to 100°C and three months was changed to six months.	2-172
	Table 2-99 • Short Current Event Duration before Failure was updated to remove 110°C data.	2-174
	In Table 2-101 • I/O Input Rise Time, Fall Time, and Related I/O Reliability, LVTTL/LVCMOS rows were changed from 110°C to 100°C.	2-174
	VCC33PMP was added to Table 3-1 • Absolute Maximum Ratings. In addition, conditions for AV, AC, AG, and AT were also updated.	3-1
	VCC33PMP was added to Table 3-2 • Recommended Operating Conditions1. In addition, conditions for AV, AC, AG, and AT were also updated.	3-3
	Table 3-5 • FPGA Programming, Storage, and Operating Limits was updated to include new data and the temperature ranges were changed. The notes were removed from the table.	3-5

Revision	Changes	Page
Advance v0.6 (continued)	The "Analog-to-Digital Converter Block" section was updated with the following statement: "All results are MSB justified in the ADC."	2-99
	The information about the ADCSTART signal was updated in the "ADC Description" section.	2-102
	Table 2-46 · Analog Channel Specifications was updated.	2-118
	Table 2-47 · ADC Characteristics in Direct Input Mode was updated.	2-121
	Table 2-51 • ACM Address Decode Table for Analog Quad was updated.	2-127
	In Table 2-53 • Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated.	2-130
	The "Introduction" section was updated to include information about digital inputs, outputs, and bibufs.	2-133
	In Table 2-69 • Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features: Single-ended receiver Voltage-referenced differential receiver LVDS/LVPECL differential receiver features	2-137
	The "User I/O Naming Convention" section was updated to include "V" and "z" descriptions	2-159
	The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and V_{CCI} pins within a given I/O bank.	2-185
	The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTEM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090.	3-8