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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-2fgg256

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Fusion Device Architecture Overview



Figure 1 • Fusion Device Architecture Overview (AFS600)

Package I/Os: Single-/Double-Ended (Analog)

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
ARM Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500
Pigeon Point Devices			P1AFS600 ¹	P1AFS1500 ¹
MicroBlade Devices		U1AFS250 ²	U1AFS600 ²	U1AFS1500 ²
QN108 ³	37/9 (16)			
QN180 ³	60/16 (20)	65/15 (24)		
PQ208 ⁴		93/26 (24)	95/46 (40)	
FG256	75/22 (20)	114/37 (24)	119/58 (40)	119/58 (40)
FG484			172/86 (40)	223/109 (40)
FG676				252/126 (40)
Notes:	•	1		•

1. Pigeon Point devices are only offered in FG484 and FG256.

2. MicroBlade devices are only offered in FG256.

3. Package not available.

4. Fusion devices in the same package are pin compatible with the exception of the PQ208 package (AFS250 and AFS600).



1 – Fusion Device Family Overview

Introduction

The Fusion mixed signal FPGA satisfies the demand from system architects for a device that simplifies design and unleashes their creativity. As the world's first mixed signal programmable logic family, Fusion integrates mixed signal analog, flash memory, and FPGA fabric in a monolithic device. Fusion devices enable designers to quickly move from concept to completed design and then deliver feature-rich systems to market. This new technology takes advantage of the unique properties of Microsemi flash-based FPGAs, including a high-isolation, triple-well process and the ability to support high-voltage transistors to meet the demanding requirements of mixed signal system design.

Fusion mixed signal FPGAs bring the benefits of programmable logic to many application areas, including power management, smart battery charging, clock generation and management, and motor control. Until now, these applications have only been implemented with costly and space-consuming discrete analog components or mixed signal ASIC solutions. Fusion mixed signal FPGAs present new capabilities for system development by allowing designers to integrate a wide range of functionality into a single device, while at the same time offering the flexibility of upgrades late in the manufacturing process or after the device is in the field. Fusion devices provide an excellent alternative to costly and

time-consuming mixed signal ASIC designs. In addition, when used in conjunction with the ARM Cortex-M1 processor, Fusion technology represents the definitive mixed signal FPGA platform.

Flash-based Fusion devices are Instant On. As soon as system power is applied and within normal operating specifications, Fusion devices are working. Fusion devices have a 128-bit flash-based lock and industry-leading AES decryption, used to secure programmed intellectual property (IP) and configuration data. Fusion devices are the most comprehensive single-chip analog and digital programmable logic solution available today.

To support this new ground-breaking technology, Microsemi has developed a series of major tool innovations to help maximize designer productivity. Implemented as extensions to the popular Microsemi Libero[®] System-on-Chip (SoC) software, these new tools allow designers to easily instantiate and configure peripherals within a design, establish links between peripherals, create or import building blocks or reference designs, and perform hardware verification. This tool suite will also add comprehensive hardware/software debug capability as well as a suite of utilities to simplify development of embedded soft-processor-based solutions.

General Description

The Fusion family, based on the highly successful ProASIC[®]3 and ProASIC3E flash FPGA architecture, has been designed as a high-performance, programmable, mixed signal platform. By combining an advanced flash FPGA core with flash memory blocks and analog peripherals, Fusion devices dramatically simplify system design and, as a result, dramatically reduce overall system cost and board space.

The state-of-the-art flash memory technology offers high-density integrated flash memory blocks, enabling savings in cost, power, and board area relative to external flash solutions, while providing increased flexibility and performance. The flash memory blocks and integrated analog peripherals enable true mixed-mode programmable logic designs. Two examples are using an on-chip soft processor to implement a fully functional flash MCU and using high-speed FPGA logic to offer system and power supervisory capabilities. Instant On, and capable of operating from a single 3.3 V supply, the Fusion family is ideally suited for system management and control applications.

The devices in the Fusion family are categorized by FPGA core density. Each family member contains many peripherals, including flash memory blocks, an analog-to-digital-converter (ADC), high-drive outputs, both RC and crystal oscillators, and a real-time counter (RTC). This provides the user with a high level of flexibility and integration to support a wide variety of mixed signal applications. The flash memory block capacity ranges from 2 Mbits to 8 Mbits. The integrated 12-bit ADC supports up to 30 independently configurable input channels.

Global Clocking

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 KHz to 20 MHz)
- Ceramic (500 KHz to 8 MHz)
- RC (32.768 KHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Digital I/Os with Advanced I/O Standards

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

The I/Os are organized into banks, with four or five banks per device. The configuration of these banks determines the I/O standards supported. The banks along the east and west sides of the device support the full range of I/O standards (single-ended and differential). The south bank supports the Analog Quads (analog I/O). In the family's two smaller devices, the north bank supports multiple single-ended digital I/O standards. In the family's larger devices, the north bank is divided into two banks of digital Pro I/Os, supporting a wide variety of single-ended, differential, and voltage-referenced I/O standards.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following applications:

- Single-Data-Rate (SDR) applications
- Double-Data-Rate (DDR) applications—DDR LVDS I/O for chip-to-chip communications
- Fusion banks support LVPECL, LVDS, BLVDS, and M-LVDS with 20 multi-drop points.

VersaTiles

The Fusion core consists of VersaTiles, which are also used in the successful ProASIC3 family. The Fusion VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set and optional enable

Refer to Figure 1-2 for the VersaTile configuration arrangement.





The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- · D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



Note: *This input can only be connected to the global clock distribution network.

Figure 2-2 • Fusion Core VersaTile



VersaTile Characteristics

Sample VersaTile Specifications—Combinatorial Module

The Fusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library (Figure 2-3). For more details, refer to the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.



Figure 2-3 • Sample of Combinatorial Cells



Figure 2-10 • Very-Long-Line Resources





Figure 2-21 • Fusion CCC Options: Global Buffers with Programmable Delay

Global Input Selections

Each global buffer, as well as the PLL reference clock, can be driven from one of the following (Figure 2-22):

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core



GAA[0:2]: GA represents global in the northwest corner of the device. A[0:2]: designates specific A clock source.

Notes:

- 1. Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-158 for more information.
- 2. Instantiate the routed clock source input as follows:
 - a) Connect the output of a logic element to the clock input of the PLL, CLKDLY, or CLKINT macro. b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS) in a relevant global pin location.
- 3. LVDS-based clock sources are available in the east and west banks on all Fusion devices.

Figure 2-22 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT



Table 2-16 • RTC Control/Status Register

Bit	Name	Description	Default Value
7	rtc_rst	RTC Reset	
		1 – Resets the RTC	
		0 – Deassert reset on after two ACM_CLK cycle.	
6	cntr_en	Counter Enable	0
		1 – Enables the counter; rtc_rst must be deasserted as well. First counter increments after 64 RTCCLK positive edges.	
		0 – Disables the crystal prescaler but does not reset the counter value. Counter value can only be updated when the counter is disabled.	
5	vr_en_mat	Voltage Regulator Enable on Match	0
		1 – Enables RTCMATCH and RTCPSMMATCH to output 1 when the counter value equals the Match Register value. This enables the 1.5 V voltage regulator when RTCPSMMATCH connects to the RTCPSMMATCH signal in VRPSM.	
		0 – RTCMATCH and RTCPSMMATCH output 0 at all times.	
4:3	xt_mode[1:0]	Crystal Mode	00
		Controls RTCXTLMODE[1:0]. Connects to RTC_MODE signal in XTLOSC. XTL_MODE uses this value when xtal_en is 1. See the "Crystal Oscillator" section on page 2-20 for mode configuration.	
2	rst_cnt_omat	Reset Counter on Match	0
		1 – Enables the sync clear of the counter when the counter value equals the Match Register value. The counter clears on the rising edge of the clock. If all the Match Registers are set to 0, the clear is disabled.	
		0 – Counter increments indefinitely	
1	rstb_cnt	Counter Reset, active Low	0
		0 - Resets the 40-bit counter value	
0	xtal_en	Crystal Enable	0
		Controls RTCXTLSEL. Connects to SELMODE signal in XTLOSC.	
		0 – XTLOSC enables control by FPGA_EN; xt_mode is not used. Sleep mode requires this bit to equal 0.	
		1 – Enables XTLOSC, XTL_MODE control by xt_mode	
		Standby mode requires this bit to be set to 1.	
		See the "Crystal Oscillator" section on page 2-20 for further details on SELMODE configuration.	



Timing Characteristics

Table 2-35 • FIFO

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ENS}	REN, WEN Setup time	1.34	1.52	1.79	ns
t _{ENH}	REN, WEN Hold time	0.00	0.00	0.00	ns
t _{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t _{вкн}	BLK Hold time	0.00	0.00	0.00	ns
t _{DS}	Input data (WD) Setup time	0.18	0.21	0.25	ns
t _{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t _{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t _{RCKEF}	RCLK High to Empty Flag Valid		1.96	2.30	ns
t _{WCKFF}	WCLK High to Full Flag Valid		1.86	2.18	ns
t _{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t _{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t _{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.13	6.98	8.20	ns
+	RESET Low to Data out Low on RD (flow-through)	0.92	1.05	1.23	ns
^I RSTBQ	RESET Low to Data out Low on RD (pipelined)	0.92	1.05	1.23	ns
t _{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t _{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t _{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t _{CYC}	Clock Cycle time	3.23	3.68	4.32	ns
F _{MAX}	Maximum Frequency for FIFO	310	272	231	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Table 2-50 • ADC Characteristics in Direct Input Mode (continued)

Commercial Temperature Range Conditions, $T_J = 85^{\circ}C$ (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Dynamic Pe	erformance					
SNR	Signal-to-Noise Ratio	8-bit mode	48.0	49.5		dB
		10-bit mode	58.0	60.0		dB
		12-bit mode	62.9	64.5		dB
SINAD	Signal-to-Noise Distortion	8-bit mode	47.6	49.5		dB
		10-bit mode	57.4	59.8		dB
		12-bit mode	62.0	64.2		dB
THD	Total Harmonic Distortion	8-bit mode		-74.4	-63.0	dBc
		10-bit mode		-78.3	-63.0	dBc
		12-bit mode		-77.9	-64.4	dBc
ENOB	Effective Number of Bits	8-bit mode	7.6	7.9		bits
		10-bit mode	9.5	9.6		bits
		12-bit mode	10.0	10.4		bits
Conversion	Rate	ŀ				
	Conversion Time	8-bit mode	1.7			μs
		10-bit mode	1.8			μs
		12-bit mode	2			μs
	Sample Rate	8-bit mode			600	Ksps
		10-bit mode			550	Ksps
		12-bit mode			500	Ksps

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.



I/O Standard	Input/Output Supply Voltage (VCCI_TYP)	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_TYP)
LVTTL/LVCMOS 3.3 V	3.30 V	-	-
LVCMOS 2.5 V	2.50 V	-	-
LVCMOS 2.5 V / 5.0 V Input	2.50 V	-	-
LVCMOS 1.8 V	1.80 V	-	-
LVCMOS 1.5 V	1.50 V	-	-
PCI 3.3 V	3.30 V	-	-
PCI-X 3.3 V	3.30 V	-	-
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS, BLVDS, M-LVDS	2.50 V	-	-
LVPECL	3.30 V	_	-

Table 2-83 • Fusion Pro I/O Supported Standards and Corresponding VREF and VTT Voltages



Table 2-105 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/Os

Drive	Speed						^τ ΕΟU							11
Strength	Grade	TDOUT	τ _{DP}	τ _{DIN}	τ _{ΡΥ}	τ _{PYS}	Т	۲ZL	τzΗ	ιLZ	τ _{HZ}	τ _{ZLS}	τ _{zhs}	Units
4 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	-1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	-2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	-1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	-2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	-1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	-2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	-1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	-2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	-1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	-2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

SSTL3 Class II		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
21 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Table 2-165 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-133 • AC Loading

Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-167 • SSTL3- Class II Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
-1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
-2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



TMS Test Mode Select

The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 2-183 and must satisfy the parallel resistance value requirement. The values in Table 2-183 correspond to the resistor recommended when a single device is used and to the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin. Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Don't Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

NCAP Negative Capacitor

Negative Capacitor is where the negative terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 μ F recommended value, is required to connect between PCAP and NCAP.

PCAP Positive Capacitor

Positive Capacitor is where the positive terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 μ F recommended value, is required to connect between PCAP and NCAP.

PUB Push Button

Push button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

PTBASE Pass Transistor Base

Pass Transistor Base is the control signal of the voltage regulator. This pin should be connected to the base of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

PTEM Pass Transistor Emitter

Pass Transistor Emitter is the feedback input of the voltage regulator.

This pin should be connected to the emitter of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

XTAL1 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.



Symbol	Parameter ²		Commercial	Industrial	Units
Τ _J	Junction temperature		0 to +85	-40 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming mode ³	3.15 to 3.45	3.15 to 3.45	V
		Operation ⁴	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VCC33PMP	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VAREF	Voltage reference for ADC		2.527 to 2.593	2.527 to 2.593	V
VCC15A ⁵	Digital power supply for the analog	system	1.425 to 1.575	1.425 to 1.575	V
VCCNVM	Embedded flash power supply		1.425 to 1.575	1.425 to 1.575	V
VCCOSC	Oscillator power supply		2.97 to 3.63	2.97 to 3.63	V
AV, AC ⁶	Unpowered, ADC reset asserted or	unconfigured	-10.5 to 12.0	-10.5 to 11.6	V
	Analog input (+16 V to +2 V presca	ller range)	-0.3 to 12.0	–0.3 to 11.6	V
	Analog input (+1 V to + 0.125 V pre	escaler range)	-0.3 to 3.6	-0.3 to 3.6	V
	Analog input (–16 V to –2 V presca	ler range)	-10.5 to 0.3	-10.5 to 0.3	V
	Analog input (–1 V to –0.125 V pres	scaler range)	-3.6 to 0.3	-3.6 to 0.3	V
	Analog input (direct input to ADC)		-0.3 to 3.6	-0.3 to 3.6	V
	Digital input		-0.3 to 12.0	–0.3 to 11.6	V
AG ⁶	Unpowered, ADC reset asserted or	unconfigured	-10.5 to 12.0	-10.5 to 11.6	V
	Low Current Mode (1 µA, 3 µA, 10	μΑ, 30 μΑ)	-0.3 to 12.0	–0.3 to 11.6	V
	Low Current Mode (–1 µA, –3 µA, -	–10 μA, –30 μA)	-10.5 to 0.3	-10.5 to 0.3	V
	High Current Mode ⁷		-10.5 to 12.0	-10.5 to 11.6	V
AT ⁶	Unpowered, ADC reset asserted or	unconfigured	-0.3 to 15.5	–0.3 to 14.5	V
	Analog input (+16 V, +4 V prescale	r range)	-0.3 to 15.5	–0.3 to 14.5	V
	Analog input (direct input to ADC)		-0.3 to 3.6	-0.3 to 3.6	V
	Digital input		-0.3 to 15.5	-0.3 to 14.5	V

Table 3-2 • Recommended Operating Conditions¹

Notes:

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-157.

- 2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
- 3. The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.
- 4. VPUMP can be left floating during normal operation (not programming mode).
- 5. Violating the V_{CC15A} recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.
- 6. The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.
- 7. The AG pad should also conform to the limits as specified in Table 2-48 on page 2-114.



Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹ (continued)

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³					
Differential									
LVDS	-	2.5	7.74	88.92					
LVPECL	_	3.3	19.54	166.52					
Applicable to Standard I/O Banks									
Single-Ended									
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	431.08					
2.5 V LVCMOS	35	2.5	-	247.36					
1.8 V LVCMOS	35	1.8	-	128.46					
1.5 V LVCMOS (JESD8-11)	35	1.5	-	89.46					

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.

2. PDC8 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.

RAM Dynamic Contribution—P_{MEMORY}

Operating Mode

 $P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE-CLOCK})$ $N_{BLOCKS} \text{ is the number of RAM blocks used in the design.}$

F_{READ-CLOCK} is the memory read clock frequency.

 β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-17 on page 3-27.

 β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-17 on page 3-27.

 $\mathsf{F}_{\mathsf{WRITE}\text{-}\mathsf{CLOCK}}$ is the memory write clock frequency.

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W

PLL/CCC Dynamic Contribution—PPLL

Operating Mode

P_{PLL} = PAC13 * F_{CLKOUT}

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Standby Mode and Sleep Mode

 $P_{PLL} = 0 W$

Nonvolatile Memory Dynamic Contribution—P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

 $P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * PAC15 * F_{READ-NVM}$ when $F_{READ-NVM} \le 33$ MHz,

 $P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * (PAC16 + PAC17 * F_{READ-NVM} \text{ when } F_{READ-NVM} > 33 \text{ MHz}$

N_{NVM-BLOCKS} is the number of NVM blocks used in the design (2 inAFS600).

 β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state). F_{READ-NVM} is the NVM read clock frequency.

Standby Mode and Sleep Mode

P_{NVM} = 0 W

Crystal Oscillator Dynamic Contribution—P_{XTL-OSC}

Operating Mode

 $P_{XTL-OSC} = PAC18$

Standby Mode

 $P_{XTL-OSC} = PAC18$

Sleep Mode

 $P_{XTL-OSC} = 0 W$

The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution (P_{AC14} * F_{CLKOUT} product) to the total PLL contribution.



 $P_{S-CELL} = 0 W$ $P_{C-CELL} = 0 W$ $P_{NET} = 0 W$ $P_{LOGIC} = 0 W$

I/O Input and Output Buffer Contribution—P_{I/O}

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

 $F_{CLK} = 50 \text{ MHz}$ Number of input pins used: N_{INPUTS} = 30 Number of output pins used: N_{OUTPUTS} = 40 Estimated I/O buffer toggle rate: α_2 = 0.1 (10%) Estimated IO buffer enable rate: β_1 = 1 (100%)

Operating Mode

$$\begin{split} \mathsf{P}_{\mathsf{INPUTS}} &= \mathsf{N}_{\mathsf{INPUTS}} * (\alpha_2 \,/\, 2) * \mathsf{PAC9} * \mathsf{F}_{\mathsf{CLK}} \\ \mathsf{P}_{\mathsf{INPUTS}} &= 30 * (0.1 \,/\, 2) * 0.01739 * 50 \\ \mathsf{P}_{\mathsf{INPUTS}} &= 1.30 \text{ mW} \end{split}$$

$$\begin{split} \mathsf{P}_{\text{OUTPUTS}} &= \mathsf{N}_{\text{OUTPUTS}} * (\alpha_2 / 2) * \beta_1 * \mathsf{PAC10} * \mathsf{F}_{\text{CLK}} \\ \mathsf{P}_{\text{OUTPUTS}} &= 40 * (0.1 / 2) * 1 * 0.4747 * 50 \\ \mathsf{P}_{\text{OUTPUTS}} &= 47.47 \text{ mW} \end{split}$$

 $P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$ $P_{I/O} = 1.30 \text{ mW} + 47.47 \text{ mW}$

P_{I/O} = 48.77 mW

Standby Mode and Sleep Mode

 $P_{INPUTS} = 0 W$

 $P_{OUTPUTS} = 0 W$ $P_{I/O} = 0 W$

RAM Contribution—P_{MEMORY}

Frequency of Read Clock: $F_{READ-CLOCK} = 10 \text{ MHz}$ Frequency of Write Clock: $F_{WRITE-CLOCK} = 10 \text{ MHz}$ Number of RAM blocks: $N_{BLOCKS} = 20$ Estimated RAM Read Enable Rate: $\beta_2 = 0.125 (12.5\%)$ Estimated RAM Write Enable Rate: $\beta_3 = 0.125 (12.5\%)$

Operating Mode

$$\begin{split} \mathsf{P}_{\mathsf{MEMORY}} &= (\mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{PAC11} * \beta_2 * \mathsf{F}_{\mathsf{READ-CLOCK}}) + (\mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{PAC12} * \beta_3 * \mathsf{F}_{\mathsf{WRITE-CLOCK}}) \\ \mathsf{P}_{\mathsf{MEMORY}} &= (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10) \\ \mathsf{P}_{\mathsf{MEMORY}} &= 1.38 \text{ mW} \end{split}$$

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W



Package Pin Assignments

FG484		FG484			
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
V3	VCCIB4	VCCIB4	W16	GNDA	GNDA
V4	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0	W17	AV9	AV9
V5	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0	W18	VCCIB2	VCCIB2
V6	GND	GND	W19	NC	IO68PPB2V0
V7	VCC33PMP	VCC33PMP	W20	ТСК	ТСК
V8	NC	NC	W21	GND	GND
V9	VCC33A	VCC33A	W22	NC	IO76PPB2V0
V10	AG4	AG4	Y1	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
V11	AT4	AT4	Y2	IO60NDB4V0	IO87NDB4V0
V12	ATRTN2	ATRTN2	Y3	GEA2/IO58PDB4V0	GEA2/IO85PDB4V0
V13	AT5	AT5	Y4	IO58NDB4V0	IO85NDB4V0
V14	VCC33A	VCC33A	Y5	NCAP	NCAP
V15	NC	NC	Y6	AC0	AC0
V16	VCC33A	VCC33A	Y7	VCC33A	VCC33A
V17	GND	GND	Y8	AC1	AC1
V18	TMS	TMS	Y9	AC2	AC2
V19	VJTAG	VJTAG	Y10	VCC33A	VCC33A
V20	VCCIB2	VCCIB2	Y11	AC3	AC3
V21	TRST	TRST	Y12	AC6	AC6
V22	TDO	TDO	Y13	VCC33A	VCC33A
W1	NC	IO93PDB4V0	Y14	AC7	AC7
W2	GND	GND	Y15	AC8	AC8
W3	NC	IO93NDB4V0	Y16	VCC33A	VCC33A
W4	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0	Y17	AC9	AC9
W5	IO59NDB4V0	IO86NDB4V0	Y18	ADCGNDREF	ADCGNDREF
W6	AV0	AV0	Y19	PTBASE	PTBASE
W7	GNDA	GNDA	Y20	GNDNVM	GNDNVM
W8	AV1	AV1	Y21	VCCNVM	VCCNVM
W9	AV2	AV2	Y22	VPUMP	VPUMP
W10	GNDA	GNDA			
W11	AV3	AV3			
W12	AV6	AV6			
W13	GNDA	GNDA			
W14	AV7	AV7			
W15	AV8	AV8			



Datasheet Information

Revision	Changes	Page	
Advance v0.8 (continued)	The voltage range in the "VPUMP Programming Supply Voltage" section was updated. The parenthetical reference to "pulled up" was removed from the statement, "VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V."		
	The "ATRTNx Temperature Monitor Return" section was updated with information about grounding and floating the pin.		
	The following text was deleted from the "VREF I/O Voltage Reference" section: (all digital I/O).		
	The "NCAP Negative Capacitor" section and "PCAP Positive Capacitor" section were updated to include information about the type of capacitor that is required to connect the two.		
	1 µF was changed to 100 pF in the "XTAL1 Crystal Oscillator Circuit Input".	2-228	
	The "Programming" section was updated to include information about V_{CCOSC} .	2-229	
	The VMV pins have now been tied internally with the V _{CCI} pins.	N/A	
	The AFS090"108-Pin QFN" table was updated.	3-2	
	The AFS090 and AFS250 devices were updated in the "108-Pin QFN" table.	3-2	
	The AFS250 device was updated in the "208-Pin PQFP" table.	3-8	
	The AFS600 device was updated in the "208-Pin PQFP" table.	3-8	
	The AFS090, AFS250, AFS600, and AFS1500 devices were updated in the "256-Pin FBGA" table.	3-12	
	The AFS600 and AFS1500 devices were updated in the "484-Pin FBGA" table.	3-20	
Advance v0.7	The AFS600 device was updated in the "676-Pin FBGA" table.	3-28	
(January 2007)	The AFS1500 digital I/O count was updated in the "Fusion Family" table.	I	
	The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double- Ended (Analog)" table.	II	
Advance v0.6 (October 2006)	The second paragraph of the "PLL Macro" section was updated to include information about POWERDOWN.	2-30	
	The description for bit 0 was updated in Table 2-17 · RTC Control/Status Register.	2-38	
	3.9 was changed to 7.8 in the "Crystal Oscillator (Xtal Osc)" section.	2-40.	
	All function descriptions in Table 2-18 · Signals for VRPSM Macro.	2-42	
	In Table 2-19 • Flash Memory Block Pin Names, the RD[31:0] description was updated.	2-43	
	The "RESET" section was updated.	2-61	
	The "RESET" section was updated.	2-64	
	Table 2-35 • FIFO was updated.	2-79	
	The VAREF function description was updated in Table 2-36 • Analog Block Pin Description.	2-82	
	The "Voltage Monitor" section was updated to include information about low power mode and sleep mode.	2-86	
	The text in the "Current Monitor" section was changed from 2 mV to 1 mV.	2-90	
	The "Gate Driver" section was updated to include information about forcing 1 V on the drain.	2-94	