# Microchip Technology - M1AFS600-2FGG256I Datasheet

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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 110592 |
| Number of I/O | 119 |
| Number of Gates | 600000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-2fgg256i |

## *Global Clocking*

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 KHz to 20 MHz)
- Ceramic (500 KHz to 8 MHz)
- RC (32.768 KHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

## *Digital I/Os with Advanced I/O Standards*

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

The I/Os are organized into banks, with four or five banks per device. The configuration of these banks determines the I/O standards supported. The banks along the east and west sides of the device support the full range of I/O standards (single-ended and differential). The south bank supports the Analog Quads (analog I/O). In the family's two smaller devices, the north bank supports multiple single-ended digital I/O standards. In the family’s larger devices, the north bank is divided into two banks of digital Pro I/Os, supporting a wide variety of single-ended, differential, and voltage-referenced I/O standards.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following applications:

- Single-Data-Rate (SDR) applications
- Double-Data-Rate (DDR) applications—DDR LVDS I/O for chip-to-chip communications
- Fusion banks support LVPECL, LVDS, BLVDS, and M-LVDS with 20 multi-drop points.

## *VersaTiles*

The Fusion core consists of VersaTiles, which are also used in the successful ProASIC3 family. The Fusion VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set and optional enable

Refer to Figure 1-2 for the VersaTile configuration arrangement.

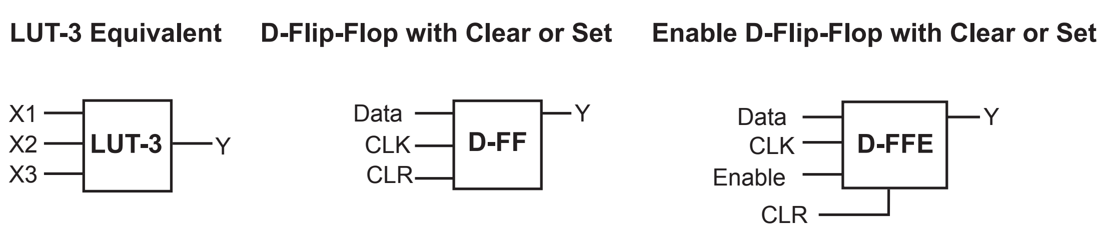



***Figure 1-2 •*** **VersaTile Configurations**

## VersaTile Characteristics

### Sample VersaTile Specifications—Combinatorial Module

The Fusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library (Figure 2-3). For more details, refer to the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.

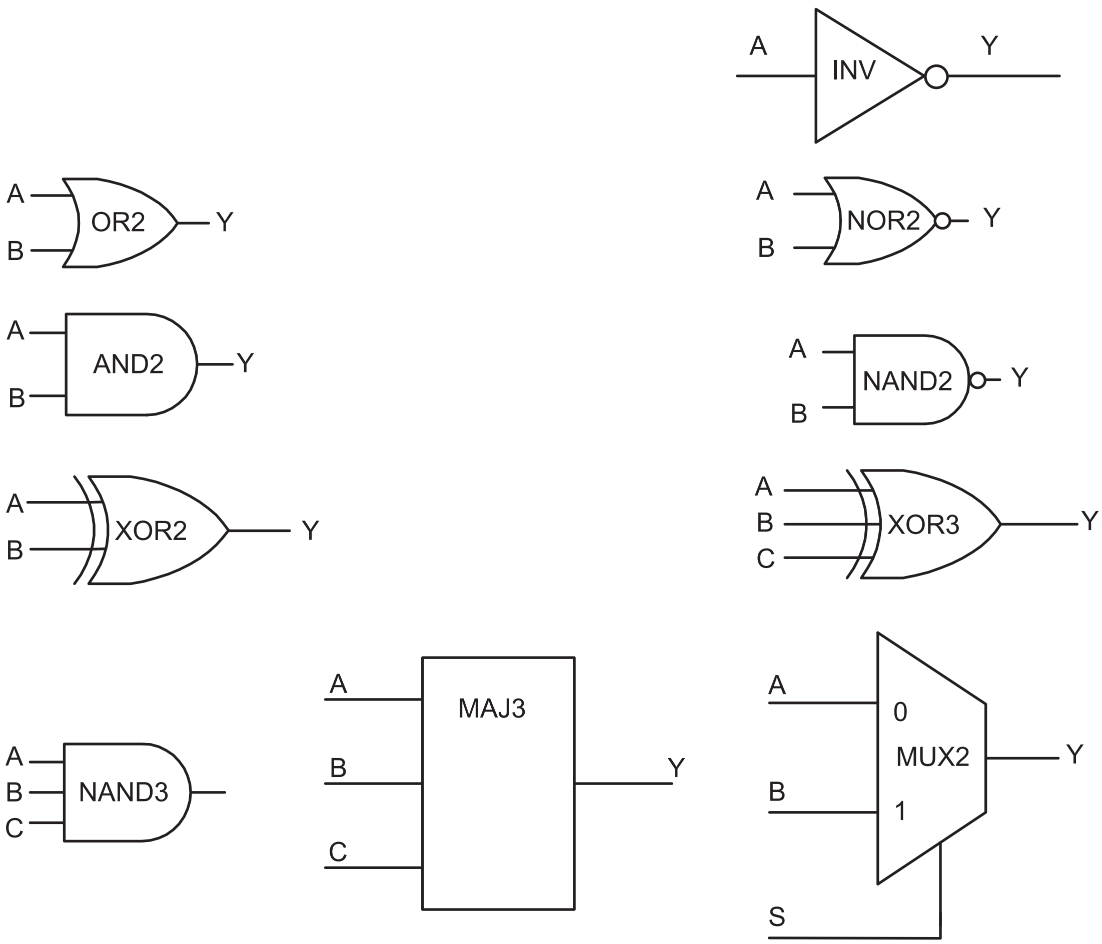



**Figure 2-3 • Sample of Combinatorial Cells**

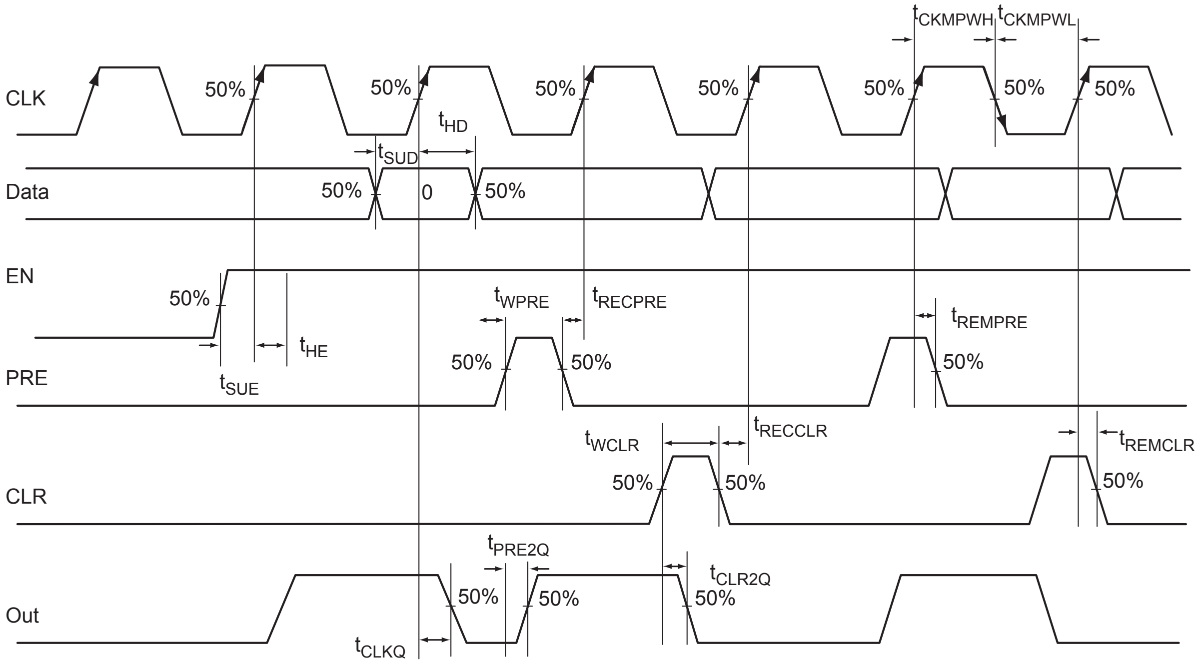



**Figure 2-6 • Sequential Timing Model and Waveforms**

### Sequential Timing Characteristics

**Table 2-2 • Register Delays**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.37 | 0.43 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.41 | 0.48 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### VersaNet Global Networks and Spine Access

The Fusion architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles on the Fusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 180 internal/external clocks (in an AFS1500 device) or other high-fanout nets in Fusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on Fusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-12 on page 2-12).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the Fusion device (the "scope" of the spine; see Figure 2-11 on page 2-11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device. For details on using spines in Fusion devices, see the application note *Using Global Resources in Actel Fusion Devices*.

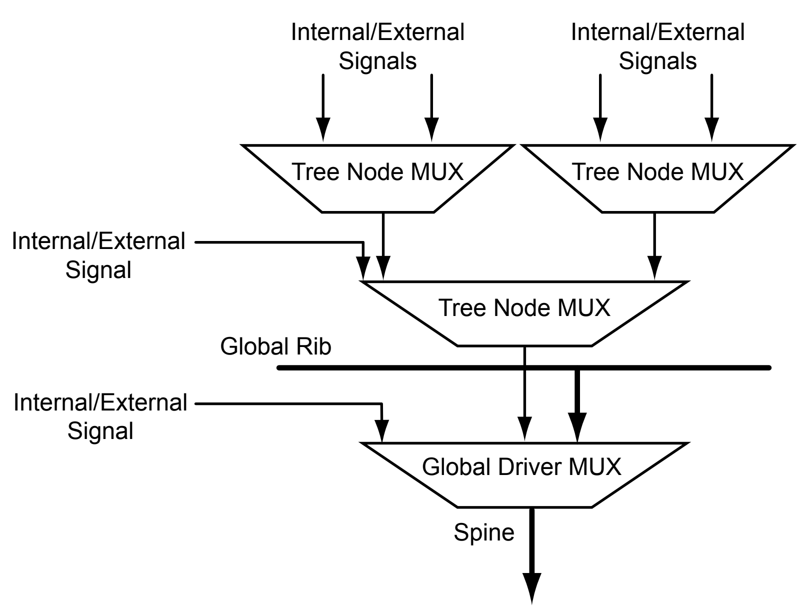



***Figure 2-13*** **• Spine-Selection MUX of Global Tree**

## Clock Conditioning Circuits

In Fusion devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, and CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and, optionally, the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-19). Refer to the "PLL Macro" section on page 2-27 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the Fusion device to permit changes of parameters (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the "UJTAG Applications in Microsemi's Low-Power Flash Devices" chapter of the *Fusion FPGA Fabric User Guide* and the "CCC and PLL Characteristics" section on page 2-28 for more information.

## Real-Time Counter (part of AB macro)

The RTC is a 40-bit loadable counter and used as the primary timekeeping element (Figure 2-29). The clock source, RTCCLK, must come from the CLKOUT signal of the crystal oscillator. The RTC can be configured to reset itself when a count value reaches the match value set in the Match Register.

The RTC is part of the Analog Block (AB) macro. The RTC is configured by the analog configuration MUX (ACM). Each address contains one byte of data. The circuitry in the RTC is powered by VCC33A, so the RTC can be used in standby mode when the 1.5 V supply is not present.

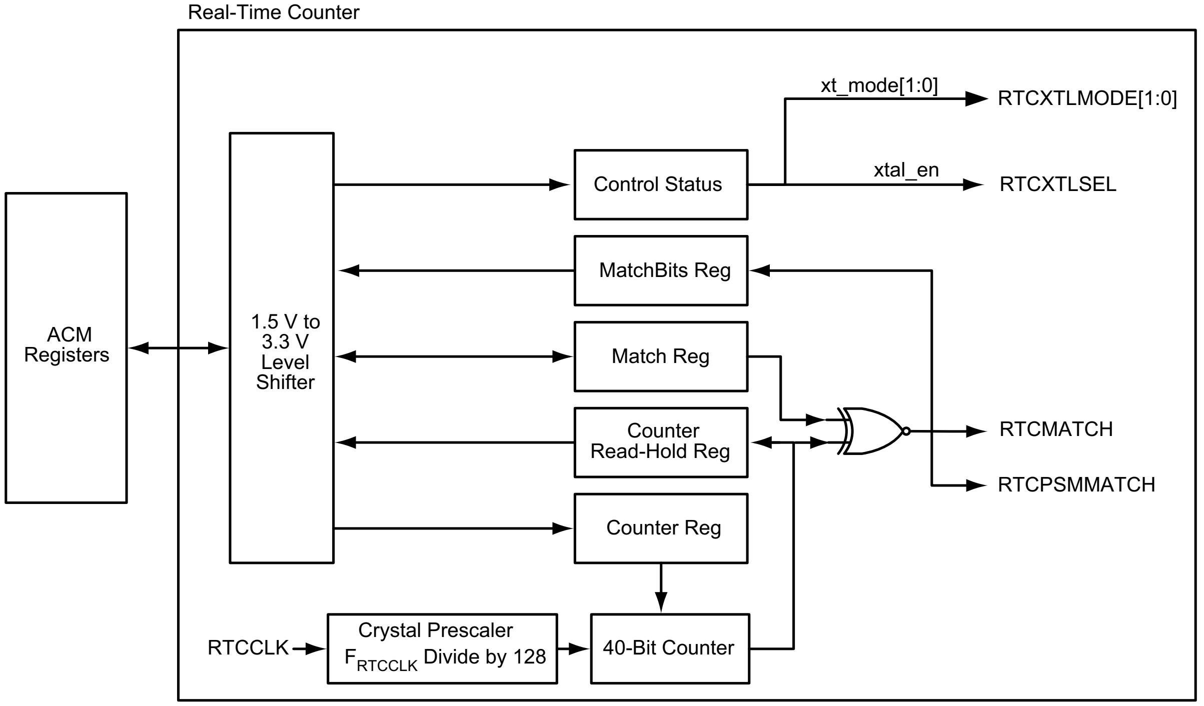



***Figure 2-29* • RTC Block Diagram**

***Table 2-14* • RTC Signal Description**

| Signal Name | Width | Direction | Function |
|---|---|---|---|
| RTCCLK | 1 | In | Must come from CLKOUT of XTLOSC. |
| RTCXTLMODE[1:0] | 2 | Out | Controlled by xt_mode in CTRL_STAT. Signal must connect to the RTC_MODE signal in XTLOSC, as shown in Figure 2-27. |
| RTCXTLSEL | 1 | Out | Controlled by xtal_en from CTRL_STAT register. Signal must connect to RTC_MODE signal in XTLOSC in Figure 2-27. |
| RTCMATCH | 1 | Out | Match signal for FPGA<br>0 – Counter value does not equal the Match Register value.<br>1 – Counter value equals the Match Register value. |
| RTCPSMMATCH | 1 | Out | Same signal as RTCMATCH. Signal must connect to RTCPSMMATCH in VRPSM, as shown in Figure 2-27. |

The 40-bit counter can be preloaded with an initial value as a starting point by the Counter Register. The count from the 40-bit counter can be read through the same set of address space. The count comes from a Read-Hold Register to avoid data changing during read. When the counter value equals the Match Register value, all Match Bits Register values will be 0xFFFFFFFFFF. The RTCMATCH and RTCPSMMATCH signals will assert. The 40-bit counter can be configured to automatically reset to 0x0000000000 when the counter value equals the Match Register value. The automatic reset does not apply if the Match Register value is 0x0000000000. The RTCCLK has a prescaler to divide the clock by 128 before it is used for the 40-bit counter. Below is an example of how to calculate the OFF time.

Data operations are performed in widths of 1 to 4 bytes. A write to a location in a page that is not already in the Page Buffer will cause the page to be read from the FB Array and stored in the Page Buffer. The block that was addressed during the write will be put into the Block Buffer, and the data written by WD will overwrite the data in the Block Buffer. After the data is written to the Block Buffer, the Block Buffer is then written to the Page Buffer to keep both buffers in sync. Subsequent writes to the same block will overwrite the Block Buffer and the Page Buffer. A write to another block in the page will cause the addressed block to be loaded from the Page Buffer, and the write will be performed as described previously.

The data width can be selected dynamically via the DATAWIDTH input bus. The truth table for the data width settings is detailed in Table 2-21. The minimum resolvable address is one 8-bit byte. For data widths greater than 8 bits, the corresponding address bits are ignored—when DATAWIDTH = 0 (2 bytes), ADDR[0] is ignored, and when DATAWIDTH = '10' or '11' (4 bytes), ADDR[1:0] are ignored. Data pins are LSB-oriented and unused WD data pins must be grounded.

***Table 2-21* • Data Width Settings**

| DATAWIDTH[1:0] | Data Width |
|---|---|
| 00 | 1 byte [7:0] |
| 01 | 2 byte [15:0] |
| 10, 11 | 4 bytes [31:0] |

## Flash Memory Block Protection

### Page Loss Protection

When the PAGELOSSPROTECT pin is set to logic 1, it prevents writes to any page other than the current page in the Page Buffer until the page is either discarded or programmed.

A write to another page while the current page is Page Loss Protected will return a STATUS of '11'.

### Overwrite Protection

Any page that is Overwrite Protected will result in the STATUS being set to '01' when an attempt is made to either write, program, or erase it. To set the Overwrite Protection state for a page, set the OVERWRITEPROTECT pin when a Program operation is undertaken. To clear the Overwrite Protect state for a given page, an Unprotect Page operation must be performed on the page, and then the page must be programmed with the OVERWRITEPROTECT pin cleared to save the new page.

### LOCKREQUEST

The LOCKREQUEST signal is used to give the user interface control over simultaneous access of the FB from both the User and JTAG interfaces. When LOCKREQUEST is asserted, the JTAG interface will hold off any access attempts until LOCKREQUEST is deasserted.

## Flash Memory Block Operations

### FB Operation Priority

The FB provides for priority of operations when multiple actions are requested simultaneously. Table 2-22 shows the priority order (priority 0 is the highest).

***Table 2-22* • FB Operation Priority**

| Operation | Priority |
|---|---|
| System Initialization | 0 |
| FB Reset | 1 |
| Read | 2 |
| Write | 3 |
| Erase Page | 4 |
| Program | 5 |
| Unprotect Page | 6 |
| Discard Page | 7 |

## Timing Characteristics

***Table 2-31* • RAM4K9**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| $t_{BKH}$ | BL hold time | 0.02 | 0.02 | 0.02 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 1.79 | 2.03 | 2.39 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 2.36 | 2.68 | 3.15 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{C2CWWH}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum frequency | 310 | 272 | 231 | MHz |

*Notes:*

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-80). Table 2-40 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Family" table on page I of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-39.

***Table 2-39*** **• Channel Selection**

| Channel Number | CHNUMBER[4:0] |
|---|---|
| 0 | 00000 |
| 1 | 00001 |
| 2 | 00010 |
| 3 | 00011 |
| .<br>.<br>. | .<br>.<br>. |
| 30 | 11110 |
| 31 | 11111 |

Table 2-40 shows the correlation between the analog MUX input channels and the analog input pins.

***Table 2-40*** **• Analog MUX Channels**

| Analog MUX Channel | Signal | Analog Quad Number |
|---|---|---|
| 0 | Vcc_analog | |
| 1 | AV0 | Analog Quad 0 |
| 2 | AC0 | |
| 3 | AT0 | |
| 4 | AV1 | Analog Quad 1 |
| 5 | AC1 | |
| 6 | AT1 | |
| 7 | AV2 | Analog Quad 2 |
| 8 | AC2 | |
| 9 | AT2 | |
| 10 | AV3 | Analog Quad 3 |
| 11 | AC3 | |
| 12 | AT3 | |
| 13 | AV4 | Analog Quad 4 |
| 14 | AC4 | |
| 15 | AT4 | |

Similarly,

Min. Output Voltage = (Max. Negative input offset) + (Input Voltage x Max. Negative Channel Gain) = (–88 mV) + (5 V x 0.96) = **4.712 V**

### Calculating Accuracy for a Calibrated Analog Channel

***Formula***

For a given prescaler range, EQ 31 gives the output voltage.

*Output Voltage = Channel Error in V + Input Voltage*

*EQ 31*

where

*Channel Error in V = Total Channel Error in LSBs x Equivalent voltage per LSB*

***Example***

Input Voltage = 5 V

Chosen Prescaler range = 8 V range

Refer to Table 2-52 on page 2-123.

Max. Output Voltage = Max. Positive Channel Error in V + Input Voltage

Max. Positive Channel Error in V = (6 LSB) × (8 mV per LSB in 10-bit mode) = 48 mV

Max. Output Voltage = 48 mV + 5 V = **5.048 V**

Similarly,

Min. Output Voltage = Max. Negative Channel Error in V + Input Voltage = (–48 mV) + 5 V = **4.952 V**

### Calculating LSBs from a Given Error Budget

***Formula***

For a given prescaler range,

*LSB count = ± (Input Voltage × Required % error) / (Equivalent voltage per LSB)*

***Example***

Input Voltage = 3.3 V

Required error margin= 1%

Refer to Table 2-52 on page 2-123.

Equivalent voltage per LSB = 16 mV for a 16V prescaler, with ADC in 10-bit mode

LSB Count = ± (5.0 V × 1%) / (0.016)

LSB Count = **± 3.125**

Equivalent voltage per LSB = **8 mV** for an 8 V prescaler, with ADC in 10-bit mode

LSB Count = ± (5.0 V × 1%) / (0.008)

LSB Count = **± 6.25**

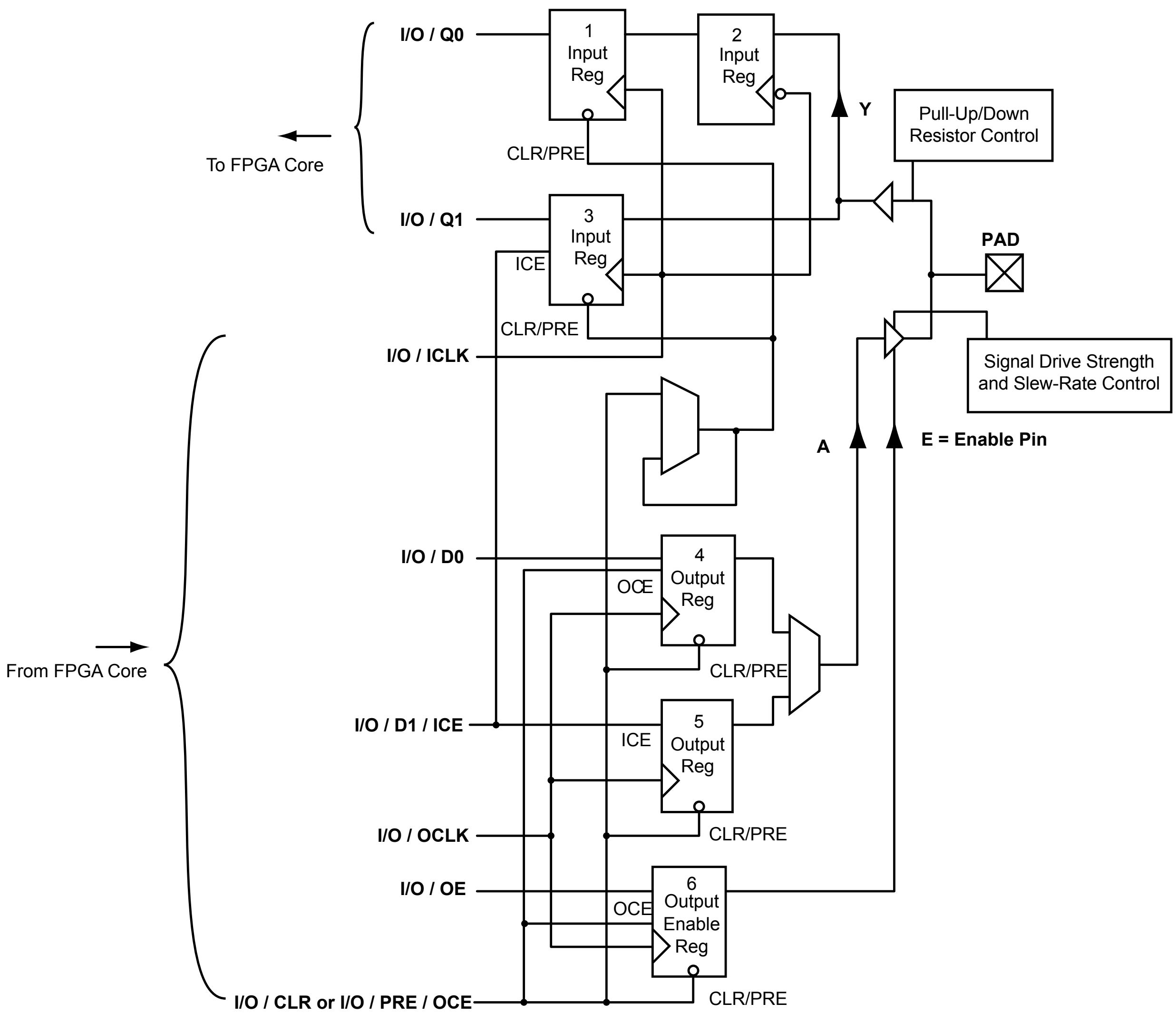
The 8 V prescaler satisfies the calculated LSB count accuracy requirement (see Table 2-52 on page 2-123).

## I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-100 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-100) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O register combining must satisfy some rules.




*Note:* *Fusion I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-139 for more information).*

***Figure 2-100* • I/O Block Logical Representation**

**Table 2-96 • I/O Output Buffer Maximum Resistances [1] (continued)**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (ohms) [2] | $R_{PULL\text{-}UP}$ (ohms) [3] |
|---|---|---|---|
| **Applicable to Standard I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$

**Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances**
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| VCCI | $R_{(WEAK\ PULL\text{-}UP)}$ [1] (ohms) | | $R_{(WEAK\ PULL\text{-}DOWN)}$ [2] (ohms) | |
|---|---|---|---|---|
| | **Min.** | **Max.** | **Min.** | **Max.** |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |

*Notes:*

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{WEAK\ PULL\text{-}UP\text{-}MIN}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{WEAK\ PULL\text{-}DOWN\text{-}MIN}$

### *Timing Characteristics*

***Table 2-112* • 2.5 V LVCMOS Low Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Pro I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.60 | 12.00 | 0.04 | 1.51 | 1.66 | 0.43 | 12.23 | 11.61 | 2.72 | 2.20 | 14.46 | 13.85 | ns |
| | –1 | 0.51 | 10.21 | 0.04 | 1.29 | 1.41 | 0.36 | 10.40 | 9.88 | 2.31 | 1.87 | 12.30 | 11.78 | ns |
| | –2 | 0.45 | 8.96 | 0.03 | 1.13 | 1.24 | 0.32 | 9.13 | 8.67 | 2.03 | 1.64 | 10.80 | 10.34 | ns |
| 8 mA | Std. | 0.60 | 8.73 | 0.04 | 1.51 | 1.66 | 0.43 | 8.89 | 8.01 | 3.10 | 2.93 | 11.13 | 10.25 | ns |
| | –1 | 0.51 | 7.43 | 0.04 | 1.29 | 1.41 | 0.36 | 7.57 | 6.82 | 2.64 | 2.49 | 9.47 | 8.72 | ns |
| | –2 | 0.45 | 6.52 | 0.03 | 1.13 | 1.24 | 0.32 | 6.64 | 5.98 | 2.32 | 2.19 | 8.31 | 7.65 | ns |
| 12 mA | Std. | 0.66 | 6.77 | 0.04 | 1.51 | 1.66 | 0.43 | 6.90 | 6.11 | 3.37 | 3.39 | 9.14 | 8.34 | ns |
| | –1 | 0.56 | 5.76 | 0.04 | 1.29 | 1.41 | 0.36 | 5.87 | 5.20 | 2.86 | 2.89 | 7.77 | 7.10 | ns |
| | –2 | 0.49 | 5.06 | 0.03 | 1.13 | 1.24 | 0.32 | 5.15 | 4.56 | 2.51 | 2.53 | 6.82 | 6.23 | ns |
| 16 mA | Std. | 0.66 | 6.31 | 0.04 | 1.51 | 1.66 | 0.43 | 6.42 | 5.73 | 3.42 | 3.52 | 8.66 | 7.96 | ns |
| | –1 | 0.56 | 5.37 | 0.04 | 1.29 | 1.41 | 0.36 | 5.46 | 4.87 | 2.91 | 3.00 | 7.37 | 6.77 | ns |
| | –2 | 0.49 | 4.71 | 0.03 | 1.13 | 1.24 | 0.32 | 4.80 | 4.28 | 2.56 | 2.63 | 6.47 | 5.95 | ns |
| 24 mA | Std. | 0.66 | 5.93 | 0.04 | 1.51 | 1.66 | 0.43 | 6.04 | 5.70 | 3.49 | 4.00 | 8.28 | 7.94 | ns |
| | –1 | 0.56 | 5.05 | 0.04 | 1.29 | 1.41 | 0.36 | 5.14 | 4.85 | 2.97 | 3.40 | 7.04 | 6.75 | ns |
| | –2 | 0.49 | 4.43 | 0.03 | 1.13 | 1.24 | 0.32 | 4.51 | 4.26 | 2.61 | 2.99 | 6.18 | 5.93 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to* *Table 3-7 on page 3-9.*

## Differential I/O Characteristics

Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

### LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-134. The building blocks of the LVDS transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

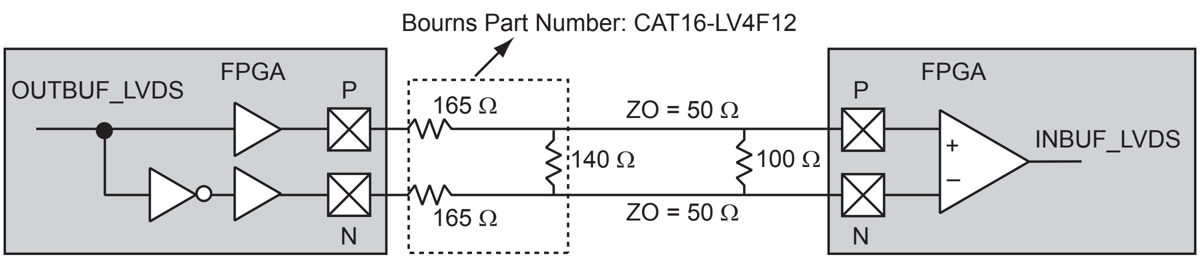



***Figure 2-134*** **• LVDS Circuit Diagram and Board-Level Implementation**

***Table 2-168*** **• Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Input High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL [1] | Output Low Voltage | 0.65 | 0.91 | 1.16 | mA |
| IOH [1] | Output High Voltage | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIL [2,3] | Input Low Voltage | | | 10 | µA |
| IIH [2,4] | Input High Voltage | | | 10 | µA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage | 100 | 350 | | mV |

*Notes:*

1. *IOL/IOH defined by VODIFF/(Resistor Network)*
2. *Currents are measured at 85°C junction temperature.*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

## I/O Register Specifications

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

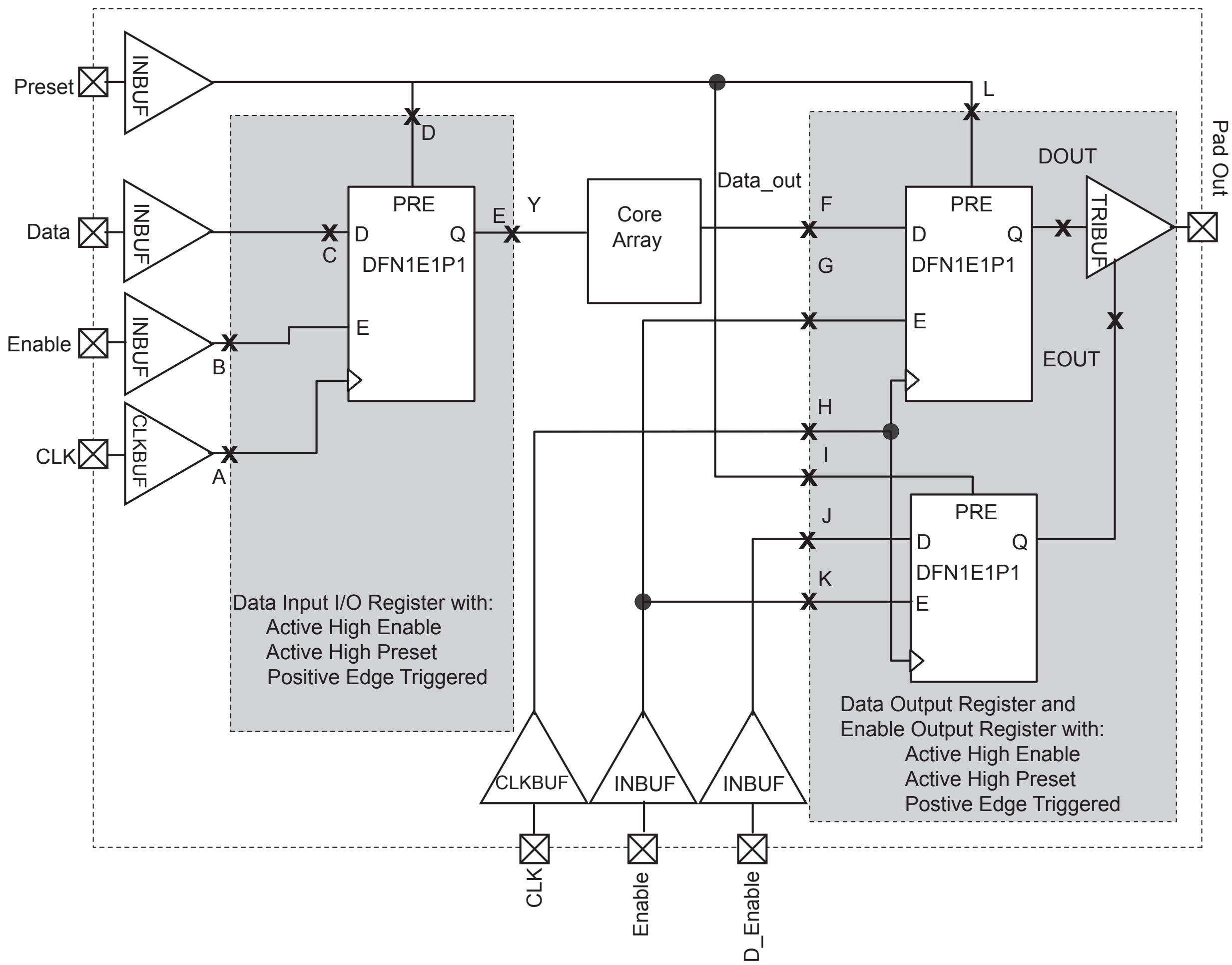



***Figure 2-137* • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

## Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

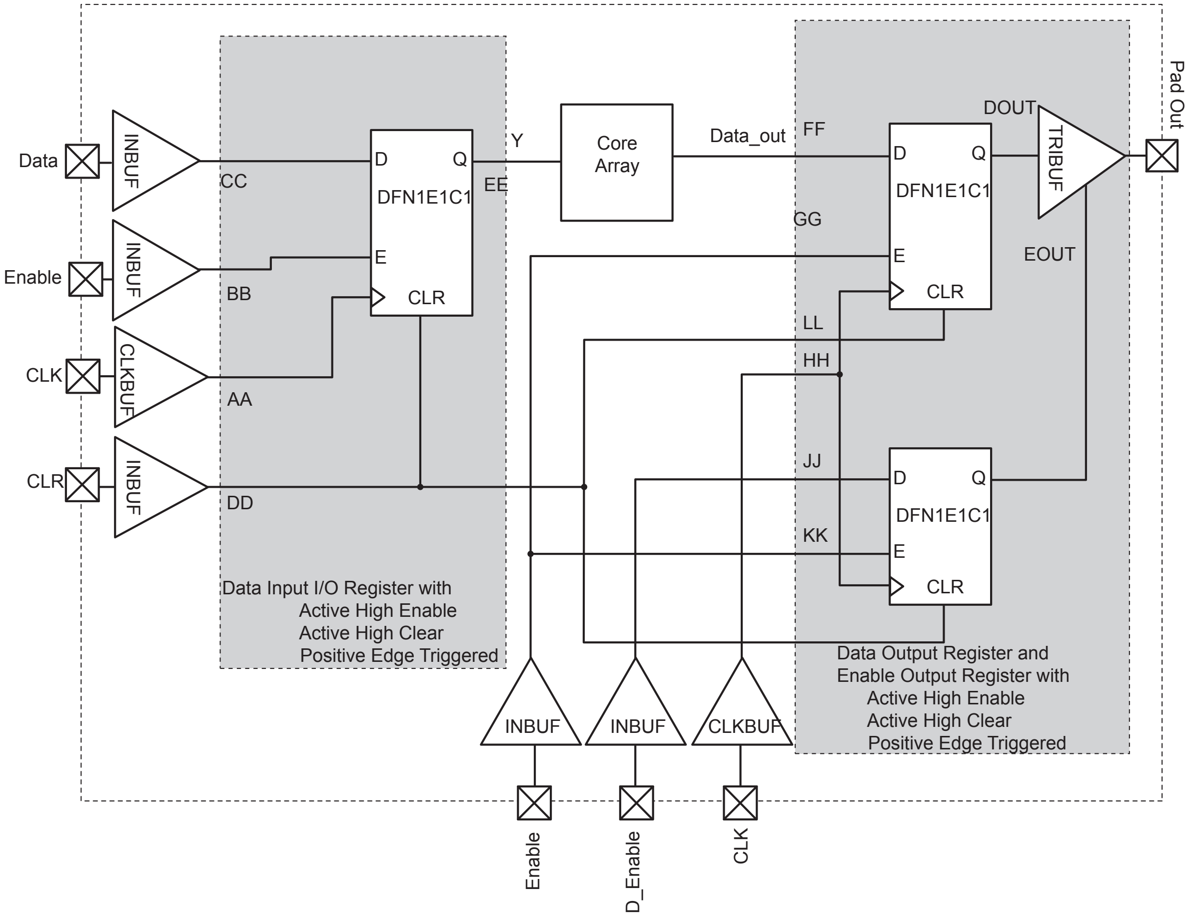



**Figure 2-138 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

## Input Register

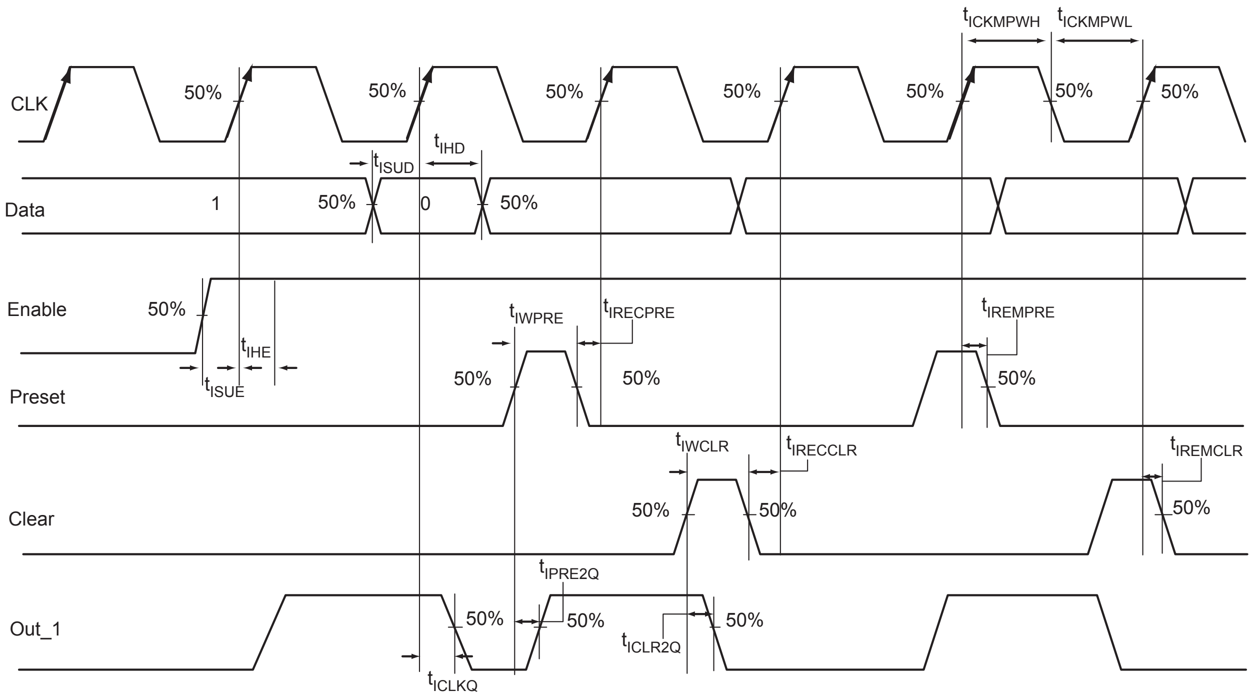



***Figure 2-139*** **• Input Register Timing Diagram**

### *Timing Characteristics*

***Table 2-176*** **• Input Data Register Propagation Delays**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.24 | 0.27 | 0.32 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.26 | 0.30 | 0.35 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 0.37 | 0.42 | 0.50 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.32 | 0.37 | 0.43 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to* *Table 3-7 on page 3-9.*

***Table 3-8 •* AFS1500 Quiescent Supply Current Characteristics (continued)**

| Parameter | Description | Conditions | Temp. | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| IJTAG | JTAG I/O quiescent current | Operational standby[4], VJTAG = 3.63 V | $T_J$ = 25°C | | 80 | 100 | µA |
| | | | $T_J$ = 85°C | | 80 | 100 | µA |
| | | | $T_J$ = 100°C | | 80 | 100 | µA |
| | | Standby mode[5] or Sleep mode[6], VJTAG = 0 V | | | 0 | 0 | µA |
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | $T_J$ = 25°C | | 39 | 80 | µA |
| | | | $T_J$ = 85°C | | 40 | 80 | µA |
| | | | $T_J$ = 100°C | | 40 | 80 | µA |
| | | Standby mode[5] or Sleep mode[6], VPUMP = 0 V | | | 0 | 0 | µA |
| ICCNVM | Embedded NVM current | Reset asserted, $V_{CCNVM}$ = 1.575 V | $T_J$ = 25°C | | 50 | 150 | µA |
| | | | $T_J$ =85°C | | 50 | 150 | µA |
| | | | $T_J$ = 100°C | | 50 | 150 | µA |
| ICCPLL | 1.5 V PLL quiescent current | Operational standby , VCCPLL = 1.575 V | $T_J$ = 25°C | | 130 | 200 | µA |
| | | | $T_J$ = 85°C | | 130 | 200 | µA |
| | | | $T_J$ = 100°C | | 130 | 200 | µA |

*Notes:*

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

| FG256 | | | | |
|---|---|---|---|---|
| Pin Number | AFS090 Function | AFS250 Function | AFS600 Function | AFS1500 Function |
| C7 | IO09RSB0V0 | IO12RSB0V0 | IO06NDB0V0 | IO09NDB0V1 |
| C8 | IO14RSB0V0 | IO22RSB0V0 | IO16PDB1V0 | IO23PDB1V0 |
| C9 | IO15RSB0V0 | IO23RSB0V0 | IO16NDB1V0 | IO23NDB1V0 |
| C10 | IO22RSB0V0 | IO30RSB0V0 | IO25NDB1V1 | IO31NDB1V1 |
| C11 | IO20RSB0V0 | IO31RSB0V0 | IO25PDB1V1 | IO31PDB1V1 |
| C12 | VCCIB0 | VCCIB0 | VCCIB1 | VCCIB1 |
| C13 | GBB1/IO28RSB0V0 | GBC1/IO35RSB0V0 | GBC1/IO26PPB1V1 | GBC1/IO40PPB1V2 |
| C14 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| C15 | GND | GND | GND | GND |
| C16 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| D1 | GFC2/IO50NPB3V0 | IO75NDB3V0 | IO84NDB4V0 | IO124NDB4V0 |
| D2 | GFA2/IO51NDB3V0 | GAB2/IO75PDB3V0 | GAB2/IO84PDB4V0 | GAB2/IO124PDB4V0 |
| D3 | GAC2/IO51PDB3V0 | IO76NDB3V0 | IO85NDB4V0 | IO125NDB4V0 |
| D4 | GAA2/IO52PDB3V0 | GAA2/IO76PDB3V0 | GAA2/IO85PDB4V0 | GAA2/IO125PDB4V0 |
| D5 | GAB2/IO52NDB3V0 | GAB0/IO02RSB0V0 | GAB0/IO02NPB0V0 | GAB0/IO02NPB0V0 |
| D6 | GAC0/IO04RSB0V0 | GAC0/IO04RSB0V0 | GAC0/IO03NDB0V0 | GAC0/IO03NDB0V0 |
| D7 | IO08RSB0V0 | IO13RSB0V0 | IO06PDB0V0 | IO09PDB0V1 |
| D8 | NC | IO20RSB0V0 | IO14NDB0V1 | IO15NDB0V2 |
| D9 | NC | IO21RSB0V0 | IO14PDB0V1 | IO15PDB0V2 |
| D10 | IO21RSB0V0 | IO28RSB0V0 | IO23PDB1V1 | IO37PDB1V2 |
| D11 | IO23RSB0V0 | GBB0/IO36RSB0V0 | GBB0/IO27NDB1V1 | GBB0/IO41NDB1V2 |
| D12 | NC | NC | VCCIB1 | VCCIB1 |
| D13 | GBA2/IO31PDB1V0 | GBA2/IO40PDB1V0 | GBA2/IO30PDB2V0 | GBA2/IO44PDB2V0 |
| D14 | GBB2/IO31NDB1V0 | IO40NDB1V0 | IO30NDB2V0 | IO44NDB2V0 |
| D15 | GBC2/IO32PDB1V0 | GBB2/IO41PDB1V0 | GBB2/IO31PDB2V0 | GBB2/IO45PDB2V0 |
| D16 | GCA2/IO32NDB1V0 | IO41NDB1V0 | IO31NDB2V0 | IO45NDB2V0 |
| E1 | GND | GND | GND | GND |
| E2 | GFB0/IO48NPB3V0 | IO73NDB3V0 | IO81NDB4V0 | IO118NDB4V0 |
| E3 | GFB2/IO50PPB3V0 | IO73PDB3V0 | IO81PDB4V0 | IO118PDB4V0 |
| E4 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| E5 | NC | IO74NPB3V0 | IO83NPB4V0 | IO123NPB4V0 |
| E6 | NC | IO08RSB0V0 | IO04NPB0V0 | IO05NPB0V1 |
| E7 | GND | GND | GND | GND |
| E8 | NC | IO18RSB0V0 | IO08PDB0V1 | IO11PDB0V1 |
| E9 | NC | NC | IO20NDB1V0 | IO27NDB1V1 |
| E10 | GND | GND | GND | GND |
| E11 | IO24RSB0V0 | GBB1/IO37RSB0V0 | GBB1/IO27PDB1V1 | GBB1/IO41PDB1V2 |
| E12 | NC | IO50PPB1V0 | IO33PSB2V0 | IO48PSB2V0 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.3 (continued) | The "Temperature Monitor" section was updated. | 2-96 |
| | EQ 2 is new. | 2-103 |
| | The "ADC Description" section was updated. | 2-102 |
| | Figure 2-16 • Fusion Clocking Options was updated. | 2-20 |
| | Table 2-46 · Analog Channel Specifications was updated. | 2-118 |
| | The notes in Table 2-72 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities were updated. | 2-144 |
| | The "Simultaneously Switching Outputs and PCB Layout" section is new. | 2-149 |
| | LVPECL and LVDS were updated in Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications. | 2-157 |
| | LVPECL and LVDS were updated in Table 2-82 • Fusion Pro I/O Attributes vs. I/O Standard Applications. | 2-158 |
| | The "Timing Model" was updated. | 2-161 |
| | All voltage-referenced Minimum and Maximum DC Input and Output Level tables were updated. | N/A |
| | All Timing Characteristic tables were updated | N/A |
| | Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated. | 2-165 |
| | Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated. | 2-134 |
| | Table 2-93 • I/O Output Buffer Maximum Resistances [1] was updated. | 2-171 |
| | The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet. | 2-211 |
| | The "CoreMP7 and Cortex-M1 Software Tools" section is new. | 2-257 |
| | Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated. | 2-165 |
| | Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated. | 2-134 |
| | Table 2-93 • I/O Output Buffer Maximum Resistances [1] was updated. | 2-171 |
| | The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet. | 2-211 |
| | The "108-Pin QFN" table for the AFS090 device is new. | 3-2 |
| | The "180-Pin QFN" table for the AFS090 device is new. | 3-4 |
| | The "208-Pin PQFP" table for the AFS090 device is new. | 3-8 |
| | The "256-Pin FBGA" table for the AFS090 device is new. | 3-12 |
| | The "256-Pin FBGA" table for the AFS250 device is new. | 3-12 |