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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-2fgg484

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.

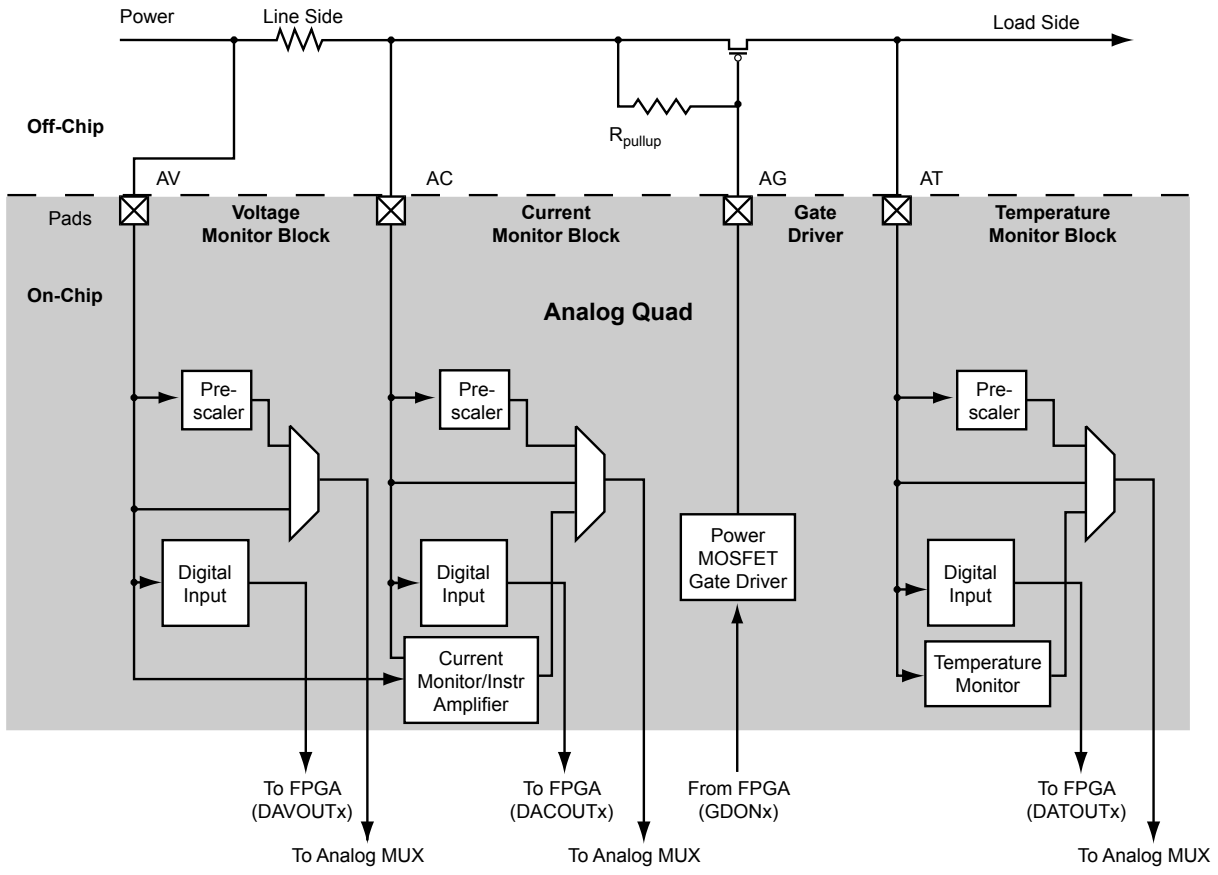


Figure 1-1 • **Analog Quad**

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

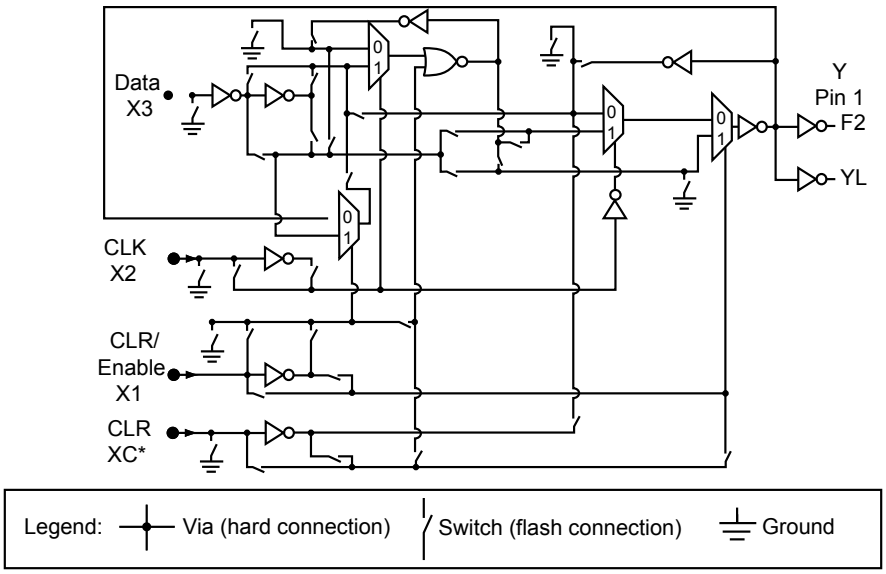
As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



*Note: *This input can only be connected to the global clock distribution network.*

Figure 2-2 • **Fusion Core VersaTile**

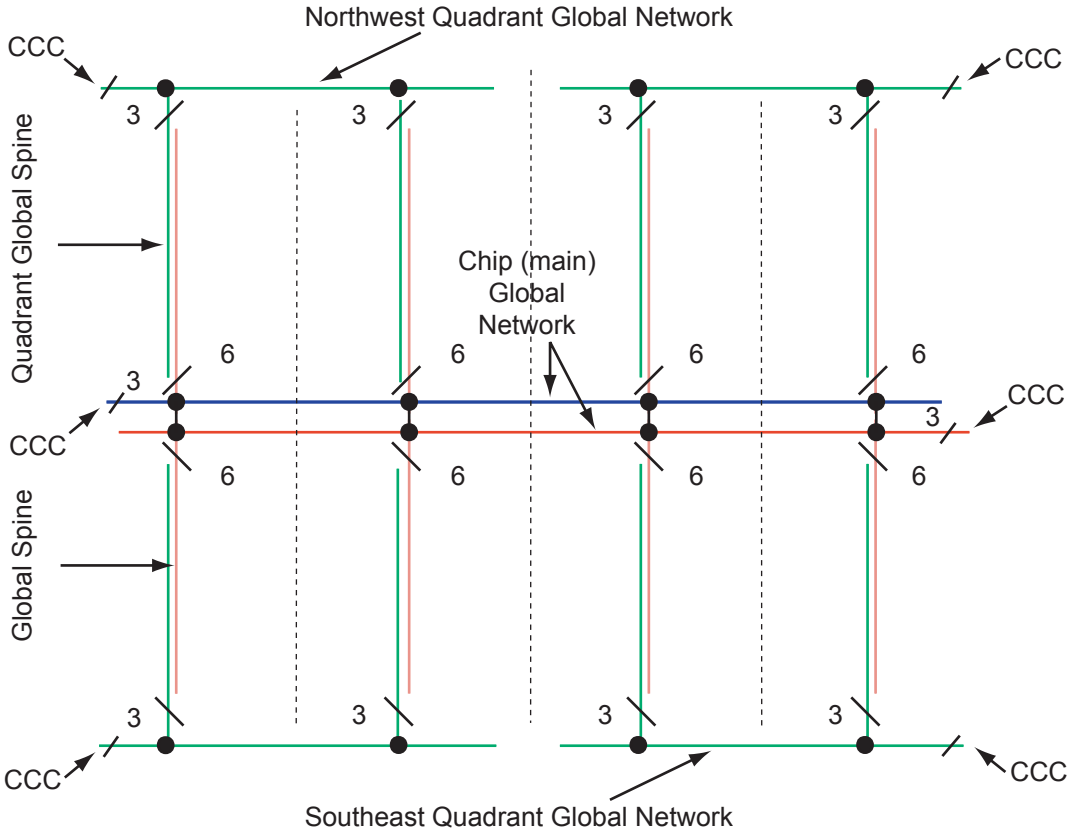


Figure 2-12 • **Global Network Architecture**

Table 2-4 • **Globals/Spines/Rows by Device**

	AFS090	AFS250	AFS600	AFS1500
Global VersaNets (trees)*	9	9	9	9
VersaNet Spines/Tree	4	8	12	20
Total Spines	36	72	108	180
VersaTiles in Each Top or Bottom Spine	384	768	1,152	1,920
Total VersaTiles	2,304	6,144	13,824	38,400

*Note: *There are six chip (main) globals and three globals per quadrant.*

Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-40 and Figure 2-41.

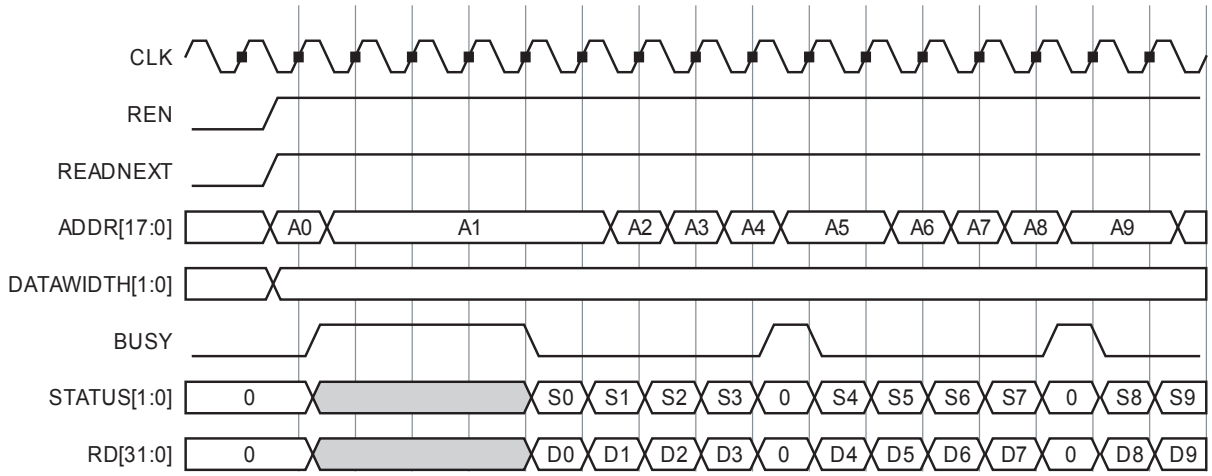


***Figure 2-40* • Read Next Waveform (Non-Pipe Mode, 32-bit access)**

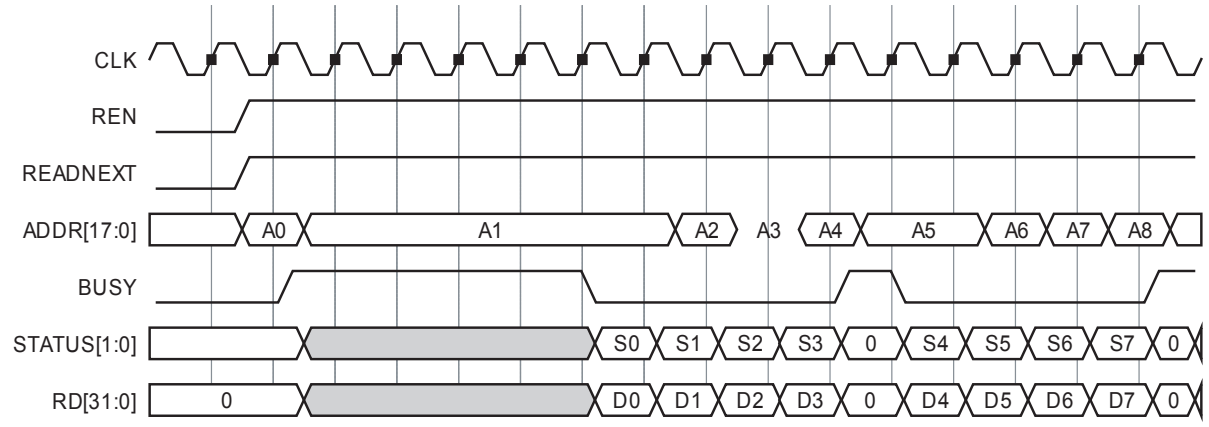


***Figure 2-41* • Read Next WaveForm (Pipe Mode, 32-bit access)**

FIFO4K18 Description

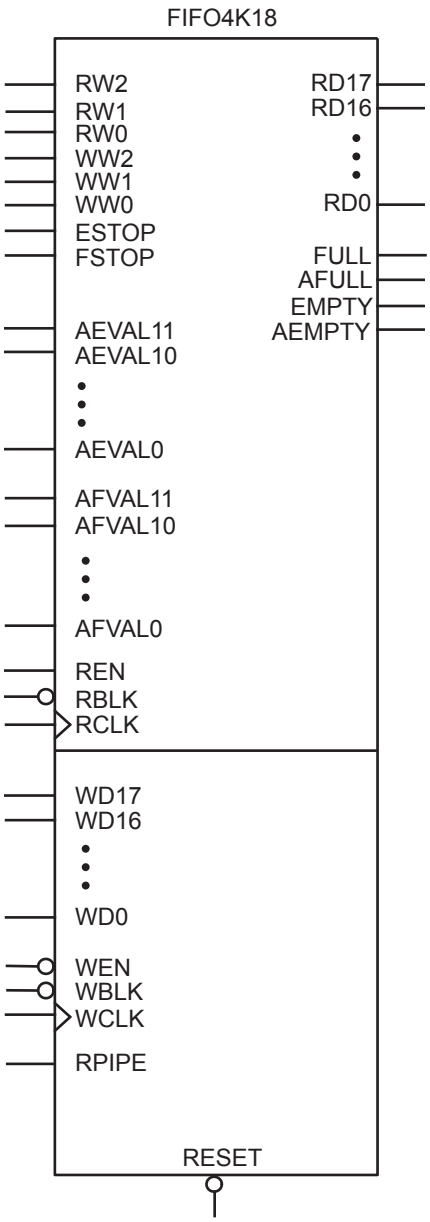


Figure 2-56 • **FIFO4KX18**

Analog-to-Digital Converter Block

At the heart of the Fusion analog system is a programmable Successive Approximation Register (SAR) ADC. The ADC can support 8-, 10-, or 12-bit modes of operation. In 12-bit mode, the ADC can resolve 500 ksps. All results are MSB-justified in the ADC. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 2-79. The ADC offers multiple self-calibrating modes to ensure consistent high performance both at power-up and during runtime.

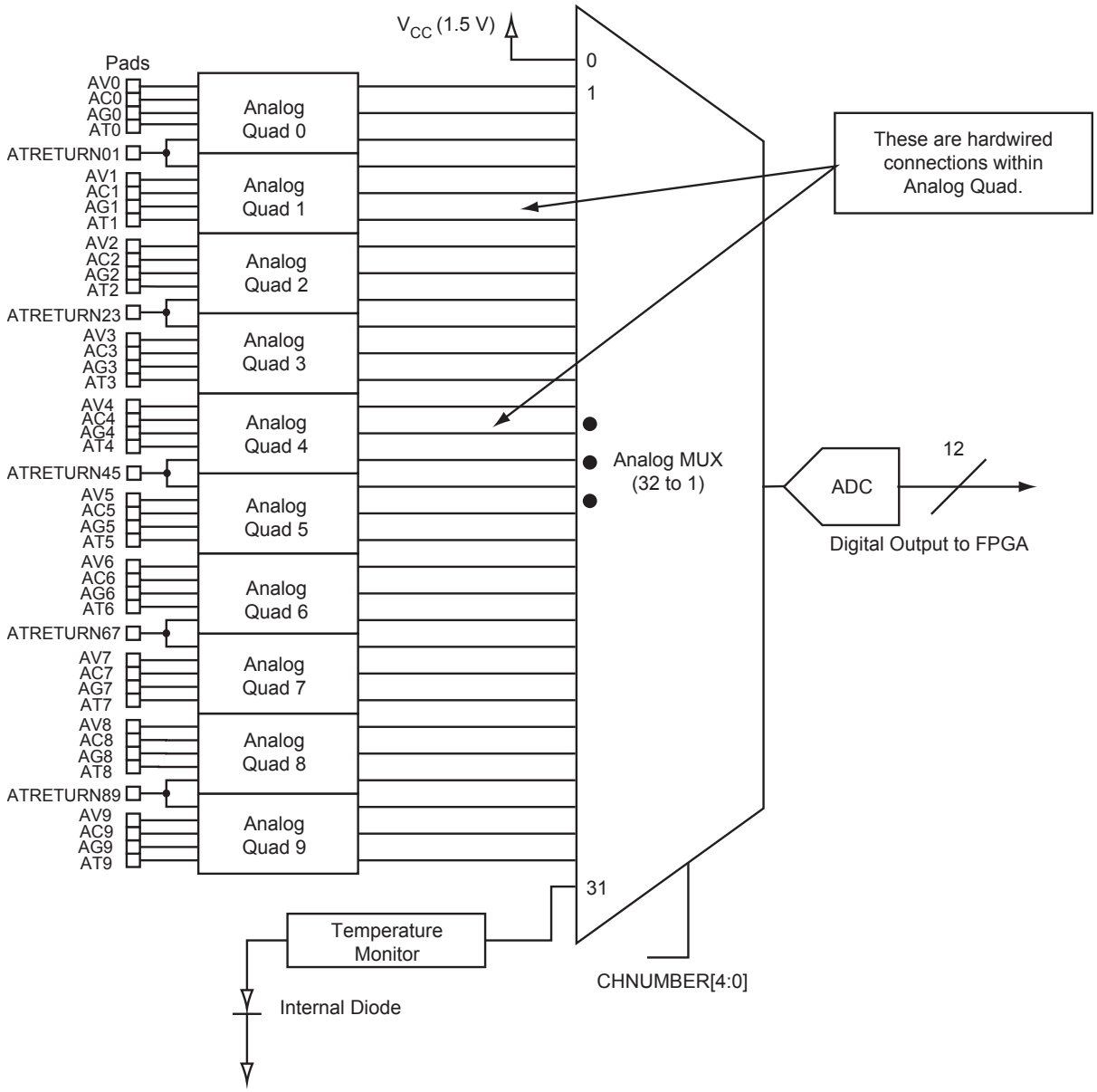


Figure 2-79 • **ADC Block Diagram**

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ideal ADC, the first transition occurs at 0.5 LSB above zero. The offset voltage is measured by applying an analog input such that the ADC outputs all zeroes and increases until the first transition occurs (Figure 2-86).

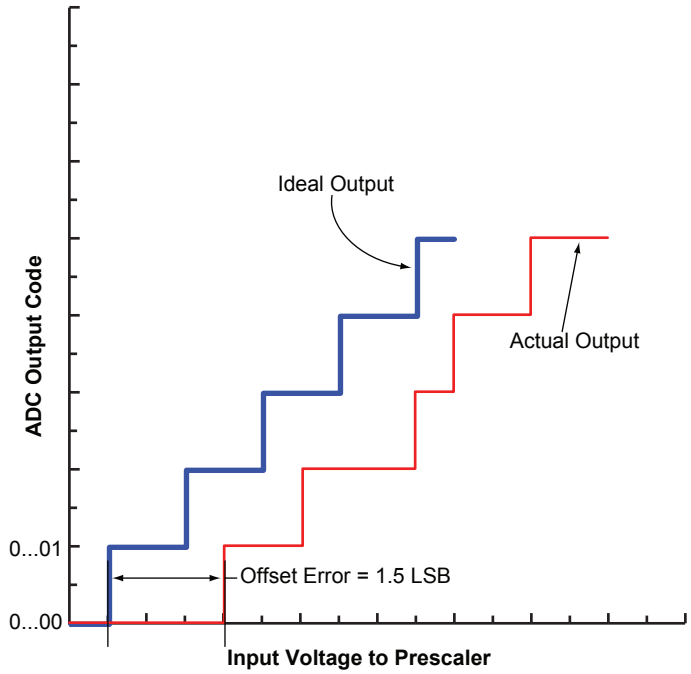


Figure 2-86 • **Offset Error**

Resolution

ADC resolution is the number of bits used to represent an analog input signal. To more accurately replicate the analog signal, resolution needs to be increased.

Sampling Rate

Sampling rate or sample frequency, specified in samples per second (sps), is the rate at which an ADC acquires (samples) the analog input.

SNR – Signal-to-Noise Ratio

SNR is the ratio of the amplitude of the desired signal to the amplitude of the noise signals at a given point in time. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR (EQ 14) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum ADC noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[MAX]} = 6.02_{dB} \times N + 1.76_{dB}$$

EQ 14

SINAD – Signal-to-Noise and Distortion

SINAD is the ratio of the rms amplitude to the mean value of the root-sum-square of the all other spectral components, including harmonics, but excluding DC. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion.

Total Harmonic Distortion

THD measures the distortion content of a signal, and is specified in decibels relative to the carrier (dBc). THD is the ratio of the RMS sum of the selected harmonics of the input signal to the fundamental itself. Only harmonics within the Nyquist limit are included in the measurement.

Table 2-54 • **ACM Address Decode Table for Analog Quad (continued)**

ACMADDR [7:0] in Decimal	Name	Description	Associated Peripheral
73	MATCHREG1	Match register bits 15:8	RTC
74	MATCHREG2	Match register bits 23:16	RTC
75	MATCHREG3	Match register bits 31:24	RTC
76	MATCHREG4	Match register bits 39:32	RTC
80	MATCHBITS0	Individual match bits 7:0	RTC
81	MATCHBITS1	Individual match bits 15:8	RTC
82	MATCHBITS2	Individual match bits 23:16	RTC
83	MATCHBITS3	Individual match bits 31:24	RTC
84	MATCHBITS4	Individual match bits 39:32	RTC
88	CTRL_STAT	Control (write) / Status (read) register bits 7:0	RTC
Note: ACMADDR bytes 1 to 40 pertain to the Analog Quads; bytes 64 to 89 pertain to the RTC.			

ACM Characteristics[1]

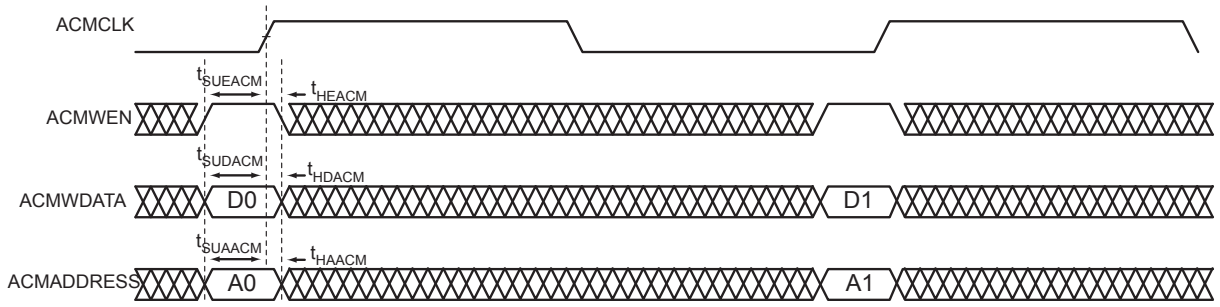


Figure 2-97 • **ACM Write Waveform**

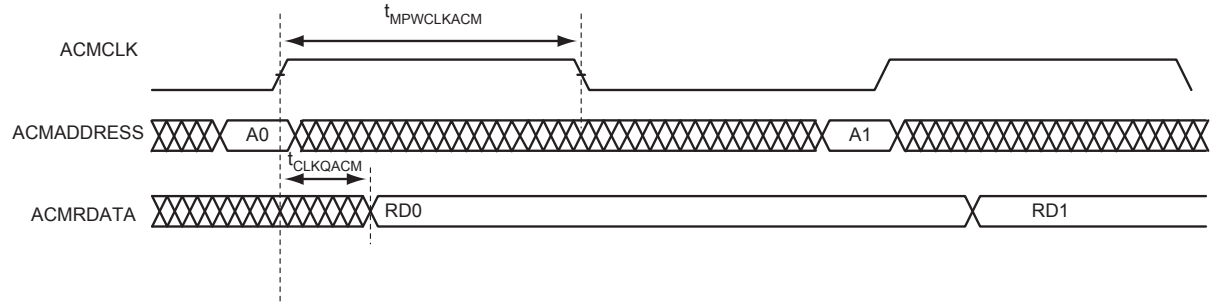


Figure 2-98 • **ACM Read Waveform**

1. *When addressing the RTC addresses (i.e., ACMADDR 64 to 89), there is no timing generator, and the rc_osc, byte_en, and aq_wen signals have no impact.*

Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = I/O Standard Dependent
Applicable to Pro I/Os

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
2.5 V LVCMOS	12 mA	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
1.8 V LVCMOS	12 mA	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
1.5 V LVCMOS	12 mA	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.49	2.09	0.03	0.77	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V GTL	20 mA	High	10	25	0.49	1.55	0.03	2.19	–	0.32	1.52	1.55	0.00	0.00	3.19	3.22	ns
2.5 V GTL	20 mA	High	10	25	0.49	1.59	0.03	1.83	–	0.32	1.61	1.59	0.00	0.00	3.28	3.26	ns
3.3 V GTL+	35 mA	High	10	25	0.49	1.53	0.03	1.19	–	0.32	1.56	1.53	0.00	0.00	3.23	3.20	ns
2.5 V GTL+	33 mA	High	10	25	0.49	1.65	0.03	1.13	–	0.32	1.68	1.57	0.00	0.00	3.35	3.24	ns
HSTL (I)	8 mA	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	0.00	0.00	4.09	4.02	ns
HSTL (II)	15 mA	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	0.00	0.00	3.97	3.70	ns
SSTL2 (I)	17 mA	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	0.00	0.00	3.29	3.05	ns
SSTL2 (II)	21 mA	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	0.00	0.00	3.32	2.99	ns
SSTL3 (I)	16 mA	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	0.00	0.00	3.42	3.04	ns
SSTL3 (II)	24 mA	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	0.00	0.00	3.24	2.92	ns
LVDS	24 mA	High	–	–	0.49	1.57	0.03	1.36	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.49	1.60	0.03	1.22	–	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-123 on page 2-197 for connectivity. This resistor is not required during normal operation.*

Table 2-96 • I/O Output Buffer Maximum Resistances [1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
Applicable to Standard I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$

Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK\ PULL\text{-}UP)}$ [1] (ohms)		$R_{(WEAK\ PULL\text{-}DOWN)}$ [2] (ohms)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{WEAK\ PULL\text{-}UP\text{-}MIN}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{WEAK\ PULL\text{-}DOWN\text{-}MIN}$

Table 2-107 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	7.66	0.04	1.20	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.56	6.51	0.04	1.02	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.49	5.72	0.03	0.90	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
8 mA	Std.	0.66	4.91	0.04	1.20	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	–1	0.56	4.17	0.04	1.02	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.49	3.66	0.03	0.90	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	Std.	0.66	3.53	0.04	1.20	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	–1	0.56	3.00	0.04	1.02	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	–2	0.49	2.64	0.03	0.90	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	Std.	0.66	3.33	0.04	1.20	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	–1	0.56	2.83	0.04	1.02	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	–2	0.49	2.49	0.03	0.90	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	Std.	0.66	3.08	0.04	1.20	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	–1	0.56	2.62	0.04	1.02	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	–2	0.49	2.30	0.03	0.90	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-108 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	–1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	–2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
4 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	–1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	–2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
6 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	–1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	–2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns
8 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	–1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	–2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Input Register

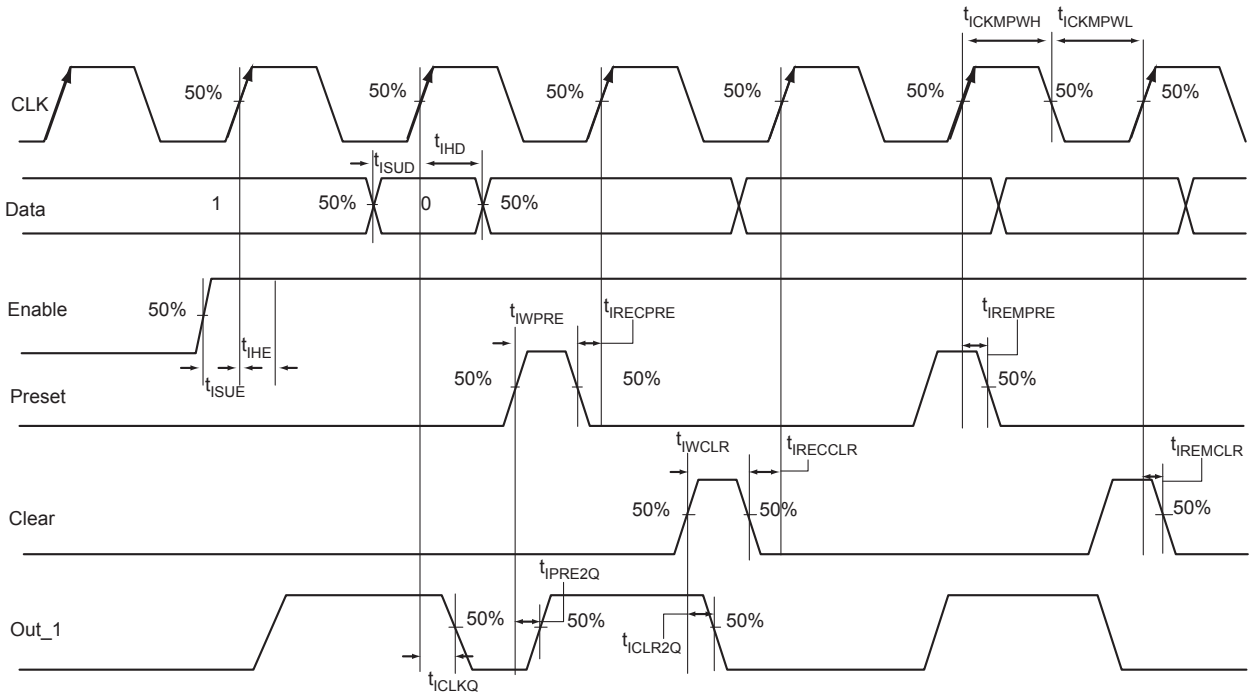


***Figure 2-139* • Input Register Timing Diagram**

Timing Characteristics

***Table 2-176* • Input Data Register Propagation Delays**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Output DDR

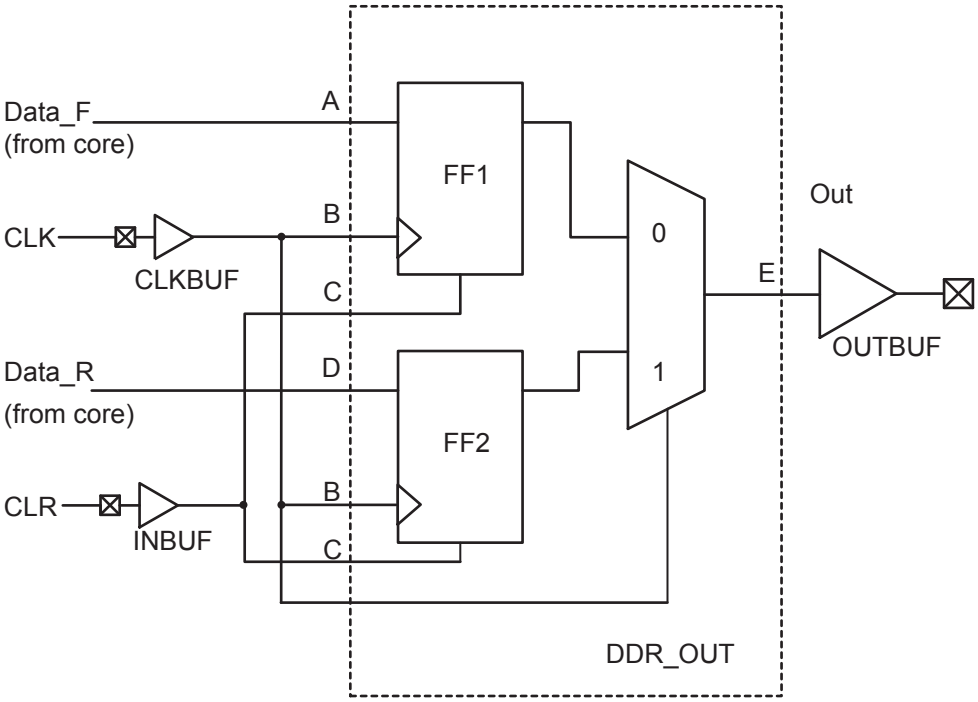


Figure 2-144 • **Output DDR Timing Model**

Table 2-181 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings[1] (continued)

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52
Applicable to Standard I/O Banks				
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	431.08
2.5 V LVCMOS	35	2.5	–	247.36
1.8 V LVCMOS	35	1.8	–	128.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	89.46

Notes:

1. *Dynamic power consumption is given for standard load and software-default drive strength and output slew.*
2. *PDC8 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*

Dynamic Power Consumption of Various Internal Resources

***Table 3-14* • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices**

Parameter	Definition	Power Supply		Device-Specific Dynamic Contributions				Units
		Name	Setting	AFS1500	AFS600	AFS250	AFS090	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	14.5	12.8	11	11	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	2.5	1.9	1.6	0.8	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	0.81				µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.11				µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07				µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29				µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29				µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	0.70				µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCI	See Table 3-12 on page 3-18					
PAC10	Contribution of an I/O output pin (standard dependent)	VCCI	See Table 3-13 on page 3-20					
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25				µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30				µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.6				µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358				µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33 MHz)	VCC	1.5 V	12.88				mW
PAC17	2nd contribution of NVM block during a read operation (F > 33 MHz)	VCC	1.5 V	4.8				µW/MHz
PAC18	Crystal Oscillator contribution	VCC33A	3.3 V	0.63				mW
PAC19	RC Oscillator contribution	VCC33A	3.3 V	3.3				mW
PAC20	Analog Block dynamic power contribution of ADC	VCC	1.5 V	3				mW

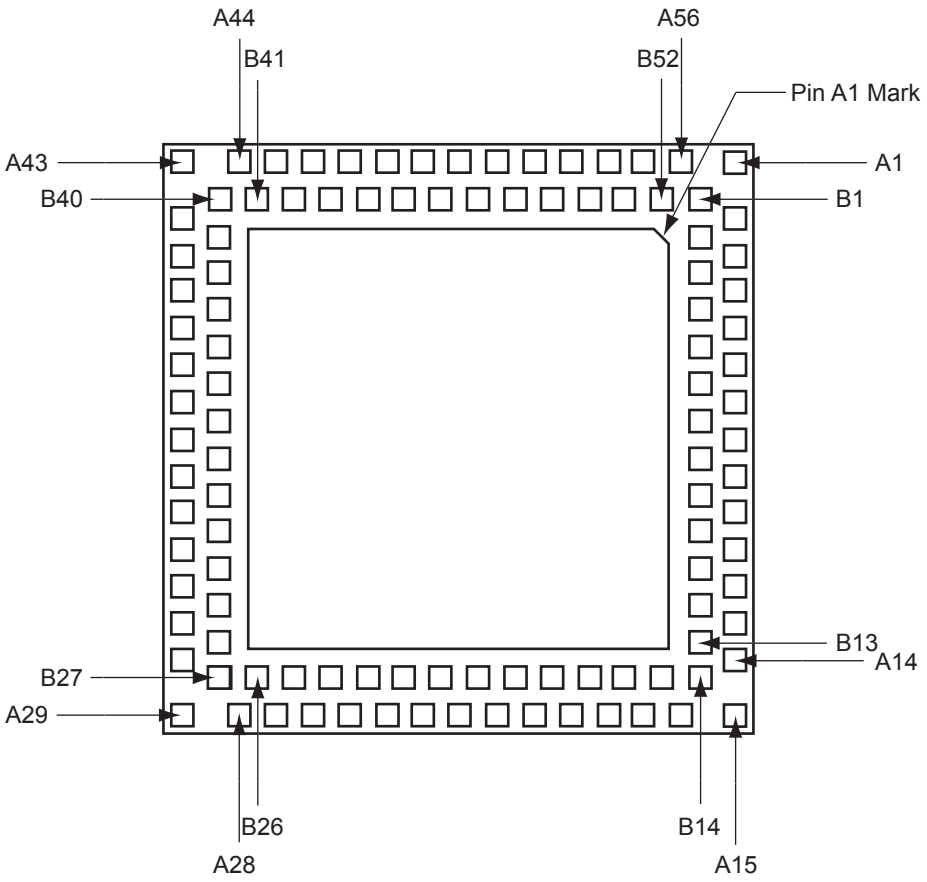
Power Consumption

***Table 3-18* • Power Consumption**

Parameter	Description	Condition	Min.	Typical	Max.	Units
Crystal Oscillator						
ISTBXTAL	Standby Current of Crystal Oscillator			10		µA
IDYNXTAL	Operating Current	RC		0.6		mA
		0.032–0.2		0.19		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
RC Oscillator						
IDYNRC	Operating Current			1		mA
ACM						
	Operating Current (fixed clock)			200		µA/MHz
	Operating Current (user clock)			30		µA
NVM System						
	NVM Array Operating Power	Idle		795		µA
		Read operation		See Table 3-15 on page 3-23.		See Table 3-15 on page 3-23.
		Erase		900		µA
		Write		900		µA
PNVMCTRL	NVM Controller Operating Power			20		µW/MHz

4 – Package Pin Assignments

QN108



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

FG484		
Pin Number	AFS600 Function	AFS1500 Function
L17	VCCIB2	VCCIB2
L18	IO46PDB2V0	IO69PDB2V0
L19	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
L20	VCCIB2	VCCIB2
L21	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0
L22	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0
M1	NC	IO103PDB4V0
M2	XTAL1	XTAL1
M3	VCCIB4	VCCIB4
M4	GNDOSC	GNDOSC
M5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
M6	VCCIB4	VCCIB4
M7	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
M8	VCCIB4	VCCIB4
M9	VCC	VCC
M10	GND	GND
M11	VCC	VCC
M12	GND	GND
M13	VCC	VCC
M14	GND	GND
M15	VCCIB2	VCCIB2
M16	IO48NDB2V0	IO70NDB2V0
M17	VCCIB2	VCCIB2
M18	IO46NDB2V0	IO69NDB2V0
M19	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
M20	VCCIB2	VCCIB2
M21	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
M22	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
N1	NC	IO103NDB4V0
N2	GND	GND
N3	IO68PDB4V0	IO101PDB4V0
N4	NC	IO100NPB4V0
N5	GND	GND
N6	NC	IO99PDB4V0
N7	NC	IO97PDB4V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
N8	GND	GND
N9	GND	GND
N10	VCC	VCC
N11	GND	GND
N12	VCC	VCC
N13	GND	GND
N14	VCC	VCC
N15	GND	GND
N16	GDB2/IO56PDB2V0	GDB2/IO83PDB2V0
N17	NC	IO78PDB2V0
N18	GND	GND
N19	IO47NDB2V0	IO72NDB2V0
N20	IO47PDB2V0	IO72PDB2V0
N21	GND	GND
N22	IO49PDB2V0	IO71PDB2V0
P1	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
P2	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
P3	IO68NDB4V0	IO101NDB4V0
P4	IO65PDB4V0	IO96PDB4V0
P5	IO65NDB4V0	IO96NDB4V0
P6	NC	IO99NDB4V0
P7	NC	IO97NDB4V0
P8	VCCIB4	VCCIB4
P9	VCC	VCC
P10	GND	GND
P11	VCC	VCC
P12	GND	GND
P13	VCC	VCC
P14	GND	GND
P15	VCCIB2	VCCIB2
P16	IO56NDB2V0	IO83NDB2V0
P17	NC	IO78NDB2V0
P18	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
P19	GDB1/IO53PDB2V0	GDB1/IO80PDB2V0
P20	IO51NDB2V0	IO73NDB2V0

FG676	
Pin Number	**AFS1500 Function**
L17	VCCIB2
L18	GCB2/IO60PDB2V0
L19	IO58NDB2V0
L20	IO57NDB2V0
L21	IO59NDB2V0
L22	GCC2/IO61PDB2V0
L23	IO55PPB2V0
L24	IO56PDB2V0
L25	IO55NPB2V0
L26	GND
M1	NC
M2	VCCIB4
M3	GFC2/IO108PDB4V0
M4	GND
M5	IO109NDB4V0
M6	IO110NDB4V0
M7	GND
M8	IO104NDB4V0
M9	IO111NDB4V0
M10	GND
M11	V**CC**
M12	GND
M13	VCC
M14	GND
M15	VCC
M16	GND
M17	GND
M18	IO60NDB2V0
M19	IO58PDB2V0
M20	GND
M21	IO68NPB2V0
M22	IO61NDB2V0
M23	GND
M24	IO56NDB2V0
M25	VCCIB2
M26	IO65PDB2V0

FG676	
Pin Number	**AFS1500 Function**
N1	NC
N2	NC
N3	IO108NDB4V0
N4	VCCOSC
N5	VCCIB4
N6	XTAL2
N7	GFC1/IO107PDB4V0
N8	VCCIB4
N9	GFB1/IO106PDB4V0
N10	VCCIB4
N11	GND
N12	VCC
N13	GND
N14	VCC
N15	GND
N16	VCC
N17	VCCIB2
N18	IO70PDB2V0
N19	VCCIB2
N20	IO69PDB2V0
N21	GCA1/IO64PDB2V0
N22	VCCIB2
N23	GCC0/IO62NDB2V0
N24	GCC1/IO62PDB2V0
N25	IO66PDB2V0
N26	IO65NDB2V0
P1	NC
P2	NC
P3	IO103PDB4V0
P4	XTAL1
P5	VCCIB4
P6	GNDOSC
P7	GFC0/IO107NDB4V0
P8	VCCIB4
P9	GFB0/IO106NDB4V0
P10	VCCIB4

FG676	
Pin Number	**AFS1500 Function**
P11	VCC
P12	GND
P13	VCC
P14	GND
P15	VCC
P16	GND
P17	VCCIB2
P18	IO70NDB2V0
P19	VCCIB2
P20	IO69NDB2V0
P21	GCA0/IO64NDB2V0
P22	VCCIB2
P23	GCB0/IO63NDB2V0
P24	GCB1/IO63PDB2V0
P25	IO66NDB2V0
P26	IO67PDB2V0
R1	NC
R2	VCCIB4
R3	IO103NDB4V0
R4	GND
R5	IO101PDB4V0
R6	IO100NPB4V0
R7	GND
R8	IO99PDB4V0
R9	IO97PDB4V0
R10	GND
R11	GND
R12	VCC
R13	GND
R14	VCC
R15	GND
R16	VCC
R17	GND
R18	GDB2/IO83PDB2V0
R19	IO78PDB2V0
R20	GND

Revision	Changes	Page
v2.0, Revision 1 (continued)	Table 3-6 • Package Thermal Resistance was updated to include new data.	3-7
	In EQ 4 to EQ 6, the junction temperature was changed from 110°C to 100°C.	3-8 to 3-8
	Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics are new and have replaced the Quiescent Supply Current Characteristics (IDDQ) table.	3-10 to 3-16
	In Table 3-14 • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices, the power supply for PAC9 and PAC10 were changed from VMV/VCC to VCCI.	3-22
	In Table 3-15 • Different Components Contributing to the Static Power Consumption in Fusion Devices, the power supply for PDC7 and PDC8 were changed from VMV/VCC to VCCI. PDC1 was updated from TBD to 18.	3-23
	The "QN108" table was updated to remove the duplicates of pins B12 and B34.	4-2
Preliminary v1.7 (October 2008)	The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.	
	For the VIL and VIH parameters, 0.30 * VCCI was changed to 0.35 * VCCI and 0.70 * VCCI was changed to 0.65 * VCCI in Table 2-126 • Minimum and Maximum DC Input and Output Levels.	2-193
	The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.	N/A
	The following updates were made to Table 2-141 • Minimum and Maximum DC Input and Output Levels: Temperature Digital Output 213 00 1111 1101 283 01 0001 1011 358 01 0110 0110 – only the digital output was updated. Temperature 358 remains in the temperature column.	2-200
	In Advance v1.2, the "VAREF Analog Reference Voltage" pin description was significantly updated but the change was not noted in the change table.	2-225
Advance v1.6 (August 2008)	The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA.	N/A
	The references to the *Peripherals User's Guide* in the "No-Glitch MUX (NGMUX)" section and "Voltage Regulator Power Supply Monitor (VRPSM)" section were changed to *Fusion Handbook*.	2-32, 2-42
Advance v1.5 (July 2008)	The following bullet was updated from High-Voltage Input Tolerance: ±12 V to High-Voltage Input Tolerance: 10.5 V to 12 V.	I
	The following bullet was updated from Programmable 1, 3, 10, 30 µA and 25 mA Drive Strengths to Programmable 1, 3, 10, 30 µA and 20 mA Drive Strengths.	I