

Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/p1afs1500-2fg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Fusion Device Family Overview

Instant On

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design.

Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.



Fusion Device Family Overview

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

- 1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
- 2. From the FlashPro GUI, click **PDB Configuration**. A FlashPoint Programming File Generator window appears.
- Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
- 4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-3).
- Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

1 - I/O is set to drive out logic High

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tri-State: I/O is tristated

Port Name	Macro Cell	Pin Number	1/O State (Output Only)
BIST	ADLIB:INBUF	T2	1
BYPASS_IO	ADLIB:INBUF	К1	1
CLK	ADLIB:INBUF	B1	1
ENOUT	ADLIB:INBUF	J16	1
LED	ADLIB:OUTBUF	M3	0
MONITOR[0]	ADLIB:OUTBUF	B5	0
MONITOR[1]	ADLIB:OUTBUF	C7	Z
MONITOR[2]	ADLIB:OUTBUF	D9	Z
MONITOR[3]	ADLIB:OUTBUF	D7	Z
MONITOR[4]	ADLIB:OUTBUF	A11	Z
OEa	ADLIB:INBUF	E4	Z
OEb	ADLIB:INBUF	F1	Z
OSC_EN	ADLIB:INBUF	К3	Z
PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
PAD[11]	ADLIB:BIBUF_LVCMOS33D	B7	Z
PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
PAD[14]	ADLIB:BIBUF LVCMOS33U	B6	7

Figure 1-3 • I/O States During Programming Window

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.



Array Coordinates

During many place-and-route operations in the Microsemi Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

VersaTiles					Memor	y Rows	All		
Device	Mi	n.	М	ax.	Bottom	Тор	Min.	Max.	
	x	У	x	У	(x, y)	(x, y)	(x, y)	(x, y)	
AFS090	3	2	98	25	None	(3, 26)	(0, 0)	(101, 29)	
AFS250	3	2	130	49	None	(3, 50)	(0, 0)	(133, 53)	
AFS600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)	
AFS1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 129)	

Table 2-3 • Array Coordinates







Routing Architecture

The routing structure of Fusion devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-8). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaNet global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire Fusion device (Figure 2-9 on page 2-9). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit loading effects.

The high-speed very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length ± 12 VersaTiles in the vertical direction and length ± 16 in the horizontal direction from a given core VersaTile (Figure 2-10 on page 2-10). Very long lines in Fusion devices, like those in ProASIC3 devices, have been enhanced. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-11 on page 2-11). These nets are typically used to distribute clocks, reset signals, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.





VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, Table 2-7, and Table 2-8 on page 2-17 present minimum and maximum global clock delays within the device Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

 Table 2-5 • AFS1500 Global Resource Timing

 Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Boromotor	Description		-2		-1		Std.	
Farameter			Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.53	1.75	1.74	1.99	2.05	2.34	ns
t _{RCKH}	Input High Delay for Global Clock	1.53	1.79	1.75	2.04	2.05	2.40	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-6 • AFS600 Global Resource Timing

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Paramotor	Description	-2		-1		Std.		Unite
Falailletei	Description		Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.27	1.49	1.44	1.70	1.69	2.00	ns
t _{RCKH}	Input High Delay for Global Clock	1.26	1.54	1.44	1.75	1.69	2.06	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.36	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Embedded Memories

Fusion devices include four types of embedded memory: flash block, FlashROM, SRAM, and FIFO.

Flash Memory Block

Fusion is the first FPGA that offers a flash memory block (FB). Each FB block stores 2 Mbits of data. The flash memory block macro is illustrated in Figure 2-32. The port pin name and descriptions are detailed on Table 2-19 on page 2-40. All flash memory block signals are active high, except for CLK and active low RESET. All flash memory operations are synchronous to the rising edge of CLK.



Figure 2-32 • Flash Memory Block

Program Operation

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, the total programming (including erase) time per page of the eNVM is 6.8 ms. While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified. Program errors include the following:

- 1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
- 2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
- Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
- 4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
- 5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
- 6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
- 7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in Figure 2-36.



Figure 2-36 • FB Program Waveform

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.



Unprotect Page Operation

An Unprotect Page operation will clear the protection for a page addressed on the ADDR input. It is initiated by setting the UNPROTECTPAGE signal on the interface along with the page address on ADDR.

If the page is not in the Page Buffer, the Unprotect Page operation will copy the page into the Page Buffer. The Copy Page operation occurs only if the current page in the Page Buffer is not Page Loss Protected.

The waveform for an Unprotect Page operation is shown in Figure 2-42.



Figure 2-42 • FB Unprotected Page Waveform

The Unprotect Page operation can incur the following error conditions:

- 1. If the copy of the page to the Page Buffer determines that the page has a single-bit correctable error in the data, it will report a STATUS = '01'.
- 2. If the address on ADDR does not match the address of the Page Buffer, PAGELOSSPROTECT is asserted, and the Page Buffer has been modified, then STATUS = '11' and the addressed page is not loaded into the Page Buffer.
- 3. If the copy of the page to the Page Buffer determines that at least one block in the page has a double-bit uncorrectable error, STATUS = '10' and the Page Buffer will contain the corrupted data.

Discard Page Operation

If the contents of the modified Page Buffer have to be discarded, the DISCARDPAGE signal should be asserted. This command results in the Page Buffer being marked as unmodified.

The timing for the operation is shown in Figure 2-43. The BUSY signal will remain asserted until the operation has completed.



Figure 2-43 • FB Discard Page Waveform

Channel Input Offset Error

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to $\frac{1}{2}$ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

Total Channel Error

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.



Figure 2-68 • Total Channel Error Example



Device Architecture

Gain Error

The gain error of an ADC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale (%FSR). Gain error is the full-scale error minus the offset error (Figure 2-84).



Figure 2-84 • Gain Error

Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.



EQ 16 through EQ 18 can be used to calculate the acquisition time required for a given input. The STC signal gives the number of sample periods in ADCCLK for the acquisition time of the desired signal. If the actual acquisition time is higher than the STC value, the settling time error can affect the accuracy of the ADC, because the sampling capacitor is only partially charged within the given sampling cycle. Example acquisition times are given in Table 2-44 and Table 2-45. When controlling the sample time for the ADC along with the use of the active bipolar prescaler, current monitor, or temperature monitor, the minimum sample time(s) for each must be obeyed. EQ 19 can be used to determine the appropriate value of STC.

You can calculate the minimum actual acquisition time by using EQ 16:

EQ 16

EQ 17

For 0.5 LSB gain error, VOUT should be replaced with (VIN –(0.5 × LSB Value)): (VIN – 0.5 × LSB Value) = VIN(1 – $e^{-t/RC}$)

$$1 - e^{-e^{-1}}$$

Solving EQ 17:

EQ 18

where $R = Z_{INAD} + R_{SOURCE}$ and $C = C_{INAD}$. Calculate the value of STC by using EQ 19.

t_{SAMPLE} = (2 + STC) x (1 / ADCCLK) or t_{SAMPLE} = (2 + STC) x (ADC Clock Period)

EQ 19

where ADCCLK = ADC clock frequency in MHz.

where VIN is the ADC reference voltage (VREF)

 t_{SAMPLE} = 0.449 µs from bit resolution in Table 2-44.

ADC Clock frequency = 10 MHz or a 100 ns period.

STC = (t_{SAMPLE} / (1 / 10 MHz)) - 2 = 4.49 - 2 = 2.49.

You must round up to 3 to accommodate the minimum sample time.

Table 2-44 • Acquisition Time Example with VAREF = 2.56 V

	VIN = 2.56V, R = 4K (R _{SOURCE} ~ 0), C = 18 pF			
Resolution	LSB Value (mV)	Min. Sample/Hold Time for 0.5 LSB (μs)		
8	10	0.449		
10	2.5	0.549		
12	0.625	0.649		

|--|

	VIN = 3.3V, R = 4	IK (R _{SOURCE} ~ 0), C = 18 pF
Resolution	LSB Value (mV)	Min. Sample/Hold time for 0.5 LSB (µs)
8	12.891	0.449
10	3.223	0.549
12	0.806	0.649

Sample Phase

A conversion is performed in three phases. In the first phase, the analog input voltage is sampled on the input capacitor. This phase is called sample phase. During the sample phase, the output signals BUSY and SAMPLE change from '0' to '1', indicating the ADC is busy and sampling the analog signal. The sample time can be controlled by input signals STC[7:0]. The sample time can be calculated by EQ 20. When controlling the sample time for the ADC along with the use of Prescaler or Current Monitor or Temperature Monitor, the minimum sample time for each must be obeyed.



Device Architecture

Table 2-49 • Analog Channel Specifications (continued)

Commercial Temperature Range Conditions, $T_J = 85^{\circ}C$ (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Digital Input us	ing Analog Pads AV, AC	and AT				
VIND ^{2,3}	Input Voltage	Refer to Table 3-2 on page 3-3				
VHYSDIN	Hysteresis			0.3		V
VIHDIN	Input High			1.2		V
VILDIN	Input Low			0.9		V
VMPWDIN	Minimum Pulse With		50			ns
F _{DIN}	Maximum Frequency				10	MHz
ISTBDIN	Input Leakage Current			2		μA
IDYNDIN	Dynamic Current			20		μA
t _{INDIN}	Input Delay			10		ns
Gate Driver Out	tput Using Analog Pad A	G				
VG	Voltage Range	Refer to Table 3-2 on page 3-3				
IG	Output Current Drive	High Current Mode ⁶ at 1.0 V			±20	mA
		Low Current Mode: ±1 µA	0.8	1.0	1.3	μA
		Low Current Mode: ±3 µA	2.0	2.7	3.3	μA
		Low Current Mode: ± 10 µA	7.4	9.0	11.5	μA
		Low Current Mode: ± 30 µA	21.0	27.0	32.0	μA
IOFFG	Maximum Off Current				100	nA
F _G	Maximum switching rate	High Current Mode ⁶ at 1.0 V, 1 k Ω resistive load		1.3		MHz
		Low Current Mode: ±1 μA, 3 MΩ resistive load		3		KHz
		Low Current Mode: ±3 μA, 1 MΩ resistive load		7		KHz
		Low Current Mode: $\pm 10 \ \mu$ A, 300 k Ω resistive load		25		KHz
		Low Current Mode: $\pm 30 \ \mu$ A, 105 k Ω resistive load		78		KHz

Notes:

1. VRSM is the maximum voltage drop across the current sense resistor.

2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.

3. VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.

4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.

- 5. The temperature offset is a fixed positive value.
- 6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
- 7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.

Analog Configuration MUX

The ACM is the interface between the FPGA, the Analog Block configurations, and the real-time counter. Microsemi Libero SoC will generate IP that will load and configure the Analog Block via the ACM. However, users are not limited to using the Libero SoC IP. This section provides a detailed description of the ACM's register map, truth tables for proper configuration of the Analog Block and RTC, as well as timing waveforms so users can access and control the ACM directly from their designs.

The Analog Block contains four 8-bit latches per Analog Quad that are initialized through the ACM. These latches act as configuration bits for Analog Quads. The ACM block runs from the core voltage supply (1.5 V).

Access to the ACM is achieved via 8-bit address and data busses with enables. The pin list is provided in Table 2-36 on page 2-78. The ACM clock speed is limited to a maximum of 10 MHz, more than sufficient to handle the low-bandwidth requirements of configuring the Analog Block and the RTC (sub-block of the Analog Block).

Table 2-54 decodes the ACM address space and maps it to the corresponding Analog Quad and configuration byte for that quad.

ACMADDR [7:0] in Decimal	Name	Description	Associated Peripheral	
0	-	_	Analog Quad	
1	AQ0	Byte 0	Analog Quad	
2	AQ0	Byte 1	Analog Quad	
3	AQ0	Byte 2	Analog Quad	
4	AQ0	Byte 3	Analog Quad	
5	AQ1	Byte 0	Analog Quad	
			Analog Quad	
	· ·	· · · ·		
36	AQ8	Byte 3	Analog Quad	
37	AQ9	Byte 0	Analog Quad	
38	AQ9	Byte 1	Analog Quad	
39	AQ9	Byte 2	Analog Quad	
40	AQ9	Byte 3	Analog Quad	
41		Undefined	Analog Quad	
		Undefined	Analog Quad	
	•			
63		Undefined	RTC	
64	COUNTER0	Counter bits 7:0	RTC	
65	COUNTER1	Counter bits 15:8	RTC	
66	COUNTER2	Counter bits 23:16	RTC	
67	COUNTER3	Counter bits 31:24	RTC	
68	COUNTER4	Counter bits 39:32	RTC	
72	MATCHREG0	Match register bits 7:0 RTC		

Table 2-54 • ACM Address Decode Table for Analog Quad

Table 2-68 • I/O Bank Support by Device

I/O Bank	AFS090	AFS250	AFS600	AFS1500
Standard I/O	Ν	Ν	_	-
Advanced I/O	E, W	E, W	E, W	E, W
Pro I/O	-	_	Ν	Ν
Analog Quad	S	S	S	S

Note: E = *East side of the device*

W = West side of the device

N = *North* side of the device

S = South side of the device

Table 2-69 • Fusion VCCI Voltages and Compatible Standards

VCCI (typical)	Compatible Standards
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II),* GTL+ 3.3, GTL 3.3,* LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II),* GTL+ 2.5,* GTL 2.5,* LVDS, BLVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I),* HSTL (Class II)*

Note: *I/O standard supported by Pro I/O banks.

Table 2-70 • Fusion VREF Voltages and Compatible Standards*

VREF (typical)	Compatible Standards
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

Note: *I/O standards supported by Pro I/O banks.

Table 2-82 • Advanced I/O Default Attributes

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	Refer to the following	Refer to the following tables	Off	None	35 pF	-
LVCMOS 2.5 V	information:	Table 2-78 on page 2-152	Off	None	35 pF	-
LVCMOS 2.5/5.0 V	Table 2-78 on page 2-152	Table 2-79 on page 2-152	Off	None	35 pF	-
LVCMOS 1.8 V	Table 2-79 on page 2-152	Table 2-80 on page 2-152	Off	None	35 pF	-
LVCMOS 1.5 V	Table 2-80 on page 2-152		Off	None	35 pF	-
PCI (3.3 V)			Off	None	10 pF	-
PCI-X (3.3 V)			Off	None	10 pF	-
LVDS, BLVDS, M-LVDS			Off	None	_	_
LVPECL			Off	None	-	-



Device Architecture

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

1.5 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
Applicable	to Pro I	/O Banks										
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable	to Adva	inced I/O Ban	iks						-	-		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable to Pro I/O Banks												
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-122 • AC Loading

Table 2-127 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.5	0.75	-	35

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.



User-Defined Supply Pins

VREF I/O Voltage Reference

Reference voltage for I/O minibanks. Both AFS600 and AFS1500 (north bank only) support Microsemi Pro I/O. These I/O banks support voltage reference standard I/O. The VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

VAREF Analog Reference Voltage

The Fusion device can be configured to generate a 2.56 V internal reference voltage that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREF pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF is internally generated by the Fusion device, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. Depending on the capacitor value selected in the Analog System Builder, a tool in Libero SoC, an automatic delay circuit will be generated using logic tiles available within the FPGA to ensure that VAREF has achieved the 2.56 V value. Microsemi recommends customers use 10 uF as the value of the bypass capacitor. Designers choosing to use an external VAREF need to ensure that a stable and clean VAREF source is supplied to the VAREF pin before initiating conversions by the ADC. Designers should also make sure that the ADCRESET signal is deasserted before initiating valid conversions.²

If the user connects VAREF to external 3.3 V on their board, the internal VAREF driving OpAmp tries to bring the pin down to the nominal 2.56 V until the device is programmed and up/functional. Under this scenario, it is recommended to connect an external 3.3 V supply through a ~1 KOhm resistor to limit current, along with placing a 10-100nF capacitor between VAREF and GNDA.

User Pins

I/O

User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are configured as inputs with pull-up resistors.

During programming, I/Os become tristated and weakly pulled up to VCCI. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os get instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

Axy Analog Input/Output

Analog I/O pin, where x is the analog pad type (C = current pad, G = Gate driver pad, T = Temperature pad, V = Voltage pad) and y is the Analog Quad number (0 to 9). There is a minimum 1 M Ω to ground on AV, AC, and AT. This pin can be left floating when it is unused.

^{2.} The ADC is functional with an external reference down to 1V, however to meet the performance parameters highlighted in the datasheet refer to the VAREF specification in Table 3-2 on page 3-3.



Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹ (continued)

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³					
Differential				•					
LVDS	-	2.5	7.74	88.92					
LVPECL	_	3.3	19.54	166.52					
Applicable to Standard I/O Bank	Applicable to Standard I/O Banks								
Single-Ended									
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	431.08					
2.5 V LVCMOS	35	2.5	-	247.36					
1.8 V LVCMOS	35	1.8	-	128.46					
1.5 V LVCMOS (JESD8-11)	35	1.5	-	89.46					

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.

2. PDC8 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.

Fusion Family of Mixed Signal FPGAs

	PQ208		PQ208			
Pin Number	AFS250 Function	AFS600 Function	Pin Number	AFS250 Function	AFS600 Function	
74	AV2	AV4	111	VCCNVM	VCCNVM	
75	AC2	AC4	112	VCC	VCC	
76	AG2	AG4	112	VCC	VCC	
77	AT2	AT4	113	VPUMP	VPUMP	
78	ATRTN1	ATRTN2	114	GNDQ	NC	
79	AT3	AT5	115	VCCIB1	ТСК	
80	AG3	AG5	116	ТСК	TDI	
81	AC3	AC5	117	TDI	TMS	
82	AV3	AV5	118	TMS	TDO	
83	AV4	AV6	119	TDO	TRST	
84	AC4	AC6	120	TRST	VJTAG	
85	AG4	AG6	121	VJTAG	IO57NDB2V0	
86	AT4	AT6	122	IO57NDB1V0	GDC2/IO57PDB2V0	
87	ATRTN2	ATRTN3	123	GDC2/IO57PDB1V0	IO56NDB2V0	
88	AT5	AT7	124	IO56NDB1V0	GDB2/IO56PDB2V0	
89	AG5	AG7	125	GDB2/IO56PDB1V0	IO55NDB2V0	
90	AC5	AC7	126	VCCIB1	GDA2/IO55PDB2V0	
91	AV5	AV7	127	GND	GDA0/IO54NDB2V0	
92	NC	AV8	128	IO55NDB1V0	GDA1/IO54PDB2V0	
93	NC	AC8	129	GDA2/IO55PDB1V0	VCCIB2	
94	NC	AG8	130	GDA0/IO54NDB1V0	GND	
95	NC	AT8	131	GDA1/IO54PDB1V0	VCC	
96	NC	ATRTN4	132	GDB0/IO53NDB1V0	GCA0/IO45NDB2V0	
97	NC	AT9	133	GDB1/IO53PDB1V0	GCA1/IO45PDB2V0	
98	NC	AG9	134	GDC0/IO52NDB1V0	GCB0/IO44NDB2V0	
99	NC	AC9	135	GDC1/IO52PDB1V0	GCB1/IO44PDB2V0	
100	NC	AV9	136	IO51NSB1V0	GCC0/IO43NDB2V	
101	GNDAQ	GNDAQ			0	
102	VCC33A	VCC33A	137	VCCIB1	GCC1/IO43PDB2V0	
103	ADCGNDREF	ADCGNDREF	138	GND	IO42NDB2V0	
104	VAREF	VAREF	139	VCC	IO42PDB2V0	
105	PUB	PUB	140	IO50NDB1V0	IO41NDB2V0	
106	VCC33A	VCC33A	141	IO50PDB1V0	GCC2/IO41PDB2V0	
107	GNDA	GNDA	142	GCA0/IO49NDB1V0	VCCIB2	
108	PTEM	PTEM	143	GCA1/IO49PDB1V0	GND	
109	PTBASE	PTBASE	144	GCB0/IO48NDB1V0	VCC	
110	GNDNVM	GNDNVM	145	GCB1/IO48PDB1V0	IO40NDB2V0	
L		L]	146	GCC0/IO47NDB1V0	GCB2/IO40PDB2V0	



Datasheet Information

Revision	Changes	Page
Advance v0.5	The low power modes of operation were updated and clarified.	N/A
(June 2006)	The AFS1500 digital I/O count was updated in Table 1 • Fusion Family.	i
	The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double- Ended (Analog)" table.	ii
	The "Voltage Regulator Power Supply Monitor (VRPSM)" was updated.	2-36
	Figure 2-45 • FlashROM Timing Diagram was updated.	2-53
	The "256-Pin FBGA" table for the AFS1500 is new.	3-12
Advance v0.4 (April 2006)	The G was moved in the "Product Ordering Codes" section.	III
Advance v0.3	The "Features and Benefits" section was updated.	I
(April 2006)	The "Fusion Family" table was updated.	I
	The "Package I/Os: Single-/Double-Ended (Analog)" table was updated.	П
	The "Product Ordering Codes" table was updated.	Ш
	The "Temperature Grade Offerings" table was updated.	IV
	The "General Description" section was updated to include ARM information.	1-1
	Figure 2-46 • FlashROM Timing Diagram was updated.	2-58
	The "FlashROM" section was updated.	2-57
	The "RESET" section was updated.	2-61
	The "RESET" section was updated.	2-64
	Figure 2-27 · Real-Time Counter System was updated.	2-35
	Table 2-19 • Flash Memory Block Pin Names was updated.	2-43
	Figure 2-33 • Flash Memory Block Diagram was updated to include AUX block information.	2-45
	Figure 2-34 • Flash Memory Block Organization was updated to include AUX block information.	2-46
	The note in the "Program Operation" section was updated.	2-48
	Figure 2-76 • Gate Driver Example was updated.	2-95
	The "Analog Quad ACM Description" section was updated.	2-130
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94
	Figure 2-65 • Analog Block Macro was updated.	2-81
	Figure 2-65 • Analog Block Macro was updated.	2-81
	The "Analog Quad" section was updated.	2-84
	The "Voltage Monitor" section was updated.	2-86
	The "Direct Digital Input" section was updated.	2-89
	The "Current Monitor" section was updated.	2-90
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94