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## Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

## Details

E·XFI

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/p1afs1500-2fg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## **Read Operation**

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer, or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-38) and Pipe Mode (Figure 2-39) reads of the flash memory block interface.



Figure 2-38 • Read Waveform (Non-Pipe Mode, 32-bit access)



Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access)

## Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- · Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-40 and Figure 2-41.



Figure 2-40 • Read Next Waveform (Non-Pipe Mode, 32-bit access)



*Figure 2-41* • Read Next WaveForm (Pipe Mode, 32-bit access)



Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.



Figure 2-47 • Fusion RAM Block with Embedded FIFO Controller





Figure 2-54 • One Port Write / Other Port Read Same



Figure 2-55 • RAM Reset. Applicable to both RAM4K9 and RAM512x18.

The diode's voltage is measured at each current level and the temperature is calculated based on EQ 7.

$$V_{\text{TMSLO}} - V_{\text{TMSHI}} = n \frac{kT}{q} \left( \ln \frac{I_{\text{TMSLO}}}{I_{\text{TMSHI}}} \right)$$

EQ 7

where

 $\textit{I}_{\textit{TMSLO}}$  is the current when the Temperature Strobe is Low, typically 100  $\mu A$ 

 $I_{TMSHI}$  is the current when the Temperature Strobe is High, typically 10  $\mu A$ 

*V<sub>TMSLO</sub>* is diode voltage while Temperature Strobe is Low

 $V_{TMSHI}$  is diode voltage while Temperature Strobe is High

n is the non-ideality factor of the diode-connected transistor. It is typically 1.004 for the Microsemirecommended transistor type 2N3904.

- $K = 1.3806 \text{ x } 10^{-23} \text{ J/K}$  is the Boltzman constant
- $Q = 1.602 \times 10^{-19} C$  is the charge of a proton

When  $I_{TMSLO} / I_{TMSHI} = 10$ , the equation can be simplified as shown in EQ 8.

$$\Delta V = V_{\text{TMSLO}} - V_{\text{TMSHI}} = 1.986 \times 10^{-4} nT$$

EQ 8

In the Fusion TMB, the ideality factor *n* for 2N3904 is 1.004 and  $\Delta V$  is amplified 12.5 times by an internal amplifier; hence the voltage before entering the ADC is as given in EQ 9.

$$V_{ADC} = \Delta V \times 12.5 = 2.5 \text{ mV}/(K \times T)$$

EQ 9

This means the temperature to voltage relationship is 2.5 mV per degree Kelvin. The unique design of Fusion has made the Temperature Monitor System simple for the user. When the 10-bit mode ADC is used, each LSB represents 1 degree Kelvin, as shown in EQ 10. That is, e. 25°C is equal to 293°K and is represented by decimal 293 counts from the ADC.

$$1K = 2.5 \text{ mV} \times \frac{2^{10}}{2.56 \text{ V}} = 1 \text{ LSB}$$

EQ 10

If 8-bit mode is used for the ADC resolution, each LSB represents 4 degrees Kelvin; however, the resolution remains as 1 degree Kelvin per LSB, even for 12-bit mode, due to the Temperature Monitor design. An example of the temperature data format for 10-bit mode is shown in Table 2-38.

Temperature	Temperature (K)	Digital Output (ADC 10-bit mode)
-40°C	233	00 1110 1001
–20°C	253	00 1111 1101
0°C	273	01 0001 0001
1°C	274	01 0001 0010
10 °C	283	01 0001 1011
25°C	298	01 0010 1010
50 °C	323	01 0100 0011
85 °C	358	01 0110 0110

Table 2-38 • Temperature Data Format

Fusion Family of Mixed Signal FPGAs

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 k $\Omega$  (or lower) output drive resistance at hot insertion, and 1 k $\Omega$  (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

- 1. Grounds
- 2. Powers, I/Os, other pins

## **Cold-Sparing Support**

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks and standard I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If Standard I/O banks are used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the standard I/O buffers do not have built-in I/O clamp diodes.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull down resistor and driven in the opposite direction. A small static current is induced on each IO pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Please refer to Table 2-95 on page 2-169, Table 2-96 on page 2-169, and Table 2-97 on page 2-171 for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTL 3.3 V, pull-up resistor is ~45 k $\Omega$  and the resulting current is equal to 3.3 V / 45 k $\Omega$  = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven low
- Input buffers with pull-down, driven high
- Bidirectional buffers with pull-up, driven low
- · Bidirectional buffers with pull-down, driven high
- Output buffers with pull-up, driven low
- Output buffers with pull-down, driven high
- Tristate buffers with pull-up, driven low
- · Tristate buffers with pull-down, driven high



Temporary overshoots are allowed according to Table 3-4 on page 3-4.



Figure 2-103 • Solution 1

## Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-4. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-104. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.



Figure 2-104 • Solution 2

## I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-84 and Table 2-85 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

Table 2-84 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)*	RES PULL	OUT_LOAD (output only)	COMBINE REGISTER
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3
PCI (3.3 V)			3		3	3
PCI-X (3.3 V)	3		3		3	3
LVDS, BLVDS, M-LVDS			3			3
LVPECL						3

Note: \* This feature does not apply to the standard I/O banks, which are the north I/O banks of AFS090 and AFS250 devices

## User I/O Naming Convention

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

- G = Global
- m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).
- n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-22 on page 2-25 shows the three input pins per clock source MUX at CCC location m.
- u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.
- x = P (Positive) or N (Negative) for differential pairs, or R (Regular single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as an LVPECL pair.
- w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

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B = Bank
```

- y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.
- V = Reference voltage
- z = Minibank number



## Standard I/O Bank

Figure 2-113 • Naming Conventions of Fusion Devices with Three Digital I/O Banks

## Table 2-99 • Short Current Event Duration before Failure

Temperature	Time Before Failure
-40°C	>20 years
0°C	>20 years
25°C	>20 years
70°C	5 years
85°C	2 years
100°C	6 months

## Table 2-100 • Schmitt Trigger Input Hysteresis Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

## Table 2-101 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/BLVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

Note: \* The maximum input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.

## SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

SSTL2 Class II		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
18 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	124	169	10	10

Table 2-159 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



## Figure 2-131 • AC Loading

#### Table 2-160 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

#### Timing Characteristics

## Table 2-161 • SSTL 2 Class II Commercial Temperature Range Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
Std.	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	4.01	ns
-1	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	3.41	ns
-2	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	2.99	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



## Table 2-174 • Parameter Definitions and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t <sub>OCLKQ</sub>	Clock-to-Q of the Output Data Register	H, DOUT
tosud	Data Setup Time for the Output Data Register	F, H
t <sub>OHD</sub>	Data Hold Time for the Output Data Register	F, H
t <sub>OSUE</sub>	Enable Setup Time for the Output Data Register	G, H
t <sub>OHE</sub>	Enable Hold Time for the Output Data Register	G, H
t <sub>OPRE2Q</sub>	Asynchronous Preset-to-Q of the Output Data Register	L,DOUT
t <sub>OREMPRE</sub>	Asynchronous Preset Removal Time for the Output Data Register	L, H
t <sub>ORECPRE</sub>	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t <sub>OECLKQ</sub>	Clock-to-Q of the Output Enable Register	H, EOUT
t <sub>OESUD</sub>	Data Setup Time for the Output Enable Register	J, H
t <sub>OEHD</sub>	Data Hold Time for the Output Enable Register	J, H
t <sub>OESUE</sub>	Enable Setup Time for the Output Enable Register	K, H
t <sub>OEHE</sub>	Enable Hold Time for the Output Enable Register	K, H
t <sub>OEPRE2Q</sub>	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
t <sub>OEREMPRE</sub>	Asynchronous Preset Removal Time for the Output Enable Register	I, H
t <sub>OERECPRE</sub>	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t <sub>ICLKQ</sub>	Clock-to-Q of the Input Data Register	A, E
t <sub>ISUD</sub>	Data Setup Time for the Input Data Register	C, A
t <sub>IHD</sub>	Data Hold Time for the Input Data Register	C, A
t <sub>ISUE</sub>	Enable Setup Time for the Input Data Register	B, A
t <sub>IHE</sub>	Enable Hold Time for the Input Data Register	B, A
t <sub>IPRE2Q</sub>	Asynchronous Preset-to-Q of the Input Data Register	D, E
t <sub>IREMPRE</sub>	Asynchronous Preset Removal Time for the Input Data Register	D, A
t <sub>IRECPRE</sub>	Asynchronous Preset Recovery Time for the Input Data Register	D, A

*Note:* \*See Figure 2-137 on page 2-212 for more information.



Device Architecture

## Table 2-175 • Parameter Definitions and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t <sub>oclkq</sub>	Clock-to-Q of the Output Data Register	HH, DOUT
t <sub>OSUD</sub>	Data Setup Time for the Output Data Register	FF, HH
t <sub>OHD</sub>	Data Hold Time for the Output Data Register	FF, HH
t <sub>OSUE</sub>	Enable Setup Time for the Output Data Register	GG, HH
t <sub>OHE</sub>	Enable Hold Time for the Output Data Register	GG, HH
t <sub>OCLR2Q</sub>	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
t <sub>OREMCLR</sub>	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
t <sub>ORECCLR</sub>	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t <sub>oeclkq</sub>	Clock-to-Q of the Output Enable Register	HH, EOUT
t <sub>OESUD</sub>	Data Setup Time for the Output Enable Register	JJ, HH
t <sub>OEHD</sub>	Data Hold Time for the Output Enable Register	JJ, HH
t <sub>OESUE</sub>	Enable Setup Time for the Output Enable Register	КК, НН
t <sub>OEHE</sub>	Enable Hold Time for the Output Enable Register	KK, HH
t <sub>OECLR2Q</sub>	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
t <sub>OEREMCLR</sub>	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
t <sub>OERECCLR</sub>	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t <sub>ICLKQ</sub>	Clock-to-Q of the Input Data Register	AA, EE
t <sub>ISUD</sub>	Data Setup Time for the Input Data Register	CC, AA
t <sub>IHD</sub>	Data Hold Time for the Input Data Register	CC, AA
t <sub>ISUE</sub>	Enable Setup Time for the Input Data Register	BB, AA
t <sub>IHE</sub>	Enable Hold Time for the Input Data Register	BB, AA
t <sub>ICLR2Q</sub>	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
t <sub>IREMCLR</sub>	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
tIRECCLR	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note:* \*See Figure 2-138 on page 2-214 for more information.

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T <sub>J</sub> = 0°C	FPGA/FlashROM	500	20 years
	Max. T <sub>J</sub> = 85°C	Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years
Industrial	Min. T <sub>J</sub> = –40°C	FPGA/FlashROM	500	20 years
	Max. T <sub>J</sub> = 100°C	Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

## Table 3-5 • FPGA Programming, Storage, and Operating Limits

# I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every Fusion device. These circuits ensure easy transition from the powered off state to the powered up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1 on page 3-6.

There are five regions to consider during power-up.

Fusion I/Os are activated only if ALL of the following three conditions are met:

- 1. VCC and VCCI are above the minimum specified trip points (Figure 3-1).
- 2. VCCI > VCC 0.75 V (typical).
- 3. Chip is in the operating mode.

## V<sub>CCI</sub> Trip Point:

Ramping up: 0.6 V < trip\_point\_up < 1.2 V

Ramping down: 0.5 V < trip\_point\_down < 1.1 V

## V<sub>CC</sub> Trip Point:

Ramping up: 0.6 V < trip\_point\_up < 1.1 V

Ramping down: 0.5 V < trip\_point\_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

## Internal Power-Up Activation Sequence

- 1. Core
- 2. Input buffers
- 3. Output buffers, after 200 ns delay from input buffer activation

## PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper powerup behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels. The  $V_{CC}$  activation level is specified as 1.1 V worst-case (see Figure 3-1 on page 3-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V  $\pm$  0.25 V), the PLL output lock signal goes low and/or the output clock is lost.

## Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings<sup>1</sup>

	C <sub>LOAD</sub> (pF)	VCCI (V)	Static Power PDC8 (mW) <sup>2</sup>	Dynamic Power PAC10 (µW/MHz) <sup>3</sup>
Applicable to Pro I/O Banks				
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	-	474.70
2.5 V LVCMOS	35	2.5	-	270.73
1.8 V LVCMOS	35	1.8	-	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	-	104.55
3.3 V PCI	10	3.3	-	204.61
3.3 V PCI-X	10	3.3	-	204.61
Voltage-Referenced	•			
3.3 V GTL	10	3.3	-	24.08
2.5 V GTL	10	2.5	-	13.52
3.3 V GTL+	10	3.3	-	24.10
2.5 V GTL+	10	2.5	-	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential	•	•		
LVDS	-	2.5	7.70	89.62
LVPECL	-	3.3	19.42	168.02
Applicable to Advanced I/O Ban	ks	•		
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	468.67
2.5 V LVCMOS	35	2.5	-	267.48
1.8 V LVCMOS	35	1.8	-	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	-	103.12
3.3 V PCI	10	3.3	-	201.02
3.3 V PCI-X	10	3.3	-	201.02

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.

2. PDC8 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.



 $P_{S-CELL}$  =  $N_{S-CELL}$  \* (PAC5 + ( $\alpha_1$  / 2) \* PAC6) \*  $F_{CLK}$ 

N<sub>S-CELL</sub> is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

 $\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

F<sub>CLK</sub> is the global clock signal frequency.

## Standby Mode and Sleep Mode

 $P_{S-CELL} = 0 W$ 

## Combinatorial Cells Dynamic Contribution—P<sub>C-CELL</sub>

## **Operating Mode**

 $P_{C-CELL} = N_{C-CELL} * (\alpha_1 / 2) * PAC7 * F_{CLK}$ 

N<sub>C-CELL</sub> is the number of VersaTiles used as combinatorial modules in the design.

 $\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

F<sub>CLK</sub> is the global clock signal frequency.

## Standby Mode and Sleep Mode

 $P_{C-CELL} = 0 W$ 

Routing Net Dynamic Contribution-PNET

#### **Operating Mode**

 $P_{NET} = (N_{S-CELL} + N_{C-CELL}) * (\alpha_1 / 2) * PAC8 * F_{CLK}$ 

N<sub>S-CELL</sub> is the number VersaTiles used as sequential modules in the design.

N<sub>C-CELL</sub> is the number of VersaTiles used as combinatorial modules in the design.

 $\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-16 on page 3-27.

F<sub>CLK</sub> is the global clock signal frequency.

## Standby Mode and Sleep Mode

 $P_{NET} = 0 W$ 

## I/O Input Buffer Dynamic Contribution—PINPUTS

## **Operating Mode**

 $P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$ 

N<sub>INPUTS</sub> is the number of I/O input buffers used in the design.

 $\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in Table 3-16 on page 3-27.

F<sub>CLK</sub> is the global clock signal frequency.

## Standby Mode and Sleep Mode

P<sub>INPUTS</sub> = 0 W

## I/O Output Buffer Dynamic Contribution—POUTPUTS

## **Operating Mode**

 $\mathsf{P}_{\mathsf{OUTPUTS}} = \mathsf{N}_{\mathsf{OUTPUTS}} * (\alpha_2 / 2) * \beta_1 * \mathsf{PAC10} * \mathsf{F}_{\mathsf{CLK}}$ 

N<sub>OUTPUTS</sub> is the number of I/O output buffers used in the design.

 $\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in Table 3-16 on page 3-27.

 $\beta_1$  is the I/O buffer enable rate—guidelines are provided in Table 3-17 on page 3-27.

F<sub>CLK</sub> is the global clock signal frequency.

## Standby Mode and Sleep Mode

P<sub>OUTPUTS</sub> = 0 W



## Total Static Power Consumption—PSTAT

Number of Quads used:  $N_{QUADS} = 4$ Number of NVM blocks available (AFS600):  $N_{NVM-BLOCKS} = 2$ Number of input pins used:  $N_{INPUTS} = 30$ Number of output pins used:  $N_{OUTPUTS} = 40$ 

## **Operating Mode**

 $\mathsf{P}_{\mathsf{STAT}} = \mathsf{PDC1} + (\mathsf{N}_{\mathsf{NVM-BLOCKS}} * \mathsf{PDC4}) + \mathsf{PDC5} + (\mathsf{N}_{\mathsf{QUADS}} * \mathsf{PDC6}) + (\mathsf{N}_{\mathsf{INPUTS}} * \mathsf{PDC7}) + (\mathsf{N}_{\mathsf{OUTPUTS}} * \mathsf{PDC8})$ 

P<sub>STAT</sub> = 7.50 mW + (2 \* 1.19 mW) + 8.25 mW + (4 \* 3.30 mW) + (30 \* 0.00) + (40 \* 0.00)

P<sub>STAT</sub> = 31.33 mW

## Standby Mode

P<sub>STAT</sub> = PDC2

 $P_{STAT}$  = 0.03 mW

## Sleep Mode

 $P_{STAT} = PDC3$ 

 $P_{STAT} = 0.03 \text{ mW}$ 

## Total Power Consumption—PTOTAL

In operating mode, the total power consumption of the device is 174.39 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$ 

P<sub>TOTAL</sub> = 143.06 mW + 31.33 mW

P<sub>TOTAL</sub> = 174.39 mW

In standby mode, the total power consumption of the device is limited to 0.66 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$ 

 $P_{TOTAL} = 0.03 \text{ mW} + 0.63 \text{ mW}$ 

 $P_{TOTAL} = 0.66 \text{ mW}$ 

In sleep mode, the total power consumption of the device drops as low as 0.03 mW:

 $P_{TOTAL} = P_{STAT} + P_{DYN}$  $P_{TOTAL} = 0.03 \text{ mW}$ 



Datasheet Information

Revision	Changes	Page
v2.0, Revision 1 (July 2009)	The MicroBlade and Fusion datasheets have been combined. Pigeon Point information is new.	N/A
	CoreMP7 support was removed since it is no longer offered.	
	–F was removed from the datasheet since it is no longer offered.	
	The operating temperature was changed from ambient to junction to better reflect actual conditions of operations.	
	Commercial: 0°C to 85°C	
	Industrial: –40°C to 100°C	
	The version number category was changed from Preliminary to Production, which means the datasheet contains information based on final characterization. The version number changed from Preliminary v1.7 to v2.0.	
	The "Integrated Analog Blocks and Analog I/Os" section was updated to include a reference to the "Analog System Characteristics" section in the <i>Device Architecture</i> chapter of the datasheet, which includes Table 2-46 • Analog Channel Specifications and specific voltage data.	1-4
	The phrase "Commercial-Case Conditions" in timing table titles was changed to "Commercial Temperature Range Conditions."	N/A
	The "Crystal Oscillator" section was updated significantly. Please review carefully.	2-20
	The "Real-Time Counter (part of AB macro)" section was updated significantly. Please review carefully.	2-33
	There was a typo in Table 2-19 • Flash Memory Block Pin Names for the ERASEPAGE description; it was the same as DISCARDPAGE. As as a result, the ERASEPAGE description was updated.	2-40
	The $t_{\mbox{FMAXCLKNVM}}$ parameter was updated in Table 2-25 $\bullet$ Flash Memory Block Timing.	2-52
	Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated.	2-66
	In Table 2-36 • Analog Block Pin Description, the Function description for PWRDWN was changed from "Comparator power-down if 1"	2-78
	to "ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin."	
	Figure 2-75 • Gate Driver Example was updated.	2-91
	The "ADC Operation" section was updated. Please review carefully.	2-104
	Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram are new.	2-113
	The "Typical Performance Characteristics" section is new.	2-115
	Table 2-49 • Analog Channel Specifications was significantly updated.	2-117
	Table 2-50 • ADC Characteristics in Direct Input Mode was significantly updated.	2-120
	In Table 2-52 • Calibrated Analog Channel Accuracy 1,2,3, note 2 was updated.	2-123
	In Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages, note 1 was updated.	2-124
	In Table 2-54 • ACM Address Decode Table for Analog Quad, bit 89 was removed.	2-126



Datasheet Information

Revision	Changes	Page
Advance v1.0 (January 2008)	All Timing Characteristics tables were updated. For the Differential I/O Standards, the Standard I/O support tables are new.	N/A
	Table 2-3 • Array Coordinates was updated to change the max x and y values	2-9
	Table 2-12 • Fusion CCC/PLL Specification was updated.	2-31
	A note was added to Table 2-16 · RTC ACM Memory Map.	2-37
	A reference to the Peripheral's User's Guide was added to the "Voltage Regulator Power Supply Monitor (VRPSM)" section.	2-42
	In Table 2-25 • Flash Memory Block Timing, the commercial conditions were updated.	2-55
	In Table 2-26 • FlashROM Access Time, the commercial conditions were missing and have been added below the title of the table.	2-58
	In Table 2-36 • Analog Block Pin Description, the function description was updated for the ADCRESET.	2-82
	In the "Voltage Monitor" section, the following sentence originally had $\pm$ 10% and it was changed to +10%.	2-86
	The Analog Quad inputs are tolerant up to 12 V + 10%.	
	In addition, this statement was deleted from the datasheet:	
	Each I/O will draw power when connected to power (3 mA at 3 V).	0.00
	The "Terminology" section is new.	2-88
	The "Current Monitor" section was significantly updated. Figure 2-72 • Timing Diagram for Current Monitor Strobe to Figure 2-74 • Negative Current Monitor and Table 2-37 • Recommended Resistor for Different Current Range Measurement are new.	2-90
	The "ADC Description" section was updated to add the "Terminology" section.	2-93
	In the "Gate Driver" section, 25 mA was changed to 20 mA and 1.5 MHz was changed to 1.3 MHz. In addition, the following sentence was deleted: The maximum AG pad switching frequency is 1.25 MHz.	2-94
	The "Temperature Monitor" section was updated to rewrite most of the text and add Figure 2-78, Figure 2-79, and Table 2-38 • Temperature Data Format.	2-96
	In Table 2-38 • Temperature Data Format, the temperature K column was changed for 85°C from 538 to 358.	2-98
	In Table 2-45 • ADC Interface Timing, "Typical-Case" was changed to "Worst-Case."	2-110
	The "ADC Interface Timing" section is new.	2-110
	Table 2-46 • Analog Channel Specifications was updated.	2-118
	The "V <sub>CC15A</sub> Analog Power Supply (1.5 V)" section was updated.	2-224
	The "V <sub>CCPLA/B</sub> PLL Supply Voltage" section is new.	2-225
	In "V $_{\rm CCNVM}$ Flash Memory Block Power Supply (1.5 V)" section, supply was changed to supply input.	2-224
	The "V_{CCPLAVB} PLL Supply Voltage" pin description was updated to include the following statement:	2-225
	Actel recommends tying VCCPLX to VCC and using proper filtering circuits to decouple $V_{CC}$ noise from PLL.	
	The "V <sub>COMPLA/B</sub> Ground for West and East PLL" section was updated.	2-225

Fusion Family of Mixed Signal FPGAs

Revision	Changes	Page
Advance v0.6 (continued)	The "Analog-to-Digital Converter Block" section was updated with the following statement: "All results are MSB justified in the ADC."	2-99
	The information about the ADCSTART signal was updated in the "ADC Description" section.	2-102
	Table 2-46 · Analog Channel Specifications was updated.	2-118
	Table 2-47 · ADC Characteristics in Direct Input Mode was updated.	2-121
	Table 2-51 • ACM Address Decode Table for Analog Quad was updated.	2-127
	In Table 2-53 • Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated.	2-130
	The "Introduction" section was updated to include information about digital inputs, outputs, and bibufs.	2-133
	In Table 2-69 • Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features:	2-137
	Single-ended receiver	
	Voltage-referenced differential receiver	
	The "liker I/O Naming Convention" section was undeted to include "V/" and "r"	2 150
	descriptions	2-159
	The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and $V_{CCI}$ pins within a given I/O bank.	2-185
	The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTEM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090.	3-8