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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/p1afs1500-2fg484

Email: info@E-XFL.COM

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Timing Characteristics

Table 2-1 • Combinatorial Cell Propagation DelaysCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	Units
INV	Y = !A	t _{PD}	0.40	0.46	0.54	ns
AND2	$Y = A \cdot B$	t _{PD}	0.47	0.54	0.63	ns
NAND2	$Y = !(A \cdot B)$	t _{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t _{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t _{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t _{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t _{PD}	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	t _{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t _{PD}	0.51	0.58	0.68	ns
AND3	$Y = A \cdot B \cdot C$	t _{PD}	0.56	0.64	0.75	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library (Figure 2-5). For more details, refer to the *IGLOO*, *ProASIC3*, *SmartFusion and Fusion Macro Library Guide*.



Figure 2-5 • Sample of Sequential Cells



VersaNet Global Networks and Spine Access

The Fusion architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles on the Fusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 180 internal/external clocks (in an AFS1500 device) or other high-fanout nets in Fusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on Fusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-12 on page 2-12).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the Fusion device (the "scope" of the spine; see Figure 2-11 on page 2-11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device. For details on using spines in Fusion devices, see the application note *Using Global Resources in Actel Fusion Devices*.



Figure 2-13 • Spine-Selection MUX of Global Tree



Table 2-7 • AFS250 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	_	·2	-	-1	St	Unite	
	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.89	1.12	1.02	1.27	1.20	1.50	ns
t _{RCKH}	Input High Delay for Global Clock	0.88	1.14	1.00	1.30	1.17	1.53	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.30		0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-8 • AFS090 Global Resource Timing

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-	2	-	1	S	Unite	
	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.84	1.07	0.96	1.21	1.13	1.43	ns
t _{RCKH}	Input High Delay for Global Clock	0.83	1.10	0.95	1.25	1.12	1.47	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.27		0.30		0.36	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[2:0] package pins. Refer to Figure 2-22 on page 2-25 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL feedback loop can be driven either internally or externally. The PLL macro also provides power-down input and lock output signals. During power-up, POWERDOWN should be asserted Low until VCC is up. See Figure 2-19 on page 2-23 for more information.

Inputs:

- · CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is power-down on (active low).

Outputs:

- LOCK (active high): indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-23 on page 2-26 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global networks, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate it from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, available with the Libero SoC and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select where the input clock is coming from. SmartGen automatically instantiates the special macro, PLLINT, when needed.



Table 2-25 • Flash Memory Block Timing (continued)Commercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{SUPGLOSSPRO}	Page Loss Protect Setup Time for the Control Logic	1.69	1.93	2.27	ns
t _{HDPGLOSSPRO}	Page Loss Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUPGSTAT}	Page Status Setup Time for the Control Logic	2.49	2.83	3.33	ns
t _{HDPGSTAT}	Page Status Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUOVERWRPG}	Over Write Page Setup Time for the Control Logic	1.88	2.14	2.52	ns
t _{HDOVERWRPG}	Over Write Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SULOCKREQUEST}	Lock Request Setup Time for the Control Logic	0.87	0.99	1.16	ns
t _{HDLOCKREQUEST}	Lock Request Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{RECARNVM}	Reset Recovery Time	0.94	1.07	1.25	ns
t _{REMARNVM}	Reset Removal Time	0.00	0.00	0.00	ns
t _{mpwarnvm}	Asynchronous Reset Minimum Pulse Width for the Control Logic	10.00	12.50	12.50	ns
t _{MPWCLKNVM}	Clock Minimum Pulse Width for the Control Logic	4.00	5.00	5.00	ns
+	Maximum Frequency for Clock for the Control Logic – for AFS1500/AFS600	80.00	80.00	80.00	MHz
'FMAXCLKNVM	Maximum Frequency for Clock for the Control Logic – for AFS250/AFS090	100.00	80.00	80.00	MHz

FlashROM

Fusion devices have 1 kbit of on-chip nonvolatile flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in eight banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read-back of the FlashROM from the FPGA core (Figure 2-45).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports a synchronous read and can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

The maximum FlashROM access clock is given in Table 2-26 on page 2-54. Figure 2-46 shows the timing behavior of the FlashROM access cycle—the address has to be set up on the rising edge of the clock for DOUT to be valid on the next falling edge of the clock.

If the address is unchanged for two cycles:

- D0 becomes invalid t_{CK2Q} ns after the second rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the second falling edge.

If the address unchanged for three cycles:

- D0 becomes invalid t_{CK2Q} ns after the second rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the second falling edge.
- D0 becomes invalid t_{CK2Q} ns after the third rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the third falling edge.

The following signals are used to configure the RAM4K9 memory element.

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-27).

|--|

WIDTHA1, WIDTHA0	WIDTHB1, WIDTHB0	D×W								
00	00	4k×1								
01 01 2k×2										
10	10	1k×4								
11	11	512×9								
Note: The aspect ratio settings are constant and cannot be changed on the fly.										

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the corresponding port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write mode for the respective ports. A Low on these signals indicates a write operation, and a High indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A Low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A High indicates a pipelined, read and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A Low on these signals makes the output retain data from the previous read. A High indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the output to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-28).

Table 2-28 • Address Pins Unused/Used for Various Supported Bus Widths

D×W	ADDRx									
	Unused	Used								
4k×1	None	[11:0]								
2k×2	[11]	[10:0]								
1k×4	[11:10]	[9:0]								
512×9	[11:9]	[8:0]								

Note: The "x" in ADDRx implies A or B.

Signal Name	Number of Bits	Direction	Function	Location of Details
AG6	1	Output		Analog Quad
AT6	1	Input		Analog Quad
ATRETURN67	1	Input	Temperature monitor return shared by Analog Quads 6 and 7	Analog Quad
AV7	1	Input	Analog Quad 7	Analog Quad
AC7	1	Input		Analog Quad
AG7	1	Output		Analog Quad
AT7	1	Input		Analog Quad
AV8	1	Input	Analog Quad 8	Analog Quad
AC8	1	Input		Analog Quad
AG8	1	Output		Analog Quad
AT8	1	Input		Analog Quad
ATRETURN89	1	Input	Temperature monitor return shared by Analog Quads 8 and 9	Analog Quad
AV9	1	Input	Analog Quad 9	Analog Quad
AC9	1	Input		Analog Quad
AG9	1	Output		Analog Quad
AT9	1	Input		Analog Quad
RTCMATCH	1	Output	МАТСН	RTC
RTCPSMMATCH	1	Output	MATCH connected to VRPSM	RTC
RTCXTLMODE[1:0]	2	Output	Drives XTLOSC RTCMODE[1:0] pins	RTC
RTCXTLSEL	1	Output	Drives XTLOSC MODESEL pin	RTC
RTCCLK	1	Input	RTC clock input	RTC

Table 2-36 • Analog Block Pin Description (continued)

Analog Quad

With the Fusion family, Microsemi introduces the Analog Quad, shown in Figure 2-65 on page 2-81, as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending it to the ADC for conversion into a digital signal. To maximize the usefulness of the Analog Quad, the analog input signals can also be configured as LVTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block, and its input pin is named AV. It contains a twochannel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler can be configured to accept analog signals between -12 V and 0 or between 0 and +12 V. The prescaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin can also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than 1 Ω) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage that can then be read using the ADC.

Channel Input Offset Error

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to $\frac{1}{2}$ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

Total Channel Error

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.



Figure 2-68 • Total Channel Error Example

There are several popular ADC architectures, each with advantages and limitations.

The analog-to-digital converter in Fusion devices is a switched-capacitor Successive Approximation Register (SAR) ADC. It supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (ksps). Built-in bandgap circuitry offers 1% internal voltage reference accuracy or an external reference voltage can be used.

As shown in Figure 2-81, a SAR ADC contains N capacitors with binary-weighted values.



Figure 2-81 • Example SAR ADC Architecture

To begin a conversion, all of the capacitors are quickly discharged. Then VIN is applied to all the capacitors for a period of time (acquisition time) during which the capacitors are charged to a value very close to VIN. Then all of the capacitors are switched to ground, and thus –VIN is applied across the comparator. Now the conversion process begins. First, C is switched to VREF Because of the binary weighting of the capacitors, the voltage at the input of the comparator is then shown by EQ 11.

Voltage at input of comparator = -VIN + VREF / 2

EQ 11

If VIN is greater than VREF / 2, the output of the comparator is 1; otherwise, the comparator output is 0. A register is clocked to retain this value as the MSB of the result. Next, if the MSB is 0, C is switched back to ground; otherwise, it remains connected to VREF, and C / 2 is connected to VREF. The result at the comparator input is now either –VIN + VREF / 4 or –VIN + 3 VREF / 4 (depending on the state of the MSB), and the comparator output now indicates the value of the next most significant bit. This bit is likewise registered, and the process continues for each subsequent bit until a conversion is complete. The conversion process requires some acquisition time plus N + 1 ADC clock cycles to complete.



Table 2-92 • Summary of I/O Timing Characteristics – Software Default SettingsCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V,Worst-Case VCCI = I/O Standard DependentApplicable to Pro I/Os

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t DOUT	top	t _{DIN}	tpy	t _{PY} S	teour	tzı	tzh	tız	tHz	tzıs	tzHS	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35	-	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
2.5 V LVCMOS	12 mA	High	35	-	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
1.8 V LVCMOS	12 mA	High	35	_	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
1.5 V LVCMOS	12 mA	High	35	_	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
3.3 V PCI	Per PCI spec	High	10	25 ²	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 ²	0.49	2.09	0.03	0.77	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V GTL	20 mA	High	10	25	0.49	1.55	0.03	2.19	_	0.32	1.52	1.55	0.00	0.00	3.19	3.22	ns
2.5 V GTL	20 mA	High	10	25	0.49	1.59	0.03	1.83	-	0.32	1.61	1.59	0.00	0.00	3.28	3.26	ns
3.3 V GTL+	35 mA	High	10	25	0.49	1.53	0.03	1.19	_	0.32	1.56	1.53	0.00	0.00	3.23	3.20	ns
2.5 V GTL+	33 mA	High	10	25	0.49	1.65	0.03	1.13	_	0.32	1.68	1.57	0.00	0.00	3.35	3.24	ns
HSTL (I)	8 mA	High	20	50	0.49	2.37	0.03	1.59	_	0.32	2.42	2.35	0.00	0.00	4.09	4.02	ns
HSTL (II)	15 mA	High	20	25	0.49	2.26	0.03	1.59	_	0.32	2.30	2.03	0.00	0.00	3.97	3.70	ns
SSTL2 (I)	17 mA	High	30	50	0.49	1.59	0.03	1.00	_	0.32	1.62	1.38	0.00	0.00	3.29	3.05	ns
SSTL2 (II)	21 mA	High	30	25	0.49	1.62	0.03	1.00	-	0.32	1.65	1.32	0.00	0.00	3.32	2.99	ns
SSTL3 (I)	16 mA	High	30	50	0.49	1.72	0.03	0.93	-	0.32	1.75	1.37	0.00	0.00	3.42	3.04	ns
SSTL3 (II)	24 mA	High	30	25	0.49	1.54	0.03	0.93	_	0.32	1.57	1.25	0.00	0.00	3.24	2.92	ns
LVDS	24 mA	High	_	_	0.49	1.57	0.03	1.36	_	_	_	_	_	_	_	_	ns
LVPECL	24 mA	High	-	-	0.49	1.60	0.03	1.22	1	_	_	-	-	_	_	-	ns

Notes:

1. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-7 for derating values.

2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-123 on page 2-197 for connectivity. This resistor is not required during normal operation.

Table 2-114 • 2.5 V LVCMOS Low Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Advanced I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
4 mA	Std.	0.66	11.40	0.04	1.31	0.43	11.22	11.40	2.68	2.20	13.45	13.63	ns
	-1	0.56	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	-2	0.49	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
8 mA	Std.	0.66	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	-1	0.56	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	-2	0.49	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
12 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	-1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	-2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
16 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	-1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	-2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
24 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	-1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	-2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

1.5 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
Applicable	to Pro I	/O Banks								1		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable	to Adva	inced I/O Ban	iks						-	-		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable	to Pro I	/O Banks							-	-		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-122 • AC Loading

Table 2-127 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.5	0.75	-	35

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.



3 – DC and Power Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-3.

Symbol	Parameter	Commercial	Industrial	Units	
VCC	DC core supply voltage	-0.3 to 1.65	–0.3 to 1.65	V	
VJTAG	JTAG DC voltage	-0.3 to 3.75	-0.3 to 3.75	V	
VPUMP	Programming voltage	-0.3 to 3.75	-0.3 to 3.75	V	
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	-0.3 to 1.65	V	
VCCI	DC I/O output buffer supply voltage	-0.3 to 3.75	-0.3 to 3.75	V	
VI	I/O input voltage ¹	 -0.3 V to 3.6 V (when I/O hot insertion mode is enabled) -0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) 			
VCC33A	+3.3 V power supply	–0.3 to 3.75 ²	–0.3 to 3.75 ²	V	
VCC33PMP	+3.3 V power supply	-0.3 to 3.75 ²	-0.3 to 3.75 ²	V	
VAREF	Voltage reference for ADC	-0.3 to 3.75	-0.3 to 3.75	V	
VCC15A	Digital power supply for the analog system	-0.3 to 1.65	–0.3 to 1.65	V	
VCCNVM	Embedded flash power supply	-0.3 to 1.65	-0.3 to 1.65	V	
VCCOSC	Oscillator power supply	-0.3 to 3.75	-0.3 to 3.75	V	

Table 3-1 • Absolute Maximum Ratings

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-4.

2. Analog data not valid beyond 3.65 V.

3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.

4. For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.

Parameter	Description	Conditions	Temp.	Min	Тур	Мах	Unit
ICC ¹	1.5 V quiescent current	Operational standby ⁴ ,	T _J = 25°C		5	7.5	mA
		VCC = 1.575 V	T _J = 85°C		6.5	20	mA
			T _J = 100°C		14	48	mA
		Standby mode ⁵ or Sleep mode ⁶ , V _{CC} = 0 V			0	0	μA
ICC33 ²	3.3 V analog supplies	Operational standby ⁴ ,	T _J = 25°C		9.8	12	mA
	current	VCC33 = 3.63 V	T _J = 85°C		9.8	12	mA
			T _J = 100°C		10.7	15	mA
		Operational standby, only	T _J = 25°C		0.30	2	mA
		output ON, VCC33 = 3.63 V	T _J = 85°C		0.30	2	mA
			T _J = 100°C		0.45	2	mA
		Standby mode ⁵ , VCC33 = 3.63 V	T _J = 25°C		2.9	2.9	mA
			T _J = 85°C		2.9	3.0	mA
			T _J = 100°C		3.5	6	mA
		Sleep mode ⁶ , VCC33 = 3.63 V	T _J = 25°C		17	18	μΑ
			T _J = 85°C		18	20	μA
			T _J = 100°C		24	25	μA
ICCI ³	I/O quiescent current	Operational standby ⁶ , VCCIx = 3.63 V	T _J = 25°C		260	437	μΑ
			T _J = 85°C		260	437	μΑ
			T _J = 100°C		260	437	μA
IJTAG	JTAG I/O quiescent current	Operational standby ⁴ ,	T _J = 25°C		80	100	μΑ
		VJTAG = 3.63 V	T _J = 85°C		80	100	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V			0	0	μA
IPP	Programming supply current	Non-programming mode, VPUMP = 3.63 V	T _J = 25°C		37	80	μA
			T _J = 85°C		37	80	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V			0	0	μA

Notes:

1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, and ICCI2.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

	QN180		QN180					
Pin Number	AFS090 Function	AFS250 Function	Pin Number	AFS090 Function	AFS250 Function			
B9	XTAL2	XTAL2	B45	GBA2/IO31PDB1V0	GBA2/IO40PDB1V0			
B10	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	B46	GNDQ	GNDQ			
B11	GEB2/IO42PDB3V0	IO60NDB3V0	B47	GBA1/IO30RSB0V0	GBA0/IO38RSB0V0			
B12	VCC	VCC	B48	GBB1/IO28RSB0V0	GBC1/IO35RSB0V0			
B13	VCCNVM	VCCNVM	B49	VCC	VCC			
B14	VCC15A	VCC15A	B50	GBC0/IO25RSB0V0	IO31RSB0V0			
B15	NCAP	NCAP	B51	IO23RSB0V0	IO28RSB0V0			
B16	VCC33N	VCC33N	B52	IO20RSB0V0	IO25RSB0V0			
B17	GNDAQ	GNDAQ	B53	VCC	VCC			
B18	AC0	AC0	B54	IO11RSB0V0	IO14RSB0V0			
B19	AT0	AT0	B55	IO08RSB0V0	IO11RSB0V0			
B20	AT1	AT1	B56	GAC1/IO05RSB0V0	IO08RSB0V0			
B21	AV1	AV1	B57	VCCIB0	VCCIB0			
B22	AC2	AC2	B58	GAB0/IO02RSB0V0	GAC0/IO04RSB0V0			
B23	ATRTN1	ATRTN1	B59	GAA0/IO00RSB0V0	GAA1/IO01RSB0V0			
B24	AG3	AG3	B60	VCCPLA	VCCPLA			
B25	AV3	AV3	C1	NC	NC			
B26	AG4	AG4	C2	NC	VCCIB3			
B27	ATRTN2	ATRTN2	C3	GND	GND			
B28	NC	AC5	C4	NC	GFC2/IO69PPB3V0			
B29	VCC33A	VCC33A	C5	GFC1/IO49PDB3V0	GFC1/IO68PDB3V0			
B30	VAREF	VAREF	C6	GFA0/IO47NPB3V0	GFB0/IO67NPB3V0			
B31	PUB	PUB	C7	VCCIB3	NC			
B32	PTEM	PTEM	C8	GND	GND			
B33	GNDNVM	GNDNVM	C9	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0			
B34	VCC	VCC	C10	GEA2/IO42NDB3V0	GEC2/IO60PDB3V0			
B35	ТСК	ТСК	C11	NC	GEA2/IO58PSB3V0			
B36	TMS	TMS	C12	NC	NC			
B37	TRST	TRST	C13	GND	GND			
B38	GDB2/IO41PSB1V0	GDA2/IO55PSB1V0	C14	NC	NC			
B39	GDC0/IO38NDB1V0	GDB0/IO53NDB1V0	C15	NC	NC			
B40	VCCIB1	VCCIB1	C16	GNDA	GNDA			
B41	GCA1/IO36PDB1V0	GCA1/IO49PDB1V0	C17	NC	NC			
B42	GCC0/IO34NDB1V0	GCC0/IO47NDB1V0	C18	NC	NC			
B43	GCB2/IO33PSB1V0	GBC2/IO42PSB1V0	C19	NC	NC			
B44	VCC	VCC	C20	NC	NC			



Package Pin Assignments

FG256						
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function		
H3	XTAL2	XTAL2	XTAL2	XTAL2		
H4	XTAL1	XTAL1	XTAL1	XTAL1		
H5	GNDOSC	GNDOSC	GNDOSC	GNDOSC		
H6	VCCOSC	VCCOSC	VCCOSC	VCCOSC		
H7	VCC	VCC	VCC	VCC		
H8	GND	GND	GND	GND		
H9	VCC	VCC	VCC	VCC		
H10	GND	GND	GND	GND		
H11	GDC0/IO38NDB1V0	IO51NDB1V0	IO47NDB2V0	IO69NDB2V0		
H12	GDC1/IO38PDB1V0	IO51PDB1V0	IO47PDB2V0	IO69PDB2V0		
H13	GDB1/IO39PDB1V0	GCA1/IO49PDB1V0	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0		
H14	GDB0/IO39NDB1V0	GCA0/IO49NDB1V0	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0		
H15	GCA0/IO36NDB1V0	GCB0/IO48NDB1V0	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0		
H16	GCA1/IO36PDB1V0	GCB1/IO48PDB1V0	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0		
J1	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0		
J2	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0		
J3	IO43NDB3V0	GFB0/IO67NDB3V0	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0		
J4	GEC2/IO43PDB3V0	GFB1/IO67PDB3V0	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0		
J5	NC	GFC0/IO68NDB3V0	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0		
J6	NC	GFC1/IO68PDB3V0	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0		
J7	GND	GND	GND	GND		
J8	VCC	VCC	VCC	VCC		
J9	GND	GND	GND	GND		
J10	VCC	VCC	VCC	VCC		
J11	GDC2/IO41NPB1V0	IO56NPB1V0	IO56NPB2V0	IO83NPB2V0		
J12	NC	GDB0/IO53NPB1V0	GDB0/IO53NPB2V0	GDB0/IO80NPB2V0		
J13	NC	GDA1/IO54PDB1V0	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0		
J14	GDA0/IO40PDB1V0	GDC1/IO52PPB1V0	GDC1/IO52PPB2V0	GDC1/IO79PPB2V0		
J15	NC	IO50NPB1V0	IO51NSB2V0	IO77NSB2V0		
J16	GDA2/IO40NDB1V0	GDC0/IO52NPB1V0	GDC0/IO52NPB2V0	GDC0/IO79NPB2V0		
K1	NC	IO65NPB3V0	IO67NPB4V0	IO92NPB4V0		
K2	VCCIB3	VCCIB3	VCCIB4	VCCIB4		
K3	NC	IO65PPB3V0	IO67PPB4V0	IO92PPB4V0		
K4	NC	IO64PDB3V0	IO65PDB4V0	IO96PDB4V0		
K5	GND	GND	GND	GND		
K6	NC	IO64NDB3V0	IO65NDB4V0	IO96NDB4V0		
K7	VCC	VCC	VCC	VCC		
K8	GND	GND	GND	GND		

FG256							
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function			
K9	VCC	VCC	VCC	VCC			
K10	GND	GND	GND	GND			
K11	NC	GDC2/IO57PPB1V0	GDC2/IO57PPB2V0	GDC2/IO84PPB2V0			
K12	GND	GND	GND	GND			
K13	NC	GDA0/IO54NDB1V0	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0			
K14	NC	GDA2/IO55PPB1V0	GDA2/IO55PPB2V0	GDA2/IO82PPB2V0			
K15	VCCIB1	VCCIB1	VCCIB2	VCCIB2			
K16	NC	GDB1/IO53PPB1V0	GDB1/IO53PPB2V0	GDB1/IO80PPB2V0			
L1	NC	GEC1/IO63PDB3V0	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0			
L2	NC	GEC0/IO63NDB3V0	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0			
L3	NC	GEB1/IO62PDB3V0	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0			
L4	NC	GEB0/IO62NDB3V0	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0			
L5	NC	IO60NDB3V0	IO60NDB4V0	IO87NDB4V0			
L6	NC	GEC2/IO60PDB3V0	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0			
L7	GNDA	GNDA	GNDA	GNDA			
L8	AC0	AC0	AC2	AC2			
L9	AV2	AV2	AV4	AV4			
L10	AC3	AC3	AC5	AC5			
L11	PTEM	PTEM	PTEM	PTEM			
L12	TDO	TDO	TDO	TDO			
L13	VJTAG	VJTAG	VJTAG	VJTAG			
L14	NC	IO57NPB1V0	IO57NPB2V0	IO84NPB2V0			
L15	GDB2/IO41PPB1V0	GDB2/IO56PPB1V0	GDB2/IO56PPB2V0	GDB2/IO83PPB2V0			
L16	NC	IO55NPB1V0	IO55NPB2V0	IO82NPB2V0			
M1	GND	GND	GND	GND			
M2	NC	GEA1/IO61PDB3V0	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0			
M3	NC	GEA0/IO61NDB3V0	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0			
M4	VCCIB3	VCCIB3	VCCIB4	VCCIB4			
M5	NC	IO58NPB3V0	IO58NPB4V0	IO85NPB4V0			
M6	NC	NC	AV0	AV0			
M7	NC	NC	AC1	AC1			
M8	AG1	AG1	AG3	AG3			
M9	AC2	AC2	AC4	AC4			
M10	AC4	AC4	AC6	AC6			
M11	NC	AG5	AG7	AG7			
M12	VPUMP	VPUMP	VPUMP	VPUMP			
M13	VCCIB1	VCCIB1	VCCIB2	VCCIB2			
M14	TMS	TMS	TMS	TMS			

	FG484		FG484				
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function		
H13	GND	GND	K4	IO75NDB4V0	IO110NDB4V0		
H14	VCCIB1	VCCIB1	K5	GND	GND		
H15	GND	GND	K6	NC	IO104NDB4V0		
H16	GND	GND	K7	NC	IO111NDB4V0		
H17	NC	IO53NDB2V0	K8	GND	GND		
H18	IO38PDB2V0	IO57PDB2V0	K9	VCC	VCC		
H19	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0	K10	GND	GND		
H20	VCCIB2	VCCIB2	K11	VCC	VCC		
H21	IO37NDB2V0	IO54NDB2V0	K12	GND	GND		
H22	IO37PDB2V0	IO54PDB2V0	K13	VCC	VCC		
J1	NC	IO112PPB4V0	K14	GND	GND		
J2	IO76NDB4V0	IO113NDB4V0	K15	GND	GND		
J3	GFB2/IO74PDB4V0	GFB2/IO109PDB4V0	K16	IO40NDB2V0	IO60NDB2V0		
J4	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0	K17	NC	IO58PDB2V0		
J5	NC	IO112NPB4V0	K18	GND	GND		
J6	NC	IO104PDB4V0	K19	NC	IO68NPB2V0		
J7	NC	IO111PDB4V0	K20	IO41NDB2V0	IO61NDB2V0		
J8	VCCIB4	VCCIB4	K21	GND	GND		
J9	GND	GND	K22	IO42NDB2V0	IO56NDB2V0		
J10	VCC	VCC	L1	IO73NDB4V0	IO108NDB4V0		
J11	GND	GND	L2	VCCOSC	VCCOSC		
J12	VCC	VCC	L3	VCCIB4	VCCIB4		
J13	GND	GND	L4	XTAL2	XTAL2		
J14	VCC	VCC	L5	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0		
J15	VCCIB2	VCCIB2	L6	VCCIB4	VCCIB4		
J16	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0	L7	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0		
J17	NC	IO58NDB2V0	L8	VCCIB4	VCCIB4		
J18	IO38NDB2V0	IO57NDB2V0	L9	GND	GND		
J19	IO39NDB2V0	IO59NDB2V0	L10	VCC	VCC		
J20	GCC2/IO41PDB2V0	GCC2/IO61PDB2V0	L11	GND	GND		
J21	NC	IO55PSB2V0	L12	VCC	VCC		
J22	IO42PDB2V0	IO56PDB2V0	L13	GND	GND		
K1	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0	L14	VCC	VCC		
K2	GND	GND	L15	VCCIB2	VCCIB2		
K3	IO74NDB4V0	IO109NDB4V0	L16	IO48PDB2V0	IO70PDB2V0		



Datasheet Information

Revision	Changes	Page		
Advance v0.5	The low power modes of operation were updated and clarified.	N/A		
(June 2006)	The AFS1500 digital I/O count was updated in Table 1 • Fusion Family.	i		
	The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double- Ended (Analog)" table.	ii		
	The "Voltage Regulator Power Supply Monitor (VRPSM)" was updated.	2-36		
	Figure 2-45 • FlashROM Timing Diagram was updated.	2-53		
	The "256-Pin FBGA" table for the AFS1500 is new.			
Advance v0.4 (April 2006)	The G was moved in the "Product Ordering Codes" section.	III		
Advance v0.3	The "Features and Benefits" section was updated.	I		
(April 2006)	The "Fusion Family" table was updated.			
	The "Package I/Os: Single-/Double-Ended (Analog)" table was updated.	П		
	The "Product Ordering Codes" table was updated.	Ш		
	The "Temperature Grade Offerings" table was updated.	IV		
	The "General Description" section was updated to include ARM information.	1-1		
	Figure 2-46 • FlashROM Timing Diagram was updated.	2-58		
	The "FlashROM" section was updated.	2-57		
	The "RESET" section was updated.	2-61		
	The "RESET" section was updated.	2-64		
	Figure 2-27 · Real-Time Counter System was updated.	2-35		
	Table 2-19 • Flash Memory Block Pin Names was updated.	2-43		
	Figure 2-33 • Flash Memory Block Diagram was updated to include AUX block information.	2-45		
	Figure 2-34 • Flash Memory Block Organization was updated to include AUX block information.	2-46		
	The note in the "Program Operation" section was updated.	2-48		
	Figure 2-76 • Gate Driver Example was updated.	2-95		
	The "Analog Quad ACM Description" section was updated.	2-130		
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94		
	Figure 2-65 • Analog Block Macro was updated.	2-81		
	Figure 2-65 • Analog Block Macro was updated.	2-81		
	The "Analog Quad" section was updated.	2-84		
	The "Voltage Monitor" section was updated.	2-86		
	The "Direct Digital Input" section was updated.	2-89		
	The "Current Monitor" section was updated.	2-90		
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94		