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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/p1afs1500-2fgg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Related Documents

Datasheet

Core8051 www.microsemi.com/soc/ipdocs/Core8051_DS.pdf

Application Notes

 Fusion FlashROM

 http://www.microsemi.com/soc/documents/Fusion_FROM_AN.pdf

 Fusion SRAM/FIFO Blocks

 http://www.microsemi.com/soc/documents/Fusion_RAM_FIFO_AN.pdf

 Using DDR in Fusion Devices

 http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129938

 Fusion Security

 http://www.microsemi.com/soc/documents/Fusion_Security_AN.pdf

 Using Fusion RAM as Multipliers

 http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129940

Handbook

Cortex-M1 Handbook www.microsemi.com/soc/documents/CortexM1_HB.pdf

User Guides

Designer User Guide http://www.microsemi.com/soc/documents/designer_UG.pdf Fusion FPGA Fabric User Guide http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130817 IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide http://www.microsemi.com/soc/documents/pa3_libguide_ug.pdf SmartGen, FlashROM, Flash Memory System Builder, and Analog System Builder User Guide http://www.microsemi.com/soc/documents/genguide_ug.pdf

White Papers

Fusion Technology http://www.microsemi.com/soc/documents/Fusion_Tech_WP.pdf



Figure 2-4 • Combinatorial Timing Model and Waveforms



Timing Characteristics

Table 2-1 • Combinatorial Cell Propagation DelaysCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	Units
INV	Y = !A	t _{PD}	0.40	0.46	0.54	ns
AND2	$Y = A \cdot B$	t _{PD}	0.47	0.54	0.63	ns
NAND2	$Y = !(A \cdot B)$	t _{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t _{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t _{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t _{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t _{PD}	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	t _{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t _{PD}	0.51	0.58	0.68	ns
AND3	$Y = A \cdot B \cdot C$	t _{PD}	0.56	0.64	0.75	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library (Figure 2-5). For more details, refer to the *IGLOO*, *ProASIC3*, *SmartFusion and Fusion Macro Library Guide*.



Figure 2-5 • Sample of Sequential Cells



Array Coordinates

During many place-and-route operations in the Microsemi Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

		Vers	saTiles		Memor	y Rows	All		
Device	Mi	n.	М	ax.	Bottom	Тор	Min.	Max.	
	x	У	x	У	(x, y)	(x, y)	(x, y)	(x, y)	
AFS090	3	2	98	25	None	(3, 26)	(0, 0)	(101, 29)	
AFS250	3	2	130	49	None	(3, 50)	(0, 0)	(133, 53)	
AFS600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)	
AFS1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 129)	

Table 2-3 • Array Coordinates







Voltage Regulator and Power System Monitor (VRPSM)

The VRPSM macro controls the power-up state of the FPGA. The power-up bar (PUB) pin can turn on the voltage regulator when set to 0. TRST can enable the voltage regulator when deasserted, allowing the FPGA to power-up when user want access to JTAG ports. The inputs VRINITSTATE and RTCPSMMATCH come from the flash bits and RTC, and can also power up the FPGA.



Note: *Signals are hardwired internally and do not exist in the macro core.

Figure 2-30 • VRPSM Macro

Table 2-17 • VRPSM Signal Descriptions

Signal Name	Width	Direction	Function
VRPU	1	In	Voltage Regulator Power-Up
			0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator.
			1 – Voltage regulator enabled
VRINITSTATE	1	In	Voltage Regulator Initial State
			Defines the voltage Regulator status upon power-up of the 3.3 V. The signal is configured by Libero SoC when the VRPSM macro is generated.
			Tie off to 1 – Voltage regulator enables when 3.3 V is powered.
			Tie off to 0 – Voltage regulator disables when 3.3 V is powered.
RTCPSMMATCH	1	In	RTC Power System Management Match
			Connect from RTCPSMATCH signal from RTC in AB
			0 transition to 1 turns on the voltage regulator
PUB	1	In	External pin, built-in weak pull-up
			Power-Up Bar
			0 – Enables voltage regulator at all times
TRST*	1	In	External pin, JTAG Test Reset
			1 – Enables voltage regulator at all times
FPGAGOOD	1	Out	Indicator that the FPGA is powered and functional
			No need to connect if it is not used.
			1 – Indicates that the FPGA is powered up and functional.
			0 – Not possible to read by FPGA since it has already powered off.
PUCORE	1	Out	Power-Up Core
			Inverted signal of PUB. No need to connect if it is not used.
VREN*	1	Out	Voltage Regulator Enable
			Connected to 1.5 V voltage regulator in Fusion device internally.
			0 – Voltage regulator disables
			1 – Voltage regulator enables
Note: *Signals a	re hard	wired interr	ally and do not exist in the macro core.



Timing Characteristics

Table 2-35 • FIFO

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ENS}	REN, WEN Setup time	1.34	1.52	1.79	ns
t _{ENH}	REN, WEN Hold time	0.00	0.00	0.00	ns
t _{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t _{вкн}	BLK Hold time	0.00	0.00	0.00	ns
t _{DS}	Input data (WD) Setup time	0.18	0.21	0.25	ns
t _{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t _{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t _{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t _{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t _{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t _{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t _{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.13	6.98	8.20	ns
+	RESET Low to Data out Low on RD (flow-through)	0.92	1.05	1.23	ns
^I RSTBQ	RESET Low to Data out Low on RD (pipelined)	0.92	1.05	1.23	ns
t _{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t _{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t _{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t _{CYC}	Clock Cycle time	3.23	3.68	4.32	ns
F _{MAX}	Maximum Frequency for FIFO	310	272	231	ns

Analog-to-Digital Converter Block

At the heart of the Fusion analog system is a programmable Successive Approximation Register (SAR) ADC. The ADC can support 8-, 10-, or 12-bit modes of operation. In 12-bit mode, the ADC can resolve 500 ksps. All results are MSB-justified in the ADC. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 2-79. The ADC offers multiple self-calibrating modes to ensure consistent high performance both at power-up and during runtime.



Figure 2-79 • ADC Block Diagram



EQ 16 through EQ 18 can be used to calculate the acquisition time required for a given input. The STC signal gives the number of sample periods in ADCCLK for the acquisition time of the desired signal. If the actual acquisition time is higher than the STC value, the settling time error can affect the accuracy of the ADC, because the sampling capacitor is only partially charged within the given sampling cycle. Example acquisition times are given in Table 2-44 and Table 2-45. When controlling the sample time for the ADC along with the use of the active bipolar prescaler, current monitor, or temperature monitor, the minimum sample time(s) for each must be obeyed. EQ 19 can be used to determine the appropriate value of STC.

You can calculate the minimum actual acquisition time by using EQ 16:

EQ 16

EQ 17

For 0.5 LSB gain error, VOUT should be replaced with (VIN –(0.5 × LSB Value)): (VIN – 0.5 × LSB Value) = VIN(1 – $e^{-t/RC}$)

$$1 - e^{-e^{-1}}$$

Solving EQ 17:

EQ 18

where $R = Z_{INAD} + R_{SOURCE}$ and $C = C_{INAD}$. Calculate the value of STC by using EQ 19.

t_{SAMPLE} = (2 + STC) x (1 / ADCCLK) or t_{SAMPLE} = (2 + STC) x (ADC Clock Period)

EQ 19

where ADCCLK = ADC clock frequency in MHz.

where VIN is the ADC reference voltage (VREF)

 t_{SAMPLE} = 0.449 µs from bit resolution in Table 2-44.

ADC Clock frequency = 10 MHz or a 100 ns period.

STC = (t_{SAMPLE} / (1 / 10 MHz)) - 2 = 4.49 - 2 = 2.49.

You must round up to 3 to accommodate the minimum sample time.

Table 2-44 • Acquisition Time Example with VAREF = 2.56 V

VIN = 2.56V, R = 4K (R _{SOURCE} ~ 0), C = 18 pF							
Resolution LSB Value (mV) Min. Sample/Hold Time for 0.5 LSB (µs)							
8	10	0.449					
10	2.5	0.549					
12	0.625	0.649					

|--|

VIN = 3.3V, R = 4K (R _{SOURCE} ~ 0), C = 18 pF							
Resolution LSB Value (mV) Min. Sample/Hold time for 0.5 LSB (μs)							
8	12.891	0.449					
10	3.223	0.549					
12	0.806	0.649					

Sample Phase

A conversion is performed in three phases. In the first phase, the analog input voltage is sampled on the input capacitor. This phase is called sample phase. During the sample phase, the output signals BUSY and SAMPLE change from '0' to '1', indicating the ADC is busy and sampling the analog signal. The sample time can be controlled by input signals STC[7:0]. The sample time can be calculated by EQ 20. When controlling the sample time for the ADC along with the use of Prescaler or Current Monitor or Temperature Monitor, the minimum sample time for each must be obeyed.



Intra-Conversion



Note: **t*_{CONV} represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, *t*_{CONV}.

Figure 2-92 • Intra-Conversion Timing Diagram



Injected Conversion

Note: *See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.

Figure 2-93 • Injected Conversion Timing Diagram

5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to $3.3 \vee LVTTL$ or $3.3 \vee LVCMOS$ mode, Fusion I/Os can directly drive signals into $5 \vee TTL$ receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both $3.3 \vee LVTTL$ and $3.3 \vee LVCMOS$ modes exceed the VIL = 0.8 V and VIH = 2 V level requirements of $5 \vee TTL$ receivers. Therefore, level '1' and level '0' will be recognized correctly by $5 \vee TTL$ receivers.

Simultaneously Switching Outputs and PCB Layout

- Simultaneously switching outputs (SSOs) can produce signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and VCCI dip noise. These two noise types are caused by rapidly changing currents through GND and VCCI package pin inductances during switching activities:
- Ground bounce noise voltage = L(GND) * di/dt
- VCCI dip noise voltage = L(VCCI) * di/dt

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

User I/O Naming Convention

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

- G = Global
- m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).
- n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-22 on page 2-25 shows the three input pins per clock source MUX at CCC location m.
- u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.
- x = P (Positive) or N (Negative) for differential pairs, or R (Regular single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as an LVPECL pair.
- w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

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B = Bank
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- y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.
- V = Reference voltage
- z = Minibank number



Standard I/O Bank

Figure 2-113 • Naming Conventions of Fusion Devices with Three Digital I/O Banks

Table 2-117 • 2.5 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	-1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	-2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
4 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	-1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	-2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
6 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	-1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	-2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
8 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	-1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	-2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns

Microsemi

Device Architecture

Table 2-123 • 1.8 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Advanced I/Os

Drive	Speed		4	4	4	4	4	4		4	4		11
Strength	Grade	^t DOUT	τ _{DP}	τ _{DIN}	τργ	^τ EOUT	τ _{ZL}	τ _{ZH}	τ _{LZ}	^τ ΗΖ	^t ZLS	τzhs	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	-1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	-2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	-1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	-2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
8 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	-1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	-2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
12 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	-1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	-2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	-1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	-2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-124 • 1.8 V LVCMOS Low Slew

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Standard I/Os

Drive	Speed										
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	15.01	0.04	1.20	0.43	13.15	15.01	1.99	1.99	ns
	–1	0.56	12.77	0.04	1.02	0.36	11.19	12.77	1.70	1.70	ns
	-2	0.49	11.21	0.03	0.90	0.32	9.82	11.21	1.49	1.49	ns
4 mA	Std.	0.66	10.10	0.04	1.20	0.43	9.55	10.10	2.41	2.37	ns
	–1	0.56	8.59	0.04	1.02	0.36	8.13	8.59	2.05	2.02	ns
	-2	0.49	7.54	0.03	0.90	0.32	7.13	7.54	1.80	1.77	ns



IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/Os" section on page 2-132 for more details.

Timing Characteristics

Table 2-186 • JTAG 1532

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{DISU}	Test Data Input Setup Time	0.50	0.57	0.67	ns
t _{DIHD}	Test Data Input Hold Time	1.00	1.13	1.33	ns
t _{TMSSU}	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t _{TMDHD}	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t _{TCK2Q}	Clock to Q (data out)	6.00	6.80	8.00	ns
t _{RSTB2Q}	Reset to Q (data out)	20.00	22.67	26.67	ns
F _{TCKMAX}	TCK Maximum Frequency	25.00	22.00	19.00	MHz
t _{TRSTREM}	ResetB Removal Time	0.00	0.00	0.00	ns
t _{TRSTREC}	ResetB Recovery Time	0.20	0.23	0.27	ns
t _{TRSTMPW}	ResetB Minimum Pulse	TBD	TBD	TBD	ns



Symbol	Parameter ²		Commercial	Industrial	Units
Τ _J	Junction temperature		0 to +85	-40 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming mode ³	3.15 to 3.45	3.15 to 3.45	V
		Operation ⁴	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage	1.7 to 1.9	1.7 to 1.9	V	
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O	3.0 to 3.6	3.0 to 3.6	V	
VCC33A	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VCC33PMP	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VAREF	Voltage reference for ADC	2.527 to 2.593	2.527 to 2.593	V	
VCC15A ⁵	Digital power supply for the analog	1.425 to 1.575	1.425 to 1.575	V	
VCCNVM	Embedded flash power supply	1.425 to 1.575	1.425 to 1.575	V	
VCCOSC	Oscillator power supply	2.97 to 3.63	2.97 to 3.63	V	
AV, AC ⁶	Unpowered, ADC reset asserted or unconfigured		-10.5 to 12.0	-10.5 to 11.6	V
	Analog input (+16 V to +2 V presca	-0.3 to 12.0	–0.3 to 11.6	V	
	Analog input (+1 V to + 0.125 V pre	-0.3 to 3.6	-0.3 to 3.6	V	
	Analog input (–16 V to –2 V presca	-10.5 to 0.3	-10.5 to 0.3	V	
	Analog input (–1 V to –0.125 V pres	-3.6 to 0.3	-3.6 to 0.3	V	
	Analog input (direct input to ADC)	-0.3 to 3.6	-0.3 to 3.6	V	
	Digital input		-0.3 to 12.0	–0.3 to 11.6	V
AG ⁶	Unpowered, ADC reset asserted or	unconfigured	-10.5 to 12.0	-10.5 to 11.6	V
	Low Current Mode (1 µA, 3 µA, 10	μΑ, 3 μΑ, 10 μΑ, 30 μΑ)		–0.3 to 11.6	V
	Low Current Mode (–1 µA, –3 µA, -	-10.5 to 0.3	-10.5 to 0.3	V	
	High Current Mode ⁷	-10.5 to 12.0	-10.5 to 11.6	V	
AT ⁶	Unpowered, ADC reset asserted or unconfigured		-0.3 to 15.5 -0.3 to 1		V
	Analog input (+16 V, +4 V prescale	–0.3 to 15.5	–0.3 to 14.5	V	
	Analog input (direct input to ADC)	-0.3 to 3.6	-0.3 to 3.6	V	
	Digital input	-0.3 to 15.5	-0.3 to 14.5	V	

Table 3-2 • Recommended Operating Conditions¹

Notes:

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-157.

- 2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
- 3. The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.
- 4. VPUMP can be left floating during normal operation (not programming mode).
- 5. Violating the V_{CC15A} recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.
- 6. The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.
- 7. The AG pad should also conform to the limits as specified in Table 2-48 on page 2-114.

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • AFS1500 Quiescent Supply Current Characteristics

Parameter	Description	Conditions	Temp.	Min.	Тур.	Max.	Unit
ICC ¹	1.5 V quiescent current	Operational standby ⁴ ,	T _J = 25°C		20	40	mA
		VCC = 1.575 V	T _J = 85°C		32	65	mA
			T _J = 100°C		59	120	mA
		Standby mode ⁵ or Sleep mode ⁶ , VCC = 0 V			0	0	μA
ICC33 ²	3.3 V analog supplies current	Operational standby ⁴ ,	T _J = 25°C		9.8	13	mA
		VCC33 = 3.63 V	T _J = 85°C		10.7	14	mA
			T _J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T _J = 25°C		0.31	2	mA
			T _J = 85°C		0.35	2	mA
			T _J = 100°C		0.45	2	mA
		Standby mode ⁵ , VCC33 = 3.63 V	T _J = 25°C		2.9	3.6	mA
			T _J = 85°C		2.9	4	mA
			T _J = 100°C		3.3	6	mA
		Sleep mode ⁶ , VCC33 = 3.63 V	T _J = 25°C		17	19	μA
			T _J = 85°C		18	20	μA
			T _J = 100°C		24	25	μA
ICCI ³	I/O quiescent current	Operational standby ⁴ ,	T _J = 25°C		417	649	μA
		Standby mode, and Sleep Mode ^o , VCCIx = 3.63 V	T _J = 85°C		417	649	μA
			T _J = 100°C		417	649	μA

Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.



Package Pin Assignments

PQ208		PQ208				
Pin Number	AFS250 Function	AFS600 Function	Pin Number	AFS250 Function	AFS600 Function	
147	GCC1/IO47PDB1V0	IO39NDB2V0	184	IO18RSB0V0	IO10PPB0V1	
148	IO42NDB1V0	GCA2/IO39PDB2V0	185	IO17RSB0V0	IO09PPB0V1	
149	GBC2/IO42PDB1V0	IO31NDB2V0	186	IO16RSB0V0	IO10NPB0V1	
150	VCCIB1	GBB2/IO31PDB2V0	187	IO15RSB0V0	IO09NPB0V1	
151	GND	IO30NDB2V0	188	VCCIB0	IO08PPB0V1	
152	VCC	GBA2/IO30PDB2V0	189	GND	IO07PPB0V1	
153	IO41NDB1V0	VCCIB2	190	VCC	IO08NPB0V1	
154	GBB2/IO41PDB1V0	GNDQ	191	IO14RSB0V0	IO07NPB0V1	
155	IO40NDB1V0	VCOMPLB	192	IO13RSB0V0	IO06PPB0V0	
156	GBA2/IO40PDB1V0	VCCPLB	193	IO12RSB0V0	IO05PPB0V0	
157	GBA1/IO39RSB0V0	VCCIB1	194	IO11RSB0V0	IO06NPB0V0	
158	GBA0/IO38RSB0V0	GNDQ	195	IO10RSB0V0	IO04PPB0V0	
159	GBB1/IO37RSB0V0	GBB1/IO27PPB1V1	196	IO09RSB0V0	IO05NPB0V0	
160	GBB0/IO36RSB0V0	GBA1/IO28PPB1V1	197	IO08RSB0V0	IO04NPB0V0	
161	GBC1/IO35RSB0V0	GBB0/IO27NPB1V1	198	IO07RSB0V0	GAC1/IO03PDB0V0	
162	VCCIB0	GBA0/IO28NPB1V1	199	IO06RSB0V0	GAC0/IO03NDB0V0	
163	GND	VCCIB1	200	GAC1/IO05RSB0V0	VCCIB0	
164	VCC	GND	201	VCCIB0	GND	
165	GBC0/IO34RSB0V0	VCC	202	GND	VCC	
166	IO33RSB0V0	GBC1/IO26PDB1V1	203	VCC	GAB1/IO02PDB0V0	
167	IO32RSB0V0	GBC0/IO26NDB1V1	204	GAC0/IO04RSB0V0	GAB0/IO02NDB0V0	
168	IO31RSB0V0	IO24PPB1V1	205	GAB1/IO03RSB0V0	GAA1/IO01PDB0V0	
169	IO30RSB0V0	IO23PPB1V1	206	GAB0/IO02RSB0V0	GAA0/IO01NDB0V0	
170	IO29RSB0V0	IO24NPB1V1	207	GAA1/IO01RSB0V0	GNDQ	
171	IO28RSB0V0	IO23NPB1V1	208	GAA0/IO00RSB0V0	VCCIB0	
172	IO27RSB0V0	IO22PPB1V0				
173	IO26RSB0V0	IO21PPB1V0				
174	IO25RSB0V0	IO22NPB1V0				
175	VCCIB0	IO21NPB1V0				
176	GND	IO20PSB1V0				
177	VCC	IO19PSB1V0				
178	IO24RSB0V0	IO14NSB0V1				
179	IO23RSB0V0	IO12PDB0V1				
180	IO22RSB0V0	IO12NDB0V1				
181	IO21RSB0V0	VCCIB0				
182	IO20RSB0V0	GND				
183	IO19RSB0V0	VCC				



Package Pin Assignments

FG484		FG484			
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
L17	VCCIB2	VCCIB2	N8	GND	GND
L18	IO46PDB2V0	IO69PDB2V0	N9	GND	GND
L19	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0	N10	VCC	VCC
L20	VCCIB2	VCCIB2	N11	GND	GND
L21	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0	N12	VCC	VCC
L22	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0	N13	GND	GND
M1	NC	IO103PDB4V0	N14	VCC	VCC
M2	XTAL1	XTAL1	N15	GND	GND
M3	VCCIB4	VCCIB4	N16	GDB2/IO56PDB2V0	GDB2/IO83PDB2V0
M4	GNDOSC	GNDOSC	N17	NC	IO78PDB2V0
M5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0	N18	GND	GND
M6	VCCIB4	VCCIB4	N19	IO47NDB2V0	IO72NDB2V0
M7	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0	N20	IO47PDB2V0	IO72PDB2V0
M8	VCCIB4	VCCIB4	N21	GND	GND
M9	VCC	VCC	N22	IO49PDB2V0	IO71PDB2V0
M10	GND	GND	P1	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
M11	VCC	VCC	P2	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
M12	GND	GND	P3	IO68NDB4V0	IO101NDB4V0
M13	VCC	VCC	P4	IO65PDB4V0	IO96PDB4V0
M14	GND	GND	P5	IO65NDB4V0	IO96NDB4V0
M15	VCCIB2	VCCIB2	P6	NC	IO99NDB4V0
M16	IO48NDB2V0	IO70NDB2V0	P7	NC	IO97NDB4V0
M17	VCCIB2	VCCIB2	P8	VCCIB4	VCCIB4
M18	IO46NDB2V0	IO69NDB2V0	P9	VCC	VCC
M19	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0	P10	GND	GND
M20	VCCIB2	VCCIB2	P11	VCC	VCC
M21	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0	P12	GND	GND
M22	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0	P13	VCC	VCC
N1	NC	IO103NDB4V0	P14	GND	GND
N2	GND	GND	P15	VCCIB2	VCCIB2
N3	IO68PDB4V0	IO101PDB4V0	P16	IO56NDB2V0	IO83NDB2V0
N4	NC	IO100NPB4V0	P17	NC	IO78NDB2V0
N5	GND	GND	P18	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
N6	NC	IO99PDB4V0	P19	GDB1/IO53PDB2V0	GDB1/IO80PDB2V0
N7	NC	IO97PDB4V0	P20	IO51NDB2V0	IO73NDB2V0

Microsemi -Fusion Family of Mixed Signal FPGAs

FG676			FG676			
Pin Number	AFS1500 Function		Pin Number	AFS1500 Function		
AD5	IO94NPB4V0		AE15	GNDA		
AD6	GND		AE16	NC		
AD7	VCC33N		AE17	NC		
AD8	AT0		AE18	GNDA		
AD9	ATRTN0		AE19	NC		
AD10	AT1		AE20	NC		
AD11	AT2		AE21	NC		
AD12	ATRTN1		AE22	NC		
AD13	AT3		AE23	NC		
AD14	AT6		AE24	NC		
AD15	ATRTN3		AE25	GND		
AD16	AT7		AE26	GND		
AD17	AT8		AF1	NC		
AD18	ATRTN4		AF2	GND		
AD19	AT9		AF3	NC		
AD20	VCC33A		AF4	NC		
AD21	GND		AF5	NC		
AD22	IO76NPB2V0		AF6	NC		
AD23	NC		AF7	NC		
AD24	GND		AF8	NC		
AD25	NC		AF9	VCC33A		
AD26	NC		AF10	NC		
AE1	GND		AF11	NC		
AE2	GND		AF12	VCC33A		
AE3	NC		AF13	NC		
AE4	NC		AF14	NC		
AE5	NC		AF15	VCC33A		
AE6	NC		AF16	NC		
AE7	NC		AF17	NC		
AE8	NC		AF18	VCC33A		
AE9	GNDA		AF19	NC		
AE10	NC		AF20	NC		
AE11	NC		AF21	NC		
AE12	GNDA		AF22	NC		
AE13	NC		AF23	NC		
AE14	NC		AF24	NC		

FG676		
Pin Number	AFS1500 Function	
AF25	GND	
AF26	NC	
B1	GND	
B2	GND	
B3	NC	
B4	NC	
B5	NC	
B6	VCCIB0	
B7	NC	
B8	NC	
B9	VCCIB0	
B10	IO15NDB0V2	
B11	IO15PDB0V2	
B12	VCCIB0	
B13	IO19NDB0V2	
B14	IO19PDB0V2	
B15	VCCIB1	
B16	IO25NDB1V0	
B17	IO25PDB1V0	
B18	VCCIB1	
B19	IO33NDB1V1	
B20	IO33PDB1V1	
B21	VCCIB1	
B22	NC	
B23	NC	
B24	NC	
B25	GND	
B26	GND	
C1	NC	
C2	NC	
C3	GND	
C4	NC	
C5	GAA1/IO01PDB0V0	
C6	GAB0/IO02NDB0V0	
C7	GAB1/IO02PDB0V0	
C8	IO07NDB0V1	