

Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/p1afs600-2fg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Fusion Device Family Overview

Instant On

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design.

Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.



Table 2-16 • RTC Control/Status Register

Bit	Name	Description	Default Value
7	rtc_rst	RTC Reset	
		1 – Resets the RTC	
		0 – Deassert reset on after two ACM_CLK cycle.	
6	cntr_en	Counter Enable	0
		1 – Enables the counter; rtc_rst must be deasserted as well. First counter increments after 64 RTCCLK positive edges.	
		0 – Disables the crystal prescaler but does not reset the counter value. Counter value can only be updated when the counter is disabled.	
5	vr_en_mat	Voltage Regulator Enable on Match	0
		1 – Enables RTCMATCH and RTCPSMMATCH to output 1 when the counter value equals the Match Register value. This enables the 1.5 V voltage regulator when RTCPSMMATCH connects to the RTCPSMMATCH signal in VRPSM.	
		0 – RTCMATCH and RTCPSMMATCH output 0 at all times.	
4:3	xt_mode[1:0]	Crystal Mode	00
		Controls RTCXTLMODE[1:0]. Connects to RTC_MODE signal in XTLOSC. XTL_MODE uses this value when xtal_en is 1. See the "Crystal Oscillator" section on page 2-20 for mode configuration.	
2	rst_cnt_omat	Reset Counter on Match	0
		1 – Enables the sync clear of the counter when the counter value equals the Match Register value. The counter clears on the rising edge of the clock. If all the Match Registers are set to 0, the clear is disabled.	
		0 – Counter increments indefinitely	
1	rstb_cnt	Counter Reset, active Low	0
		0 - Resets the 40-bit counter value	
0	xtal_en	Crystal Enable	0
		Controls RTCXTLSEL. Connects to SELMODE signal in XTLOSC.	
		0 – XTLOSC enables control by FPGA_EN; xt_mode is not used. Sleep mode requires this bit to equal 0.	
		1 – Enables XTLOSC, XTL_MODE control by xt_mode	
		Standby mode requires this bit to be set to 1.	
		See the "Crystal Oscillator" section on page 2-20 for further details on SELMODE configuration.	







Figure 2-31 • State Diagram for All Different Power Modes

When TRST is 1 or PUB is 0, the 1.5 V voltage regulator is always ON, putting the Fusion device in normal operation at all times. Therefore, when the JTAG port is not in reset, the Fusion device cannot enter sleep mode or standby mode.

To enter standby mode, the Fusion device must first power-up into normal operation. The RTC is enabled through the RTC Control/Status Register described in the "Real-Time Counter (part of AB macro)" section on page 2-33. A match value corresponding to the wake-up time is loaded into the Match Register. The 1.5 V voltage regulator is disabled by setting VRPU to 0 to allow the Fusion device to enter standby mode, when the 1.5 V supply is off but the RTC remains on.



The third part of the Analog Quad is called the Gate Driver Block, and its output pin is named AG. This section is used to drive an external FET. There are two modes available: a High Current Drive mode and a Current Source Control mode. Both negative and positive voltage polarities are available, and in the current source control mode, four different current levels are available.

The fourth section of the Analog Quad is called the Temperature Monitor Block, and its input pin name is AT. This block is similar to the Voltage Monitor Block, except that it has an additional function: it can be used to monitor the temperature of an external diode-connected transistor. It has a modified prescaler and is limited to positive voltages only.

The Analog Quad can be configured during design time by Libero SoC; however, the ACM can be used to change the parameters of any of these I/Os during runtime. This type of change is referred to as a context switch. The Analog Quad is a modular structure that is replicated to generate the analog I/O resources. Each Fusion device supports between 5 and 10 Analog Quads.

The analog pads are numbered to clearly identify both the type of pad (voltage, current, gate driver, or temperature pad) and its corresponding Analog Quad (AV0, AC0, AG0, AT0, AV1, ..., AC9, AG9, and AT9). There are three types of input pads (AVx, ACx, and ATx) and one type of analog output pad (AGx). Since there can be up to 10 Analog Quads on a device, there can be a maximum of 30 analog input pads and 10 analog output pads.



Figure 2-65 • Analog Quad



Gain Error

The gain error of an ADC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale (%FSR). Gain error is the full-scale error minus the offset error (Figure 2-84).



Figure 2-84 • Gain Error

Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.



Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ideal ADC, the first transition occurs at 0.5 LSB above zero. The offset voltage is measured by applying an analog input such that the ADC outputs all zeroes and increases until the first transition occurs (Figure 2-86).



Figure 2-86 • Offset Error

Resolution

ADC resolution is the number of bits used to represent an analog input signal. To more accurately replicate the analog signal, resolution needs to be increased.

Sampling Rate

Sampling rate or sample frequency, specified in samples per second (sps), is the rate at which an ADC acquires (samples) the analog input.

SNR – Signal-to-Noise Ratio

SNR is the ratio of the amplitude of the desired signal to the amplitude of the noise signals at a given point in time. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR (EQ 14) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum ADC noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[MAX]} = 6.02_{dB} \times N + 1.76_{dB}$$

EQ 14

SINAD – Signal-to-Noise and Distortion

SINAD is the ratio of the rms amplitude to the mean value of the root-sum-square of the all other spectral components, including harmonics, but excluding DC. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion.

Total Harmonic Distortion

THD measures the distortion content of a signal, and is specified in decibels relative to the carrier (dBc). THD is the ratio of the RMS sum of the selected harmonics of the input signal to the fundamental itself. Only harmonics within the Nyquist limit are included in the measurement.



Integrated Voltage Reference

The Fusion device has an integrated on-chip 2.56 V reference voltage for the ADC. The value of this reference voltage was chosen to make the prescaling and postscaling factors for the prescaler blocks change in a binary fashion. However, if desired, an external reference voltage of up to 3.3 V can be connected between the VAREF and ADCGNDREF pins. The VAREFSEL control pin is used to select the reference voltage.

Table 2-42 • VAREF Bit Function

Name	Bit	Function
VAREF	0	Reference voltage selection
		0 – Internal voltage reference selected. VAREF pin outputs 2.56 V.
		1 – Input external voltage reference from VAREF and ADCGNDREF

ADC Clock

The speed of the ADC depends on its internal clock, ADCCLK, which is not accessible to users. The ADCCLK is derived from SYSCLK. Input signal TVC[7:0], Time Divider Control, determines the speed of the ADCCLK in relationship to SYSCLK, based on EQ 15.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK}$$

EQ 15

TVC: Time Divider Control (0-255)

 t_{ADCCLK} is the period of ADCCLK, and must be between 0.5 MHz and 10 MHz t_{SYSCLK} is the period of SYSCLK

Table 2-43 • TVC Bits Function

Name	Bits	Function
TVC	[7:0]	SYSCLK divider control

The frequency of ADCCLK, f_{ADCCLK}, must be within 0.5 Hz to 10 MHz.

The inputs to the ADC are synchronized to SYSCLK. A conversion is initiated by asserting the ADCSTART signal on a rising edge of SYSCLK. Figure 2-90 on page 2-112 and Figure 2-91 on page 2-112 show the timing diagram for the ADC.

Acquisition Time or Sample Time Control

Acquisition time (t_{SAMPLE}) specifies how long an analog input signal has to charge the internal capacitor array. Figure 2-88 shows a simplified internal input sampling mechanism of a SAR ADC.



Figure 2-88 • Simplified Sample and Hold Circuitry

The internal impedance (Z_{INAD}), external source resistance (R_{SOURCE}), and sample capacitor (C_{INAD}) form a simple RC network. As a result, the accuracy of the ADC can be affected if the ADC is given insufficient time to charge the capacitor. To resolve this problem, you can either reduce the source resistance or increase the sampling time by changing the acquisition time using the STC signal.

Table 2-49 • Analog Channel Specifications (continued)Commercial Temperature Range Conditions, TJ = 85°C (unless noted otherwise),Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units		
Temperature Mo	nitor Using Analog Pad	AT						
External	Resolution	8-bit ADC			4	°C		
Temperature		10-bit ADC			1	°C		
(external diode		12-bit ADC		0.25				
2N3904, T _J = 25°C) ⁴	Systematic Offset ⁵	AFS090, AFS250, AFS600, AFS1500, uncalibrated ⁷			5	°C		
		AFS090, AFS250, AFS600, AFS1500, calibrated ⁷		±5				
	Accuracy			±3	±5	°C		
	External Sensor Source	High level, TMSTBx = 0		10		μA		
	Current	Low level, TMSTBx = 1		100		μA		
	Max Capacitance on AT pad				1.3	nF		
Internal	Resolution	8-bit ADC	4			°C		
Temperature		10-bit ADC	1			°C		
Mornton		12-bit ADC	0.25			°C		
	Systematic Offset ⁵	AFS090 ⁷			5	°C		
		AFS250, AFS600, AFS1500 ⁷			11	°C		
	Accuracy			±3	±5	°C		
t _{TMSHI}	Strobe High time		10		105	μs		
t _{TMSLO}	Strobe Low time		5			μs		
t _{TMSSET}	Settling time		5			μs		

Notes:

1. VRSM is the maximum voltage drop across the current sense resistor.

2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.

3. VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.

- 4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
- 5. The temperature offset is a fixed positive value.
- 6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
- 7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.

Table 2-50 • ADC Characteristics in Direct Input ModeCommercial Temperature Range Conditions, TJ = 85°C (unless noted otherwise),Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Direct Input	using Analog Pad AV, AC, A	Г				
VINADC	Input Voltage (Direct Input)	Refer to Table 3-2 on page 3-3				
CINADC	Input Capacitance	Channel not selected		7		pF
		Channel selected but not sampling		8		pF
		Channel selected and sampling		18		pF
ZINADC	Input Impedance	8-bit mode		2		kΩ
		10-bit mode		2		kΩ
		12-bit mode		2		kΩ
Analog Refe	erence Voltage VAREF					
VAREF	Accuracy	T _J = 25°C	2.537	2.56	2.583	V
	Temperature Drift of Internal Reference			65		ppm / °C
	External Reference		2.527		VCC33A + 0.05	V
ADC Accura	acy (using external reference) 1,2				
DC Accurac	у					
TUE	Total Unadjusted Error	8-bit mode		0.2	29	LSB
		10-bit mode		0.7	72	LSB
		12-bit mode	1.8			LSB
INL	Integral Non-Linearity	8-bit mode		0.20	0.25	LSB
		10-bit mode		0.32	0.43	LSB
		12-bit mode		1.71	1.80	LSB
DNL	Differential Non-Linearity (no missing code)	8-bit mode		0.20	0.24	LSB
		10-bit mode		0.60	0.65	LSB
		12-bit mode		2.40	2.48	LSB
	Offset Error	8-bit mode		0.01	0.17	LSB
		10-bit mode		0.05	0.20	LSB
		12-bit mode		0.20	0.40	LSB
	Gain Error	8-bit mode		0.0004	0.003	LSB
		10-bit mode		0.002	0.011	LSB
		12-bit mode		0.007	0.044	LSB
	Gain Error (with internal reference)	All modes		2		% FSR

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.



Hot-Swap Support

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-74. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

Table 2-74 • Levels of Hot-Swap Support

Hot Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain Fusion Devices	Compliance of Fusion Devices
1	Cold-swap	No	-	_	_	System and card with Microsemi FPGA chip are powered down, then card gets plugged into system, then power supplies are turned on for system but not for FPGA on card.	Compliant I/Os can but do not have to be set to hot insertion mode.
2	Hot-swap while reset	Yes	Held in reset state	Must be made and maintained for 1 ms before, during, and after insertion/ removal	_	In PCI hot plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant I/Os can but do not have to be set to hot insertion mode.
3	Hot-swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/re moval)	Same as Level 2	Must remain glitch-free during power-up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on bus. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.
4	Hot-swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle.	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.



Temporary overshoots are allowed according to Table 3-4 on page 3-4.



Figure 2-103 • Solution 1

Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-4. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-104. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.



Figure 2-104 • Solution 2



Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions

			VIL		VIH		VOL	VOH	IOL	ЮН
I/O Standard	Drive Strength	Slew Rate	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	-0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	-0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4
1.5 V LVCMOS	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Applicable to Standard I/Os

Note: Currents are measured at 85°C junction temperature.

Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

Applicable to All I/O Bank Types

	Comn	nercial ¹	Indu	strial ²
	IIL ³	IIH ⁴	IIL ³	IIH ⁴
DC I/O Standards	μΑ	μΑ	μΑ	μA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. Commercial range ($0^{\circ}C < T_J < 85^{\circ}C$)

2. Industrial range $(-40^{\circ}C < T_{J} < 100^{\circ}C)$

3. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

4. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.



Table 2-107 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Advanced I/Os

Drive	Speed												l
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
4 mA	Std.	0.66	7.66	0.04	1.20	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	-1	0.56	6.51	0.04	1.02	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	-2	0.49	5.72	0.03	0.90	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
8 mA	Std.	0.66	4.91	0.04	1.20	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	-1	0.56	4.17	0.04	1.02	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	-2	0.49	3.66	0.03	0.90	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	Std.	0.66	3.53	0.04	1.20	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	-1	0.56	3.00	0.04	1.02	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	-2	0.49	2.64	0.03	0.90	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	Std.	0.66	3.33	0.04	1.20	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	-1	0.56	2.83	0.04	1.02	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	-2	0.49	2.49	0.03	0.90	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	Std.	0.66	3.08	0.04	1.20	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	-1	0.56	2.62	0.04	1.02	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	-2	0.49	2.30	0.03	0.90	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-108 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard I/Os

Drive	Speed										
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	-1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	-2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
4 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	-1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	-2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
6 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	-1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	-2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns
8 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	-1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	-2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.8 V applications. It uses a 1.8 V input buffer and push-pull output buffer.

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. Max. V V		Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
Applicable	to Pro I/0) Banks										
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	16	16	74	91	10	10
Applicable	to Advar	nced I/O Banl	(S									
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	16	16	74	91	10	10
Applicable	to Stand	ard I/O Banks	5			•						
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4	22	17	10	10

Table 2-118 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-121 • AC Loading

Table 2-119 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input Low (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.8	0.9	_	35

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.



Table 2-174 • Parameter Definitions and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
tosud	Data Setup Time for the Output Data Register	F, H
t _{OHD}	Data Hold Time for the Output Data Register	F, H
t _{OSUE}	Enable Setup Time for the Output Data Register	G, H
t _{OHE}	Enable Hold Time for the Output Data Register	G, H
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L,DOUT
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	L, H
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t _{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t _{OESUD}	Data Setup Time for the Output Enable Register	J, H
t _{OEHD}	Data Hold Time for the Output Enable Register	J, H
t _{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t _{OEHE}	Enable Hold Time for the Output Enable Register	K, H
t _{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
t _{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	I, H
t _{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t _{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t _{ISUD}	Data Setup Time for the Input Data Register	C, A
t _{IHD}	Data Hold Time for the Input Data Register	C, A
t _{ISUE}	Enable Setup Time for the Input Data Register	B, A
t _{IHE}	Enable Hold Time for the Input Data Register	B, A
t _{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
t _{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	D, A
t _{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-137 on page 2-212 for more information.



Pin Descriptions

Supply Pins

GND Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF Analog Reference Ground

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA Ground (analog)

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ Ground (analog quiet)

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM Flash Memory Ground

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC Oscillator Ground

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A Analog Power Supply (1.5 V)

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A Analog Power Supply (3.3 V)

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N Negative 3.3 V Output

This is the -3.3 V output from the voltage converter. A 2.2 μ F capacitor must be connected from this pin to ground.

VCC33PMP Analog Power Supply (3.3 V)

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM Flash Memory Block Power Supply (1.5 V)

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC Oscillator Power Supply (3.3 V)

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33 pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

Parameter	Description	Conditions	Temp.	Min	Тур	Мах	Unit
ICC ¹	1.5 V quiescent current	Operational standby ⁴ ,	T _J = 25°C		5	7.5	mA
		VCC = 1.575 V	T _J = 85°C		6.5	20	mA
			T _J = 100°C		14	48	mA
		Standby mode ⁵ or Sleep mode ⁶ , V _{CC} = 0 V			0	0	μA
ICC33 ²	3.3 V analog supplies current	Operational standby ⁴ ,	T _J = 25°C		9.8	12	mA
		VCC33 = 3.63 V	T _J = 85°C		9.8	12	mA
			T _J = 100°C		10.7	15	mA
		Operational standby, only	T _J = 25°C		0.30	2	mA
		output ON, VCC33 = 3.63 V	T _J = 85°C		0.30	2	mA
			T _J = 100°C		0.45	2	mA
		Standby mode ⁵ , VCC33 = 3.63 V	T _J = 25°C		2.9	2.9	mA
			T _J = 85°C		2.9	3.0	mA
			T _J = 100°C		3.5	6	mA
		Sleep mode ⁶ , VCC33 = 3.63 V	T _J = 25°C		17	18	μΑ
			T _J = 85°C		18	20	μΑ
			T _J = 100°C		24	25	μA
ICCI ³	I/O quiescent current	Operational standby ⁶ , VCCIx = 3.63 V	T _J = 25°C		260	437	μΑ
			T _J = 85°C		260	437	μΑ
			T _J = 100°C		260	437	μA
IJTAG	JTAG I/O quiescent current	Operational standby ⁴ , VJTAG = 3.63 V	T _J = 25°C		80	100	μΑ
			T _J = 85°C		80	100	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V			0	0	μA
IPP	Programming supply current	Non-programming mode, VPUMP = 3.63 V	T _J = 25°C		37	80	μA
			T _J = 85°C		37	80	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V			0	0	μA

Notes:

1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, and ICCI2.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.



Package Pin Assignments

	FG484		FG484		
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND	AA14	AG7	AG7
A2	VCC	NC	AA15	AG8	AG8
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0	AA16	GNDA	GNDA
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0	AA17	AG9	AG9
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0	AA18	VAREF	VAREF
A6	IO07NDB0V1	IO07NDB0V1	AA19	VCCIB2	VCCIB2
A7	IO07PDB0V1	IO07PDB0V1	AA20	PTEM	PTEM
A8	IO10PDB0V1	IO09PDB0V1	AA21	GND	GND
A9	IO14NDB0V1	IO13NDB0V2	AA22	VCC	NC
A10	IO14PDB0V1	IO13PDB0V2	AB1	GND	GND
A11	IO17PDB1V0	IO24PDB1V0	AB2	VCC	NC
A12	IO18PDB1V0	IO26PDB1V0	AB3	NC	IO94NSB4V0
A13	IO19NDB1V0	IO27NDB1V1	AB4	GND	GND
A14	IO19PDB1V0	IO27PDB1V1	AB5	VCC33N	VCC33N
A15	IO24NDB1V1	IO35NDB1V2	AB6	AT0	AT0
A16	IO24PDB1V1	IO35PDB1V2	AB7	ATRTN0	ATRTN0
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2	AB8	AT1	AT1
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2	AB9	AT2	AT2
A19	IO29NDB1V1	IO43NDB1V2	AB10	ATRTN1	ATRTN1
A20	IO29PDB1V1	IO43PDB1V2	AB11	AT3	AT3
A21	VCC	NC	AB12	AT6	AT6
A22	GND	GND	AB13	ATRTN3	ATRTN3
AA1	VCC	NC	AB14	AT7	AT7
AA2	GND	GND	AB15	AT8	AT8
AA3	VCCIB4	VCCIB4	AB16	ATRTN4	ATRTN4
AA4	VCCIB4	VCCIB4	AB17	AT9	AT9
AA5	PCAP	PCAP	AB18	VCC33A	VCC33A
AA6	AG0	AG0	AB19	GND	GND
AA7	GNDA	GNDA	AB20	NC	IO76NPB2V0
AA8	AG1	AG1	AB21	VCC	NC
AA9	AG2	AG2	AB22	GND	GND
AA10	GNDA	GNDA	B1	VCC	NC
AA11	AG3	AG3	B2	GND	GND
AA12	AG6	AG6	B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
AA13	GNDA	GNDA	B4	GND	GND



Datasheet Information

Revision	Changes	Page
Advance v1.0 (continued)	This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to V_{CC33A} .	3-8
Advance v0.9 (October 2007)	In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126	II
	In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pin: B25	3-2
	In the "180-Pin QFN" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS090: B29 AFS250: B29	3-4
	In the "208-Pin PQFP" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS090: 102 AFS250: 102	3-8
	In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14	3-12
Advance v0.9 (continued)	In the "484-Pin FBGA" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS600: AB18 AFS1500: AB18	3-20
	In the "676-Pin FBGA" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS1500: AD20	3-28
Advance v0.8 (June 2007)	Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC.	2-20, 2-21
	Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added.	2-25
	The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator.	2-22
	Table 2-11 \cdot Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of I _{DYNXTAL} for 0.032–0.2 MHz to 0.19.	2-24
	The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR.	2-41
	The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR.	2-41

Fusion Family of Mixed Signal FPGAs

Revision	Changes	Page
Advance v0.3	The "Temperature Monitor" section was updated.	
(continued)	EQ 2 is new.	2-103
	The "ADC Description" section was updated.	2-102
	Figure 2-16 • Fusion Clocking Options was updated.	2-20
	Table 2-46 · Analog Channel Specifications was updated.	2-118
	The notes in Table 2-72 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities were updated.	2-144
	The "Simultaneously Switching Outputs and PCB Layout" section is new.	2-149
	LVPECL and LVDS were updated in Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications.	2-157
	LVPECL and LVDS were updated in Table 2-82 • Fusion Pro I/O Attributes vs. I/O Standard Applications.	2-158
	The "Timing Model" was updated.	2-161
	All voltage-referenced Minimum and Maximum DC Input and Output Level tables were updated.	N/A
	All Timing Characteristic tables were updated	N/A
	Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated.	2-165
	Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated.	2-134
	Table 2-93 • I/O Output Buffer Maximum Resistances ¹ was updated.	2-171
	The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet.	2-211
	The "CoreMP7 and Cortex-M1 Software Tools" section is new.	2-257
	Table 2-83 • Summary of Maximum and Minimum DC Input and Output LevelsApplicable to Commercial and Industrial Conditions was updated.	2-165
	Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated.	2-134
	Table 2-93 • I/O Output Buffer Maximum Resistances ¹ was updated.	
	The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet.	2-211
	The "108-Pin QFN" table for the AFS090 device is new.	3-2
	The "180-Pin QFN" table for the AFS090 device is new.	3-4
	The "208-Pin PQFP" table for the AFS090 device is new.	3-8
	The "256-Pin FBGA" table for the AFS090 device is new.	3-12
	The "256-Pin FBGA" table for the AFS250 device is new.	3-12