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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/p1afs600-2fgg256

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Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
 - Flash memory blocks
 - FlashROM
 - SRAM and FIFO
- Clocking resources
 - PLL and CCC
 - RC oscillator
 - Crystal oscillator
 - No-Glitch MUX (NGMUX)
- Digital I/Os with advanced I/O standards
- FPGA VersaTiles
- Analog components
 - ADC
 - Analog I/Os supporting voltage, current, and temperature monitoring
 - 1.5 V on-board voltage regulator
 - Real-time counter

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic lookup table (LUT) equivalent or a D-flip-flop or latch (with or without enable) by programming the appropriate flash switch interconnections. This versatility allows efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi families of flash-based FPGAs. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid (3.3 V) single-voltage programming of Fusion devices via an IEEE 1532 JTAG interface.

Unprecedented Integration

Integrated Analog Blocks and Analog I/Os

Fusion devices offer robust and flexible analog mixed signal capability in addition to the highperformance flash FPGA fabric and flash memory block. The many built-in analog peripherals include a configurable 32:1 input analog MUX, up to 10 independent MOSFET gate driver outputs, and a configurable ADC. The ADC supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (Ksps), differential nonlinearity (DNL) < 1.0 LSB, and Total Unadjusted Error (TUE) of 0.72 LSB in 10-bit mode. The TUE is used for characterization of the conversion error and includes errors from all sources, such as offset and linearity. Internal bandgap circuitry offers 1% voltage reference accuracy with the flexibility of utilizing an external reference voltage. The ADC channel sampling sequence and sampling rate are programmable and implemented in the FPGA logic using Designer and Libero SoC software tool support.

Two channels of the 32-channel ADCMUX are dedicated. Channel 0 is connected internally to VCC and can be used to monitor core power supply. Channel 31 is connected to an internal temperature diode which can be used to monitor device temperature. The 30 remaining channels can be connected to external analog signals. The exact number of I/Os available for external connection signals is device-dependent (refer to the "Fusion Family" table on page I for details).

CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- · 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • PLL Block

Flash Memory Block Diagram

A simplified diagram of the flash memory block is shown in Figure 2-33.





The logic consists of the following sub-blocks:

Flash Array

Contains all stored data. The flash array contains 64 sectors, and each sector contains 33 pages of data.

Page Buffer

A page-wide volatile register. A page contains 8 blocks of data and an AUX block.

- Block Buffer
 - Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic

The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.



Device Architecture

The following error indications are possible for Read operations:

- 1. STATUS = '01' when a single-bit data error was detected and corrected within the block addressed.
- 2. STATUS = '10' when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in Table 2-23, and the definition of the page status bits is shown in Table 2-24.

Table 2-23 • Page Status Read Data Format

31	8	7	4	3	2	1	0
Write Count		Rese	erved	Over Threshold	Read Protected	Write Protected	Overwrite Protected

Table 2-24 • Page Status Bit Definition

Page Status Bit(s)	Definition
31–8	The number of times the page addressed has been programmed/erased
7–4	Reserved; read as 0
3	Over Threshold indicator (see the "Program Operation" section on page 2-46)
2	Read Protected; read protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
1	Write Protected; write protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
0	Overwrite Protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a Program operation. The page cannot be written without first performing an Unprotect Page operation.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven
 onto the RD bus in the same clock cycle following RA and REN valid. The read address is
 registered on the read port clock active edge, and data appears at RD after the RAM access time.
 Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is High. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "SRAM Characteristics" section on page 2-63 and the "FIFO Characteristics" section on page 2-72.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG IEEE 1532" section on page 2-229 and the *Fusion SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

ADC Terminology

Conversion Time

Conversion time is the interval between the release of the hold state (imposed by the input circuitry of a track-and-hold) and the instant at which the voltage on the sampling capacitor settles to within one LSB of a new input value.

DNL – Differential Non-Linearity

For an ideal ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB in defined as DNL (Figure 2-83).



Figure 2-83 • Differential Non-Linearity (DNL)

ENOB – Effective Number of Bits

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization of noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD (also see "Signal-to-Noise and Distortion Ratio (SINAD)".) ENOB for a full-scale, sinusoidal input waveform is computed using EQ 12.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

EQ 12

FS Error – Full-Scale Error

Full-scale error is the difference between the actual value that triggers that transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error.



Device Architecture

Table 2-52 • Calibrated Analog Channel Accuracy 1,2,3Worst-Case Industrial Conditions, TJ = 85°C

		Condition	Total	(LSB)			
Analog Pad	Prescaler Range (V)	Input Voltage ⁴ (V)	Negative Max.	Median	Positive Max.		
P	ositive Range		ADC in 10-Bit Mode				
AV, AC	16	0.300 to 12.0	-6	1	6		
	8	0.250 to 8.00	-6	0	6		
	4	0.200 to 4.00	-7	-1	7		
	2	0.150 to 2.00	-7	0	7		
	1	0.050 to 1.00	-6	-1	6		
AT	16	0.300 to 16.0	-5	0	5		
	4	0.100 to 4.00	-7	-1	7		
Ne	egative Range		ADC in 10-Bit Mode				
AV, AC	16	-0.400 to -10.5	-7	1	9		
	8	-0.350 to -8.00	-7	-1	7		
	4	-0.300 to -4.00	-7	-2	9		
	2	-0.250 to -2.00	-7	-2	7		
	1	-0.050 to -1.00	-16	-1	20		

Notes:

1. Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Overall accuracy remains the same.

2. Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.

3. Calibrated with two-point calibration methodology, using 20% and 80% full-scale points.

4. The lower limit of the input voltage is determined by the prescaler input offset.



Device Architecture

Table 2-73 • Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os; All I/O Bank Types (maximum drive strength and high slew selected)

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
LVPECL	300 MHz



Figure 2-102 • DDR Output Support in Fusion Devices

User I/O Naming Convention

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

- G = Global
- m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).
- n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-22 on page 2-25 shows the three input pins per clock source MUX at CCC location m.
- u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.
- x = P (Positive) or N (Negative) for differential pairs, or R (Regular single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as an LVPECL pair.
- w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

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B = Bank
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- y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.
- V = Reference voltage
- z = Minibank number



Standard I/O Bank

Figure 2-113 • Naming Conventions of Fusion Devices with Three Digital I/O Banks

Fusion Family of Mixed Signal FPGAs



Figure 2-117 • Output Buffer Model and Delays (example)

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-90 • Summary of AC Measuring Points Applicable to All I/O Bank Types

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	_	-	1.4 V
2.5 V LVCMOS	_	-	1.2 V
1.8 V LVCMOS	-	-	0.90 V
1.5 V LVCMOS	_	-	0.75 V
3.3 V PCI	_	_	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	_	_	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	-	-	Cross point
LVPECL	-	-	Cross point

Table 2-91 • I/O AC Parameter Definitions

Parameter	Definition
t _{DP}	Data to Pad delay through the Output Buffer
t _{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t _{DOUT}	Data to Output Buffer delay through the I/O interface
t _{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t _{DIN}	Input Buffer to Data delay through the I/O interface
t _{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t _{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t _{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t _{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t _{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t _{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t _{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-132 • 1.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	12.33	0.04	1.42	0.43	11.79	12.33	2.45	2.32	ns
	-1	0.56	10.49	0.04	1.21	0.36	10.03	10.49	2.08	1.98	ns
	-2	0.49	9.21	0.03	1.06	0.32	8.81	9.21	1.83	1.73	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-133 • 1.5 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	7.65	0.04	1.42	0.43	6.31	7.65	2.45	2.45	ns
	-1	0.56	6.50	0.04	1.21	0.36	5.37	6.50	2.08	2.08	ns
	-2	0.49	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



3 – DC and Power Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-3.

Symbol	Parameter	Commercial	Industrial	Units		
VCC	DC core supply voltage	-0.3 to 1.65	–0.3 to 1.65	V		
VJTAG	JTAG DC voltage	-0.3 to 3.75	-0.3 to 3.75	V		
VPUMP	Programming voltage	-0.3 to 3.75	-0.3 to 3.75	V		
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	-0.3 to 1.65	V		
VCCI	DC I/O output buffer supply voltage	-0.3 to 3.75	-0.3 to 3.75	V		
VI	I/O input voltage ¹	 -0.3 V to 3.6 V (when I/O hot insertion mode is enabled) -0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) 				
VCC33A	+3.3 V power supply	–0.3 to 3.75 ²	–0.3 to 3.75 ²	V		
VCC33PMP	+3.3 V power supply	-0.3 to 3.75 ²	-0.3 to 3.75 ²	V		
VAREF	Voltage reference for ADC	-0.3 to 3.75	-0.3 to 3.75	V		
VCC15A	Digital power supply for the analog system	-0.3 to 1.65	–0.3 to 1.65	V		
VCCNVM	Embedded flash power supply	-0.3 to 1.65	-0.3 to 1.65	V		
VCCOSC	Oscillator power supply	-0.3 to 3.75	-0.3 to 3.75	V		

Table 3-1 • Absolute Maximum Ratings

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-4.

2. Analog data not valid beyond 3.65 V.

3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.

4. For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.



DC and Power Characteristics

Parameter	Description	Conditions	Temp.	Min	Тур	Мах	Unit
IPP	Programming supply	Non-programming mode,	T _J = 25°C		36	80	μA
	current	VPUMP = 3.63 V	T _J = 85°C		36	80	μA
			T _J = 100°C		36	80	μA
		Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V			0	0	μA
ICCNVM	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T _J = 25°C		22	80	μA
			T _J = 85°C		24	80	μA
			T _J = 100°C		25	80	μA
ICCPLL	1.5 V PLL quiescent current	Operational standby,	T _J = 25°C		130	200	μA
		VCCPLL = 1.575 V	T _J = 85°C		130	200	μA
			T _J = 100°C		130	200	μA

Table 3-9 • AFS600 Quiescent Supply Current Characteristics (continued)

Notes:

- 1. ICC is the 1.5 V power supplies, ICC and ICC15A.
- 2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
- 3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.
- 4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
- 5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
- 6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

RAM Dynamic Contribution—P_{MEMORY}

Operating Mode

 $P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE-CLOCK})$ $N_{BLOCKS} \text{ is the number of RAM blocks used in the design.}$

F_{READ-CLOCK} is the memory read clock frequency.

 β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-17 on page 3-27.

 β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-17 on page 3-27.

 $\mathsf{F}_{\mathsf{WRITE}\text{-}\mathsf{CLOCK}}$ is the memory write clock frequency.

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W

PLL/CCC Dynamic Contribution—PPLL

Operating Mode

P_{PLL} = PAC13 * F_{CLKOUT}

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Standby Mode and Sleep Mode

 $P_{PLL} = 0 W$

Nonvolatile Memory Dynamic Contribution—P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

 $P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * PAC15 * F_{READ-NVM}$ when $F_{READ-NVM} \le 33$ MHz,

 $P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * (PAC16 + PAC17 * F_{READ-NVM} \text{ when } F_{READ-NVM} > 33 \text{ MHz}$

N_{NVM-BLOCKS} is the number of NVM blocks used in the design (2 inAFS600).

 β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state). F_{READ-NVM} is the NVM read clock frequency.

Standby Mode and Sleep Mode

P_{NVM} = 0 W

Crystal Oscillator Dynamic Contribution—P_{XTL-OSC}

Operating Mode

 $P_{XTL-OSC} = PAC18$

Standby Mode

 $P_{XTL-OSC} = PAC18$

Sleep Mode

 $P_{XTL-OSC} = 0 W$

The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution (P_{AC14} * F_{CLKOUT} product) to the total PLL contribution.



Package Pin Assignments

	PQ208			PQ208	
Pin Number	AFS250 Function	AFS600 Function	Pin Number	AFS250 Function	AFS600 Function
147	GCC1/IO47PDB1V0	IO39NDB2V0	184	IO18RSB0V0	IO10PPB0V1
148	IO42NDB1V0	GCA2/IO39PDB2V0	185	IO17RSB0V0	IO09PPB0V1
149	GBC2/IO42PDB1V0	IO31NDB2V0	186	IO16RSB0V0	IO10NPB0V1
150	VCCIB1	GBB2/IO31PDB2V0	187	IO15RSB0V0	IO09NPB0V1
151	GND	IO30NDB2V0	188	VCCIB0	IO08PPB0V1
152	VCC	GBA2/IO30PDB2V0	189	GND	IO07PPB0V1
153	IO41NDB1V0	VCCIB2	190	VCC	IO08NPB0V1
154	GBB2/IO41PDB1V0	GNDQ	191	IO14RSB0V0	IO07NPB0V1
155	IO40NDB1V0	VCOMPLB	192	IO13RSB0V0	IO06PPB0V0
156	GBA2/IO40PDB1V0	VCCPLB	193	IO12RSB0V0	IO05PPB0V0
157	GBA1/IO39RSB0V0	VCCIB1	194	IO11RSB0V0	IO06NPB0V0
158	GBA0/IO38RSB0V0	GNDQ	195	IO10RSB0V0	IO04PPB0V0
159	GBB1/IO37RSB0V0	GBB1/IO27PPB1V1	196	IO09RSB0V0	IO05NPB0V0
160	GBB0/IO36RSB0V0	GBA1/IO28PPB1V1	197	IO08RSB0V0	IO04NPB0V0
161	GBC1/IO35RSB0V0	GBB0/IO27NPB1V1	198	IO07RSB0V0	GAC1/IO03PDB0V0
162	VCCIB0	GBA0/IO28NPB1V1	199	IO06RSB0V0	GAC0/IO03NDB0V0
163	GND	VCCIB1	200	GAC1/IO05RSB0V0	VCCIB0
164	VCC	GND	201	VCCIB0	GND
165	GBC0/IO34RSB0V0	VCC	202	GND	VCC
166	IO33RSB0V0	GBC1/IO26PDB1V1	203	VCC	GAB1/IO02PDB0V0
167	IO32RSB0V0	GBC0/IO26NDB1V1	204	GAC0/IO04RSB0V0	GAB0/IO02NDB0V0
168	IO31RSB0V0	IO24PPB1V1	205	GAB1/IO03RSB0V0	GAA1/IO01PDB0V0
169	IO30RSB0V0	IO23PPB1V1	206	GAB0/IO02RSB0V0	GAA0/IO01NDB0V0
170	IO29RSB0V0	IO24NPB1V1	207	GAA1/IO01RSB0V0	GNDQ
171	IO28RSB0V0	IO23NPB1V1	208	GAA0/IO00RSB0V0	VCCIB0
172	IO27RSB0V0	IO22PPB1V0			
173	IO26RSB0V0	IO21PPB1V0			
174	IO25RSB0V0	IO22NPB1V0			
175	VCCIB0	IO21NPB1V0			
176	GND	IO20PSB1V0			
177	VCC	IO19PSB1V0			
178	IO24RSB0V0	IO14NSB0V1			
179	IO23RSB0V0	IO12PDB0V1			
180	IO22RSB0V0	IO12NDB0V1			
181	IO21RSB0V0	VCCIB0			
182	IO20RSB0V0	GND			
183	IO19RSB0V0	VCC			

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FG676		FG676		
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	
AD5	IO94NPB4V0	AE15	GNDA	
AD6	GND	AE16	NC	
AD7	VCC33N	AE17	NC	
AD8	AT0	AE18	GNDA	
AD9	ATRTN0	AE19	NC	
AD10	AT1	AE20	NC	
AD11	AT2	AE21	NC	
AD12	ATRTN1	AE22	NC	
AD13	AT3	AE23	NC	
AD14	AT6	AE24	NC	
AD15	ATRTN3	AE25	GND	
AD16	AT7	AE26	GND	
AD17	AT8	AF1	NC	
AD18	ATRTN4	AF2	GND	
AD19	AT9	AF3	NC	
AD20	VCC33A	AF4	NC	
AD21	GND	AF5	NC	
AD22	IO76NPB2V0	AF6	NC	
AD23	NC	AF7	NC	
AD24	GND	AF8	NC	
AD25	NC	AF9	VCC33A	
AD26	NC	AF10	NC	
AE1	GND	AF11	NC	
AE2	GND	AF12	VCC33A	
AE3	NC	AF13	NC	
AE4	NC	AF14	NC	
AE5	NC	AF15	VCC33A	
AE6	NC	AF16	NC	
AE7	NC	AF17	NC	
AE8	NC	AF18	VCC33A	
AE9	GNDA	AF19	NC	
AE10	NC	AF20	NC	
AE11	NC	AF21	NC	
AE12	GNDA	AF22	NC	
AE13	NC	AF23	NC	
AE14	NC	AF24	NC	

FG676				
Pin Number	AFS1500 Function			
AF25	GND			
AF26	NC			
B1	GND			
B2	GND			
B3	NC			
B4	NC			
B5	NC			
B6	VCCIB0			
B7	NC			
B8	NC			
B9	VCCIB0			
B10	IO15NDB0V2			
B11	IO15PDB0V2			
B12	VCCIB0			
B13	IO19NDB0V2			
B14	IO19PDB0V2			
B15	VCCIB1			
B16	IO25NDB1V0			
B17	IO25PDB1V0			
B18	VCCIB1			
B19	IO33NDB1V1			
B20	IO33PDB1V1			
B21	VCCIB1			
B22	NC			
B23	NC			
B24	NC			
B25	GND			
B26	GND			
C1	NC			
C2	NC			
C3	GND			
C4	NC			
C5	GAA1/IO01PDB0V0			
C6	GAB0/IO02NDB0V0			
C7	GAB1/IO02PDB0V0			
C8	IO07NDB0V1			

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

Revision	Changes	Page
Revision 6 (March 2014)	Note added for the discontinuance of QN108 and QN180 packages to the "Package I/Os: Single-/Double-Ended (Analog)" table and the "Temperature Grade Offerings" table (SAR 55113, PDN 1306).	II and IV
	Updated details about page programming time in the "Program Operation" section (SAR 49291).	
	ADC_START changed to ADCSTART in the "ADC Operation" section (SAR 44104).	2-104
Revision 5 (January 2014)	Calibrated offset values (AFS090, AFS250) of the external temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 51464).	2-117
	Specifications for the internal temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 50870).	2-117
Revision 4 (January 2013)	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43177).	Ш
	The note in Table 2-12 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42563).	2-28
	Table 2-49 • Analog Channel Specifications was modified to update the uncalibrated offset values (AFS250) of the external and internal temperature monitors (SAR 43134).	2-117
	In Table 2-57 • Prescaler Control Truth Table—AV ($x = 0$), AC ($x = 1$), and AT ($x = 3$), changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 20812).	2-130
	The values for the Speed Grade (-1 and Std.) for FDDRIMAX (Table 2-180 • Input DDR Propagation Delays) and values for the Speed Grade (-2 and Std.) for FDDOMAX (Table 2-182 • Output DDR Propagation Delays) had been inadvertently interchanged. This has been rectified (SAR 38514).	2-220, 2-222
	Added description about what happens if a user connects VAREF to an external 3.3 V on their board to the "VAREF Analog Reference Voltage" section (SAR 35188).	2-225
	Added a note to Table 3-2 • Recommended Operating Conditions1 (SAR 43429): The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.	3-3
	Added the Package Thermal details for AFS600-PQ208 and AFS250-PQ208 to Table 3-6 • Package Thermal Resistance (SAR 37816). Deleted the Die Size column from the table (SAR 43503).	3-7
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 42495).	NA
Devision 0	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	1 . 15.7
Revision 3 (August 2012)	Microblade U1AFS250 and U1AFS1500 devices were added to the product tables.	I – IV
	A sentence pertaining to the analog I/Os was added to the "Specifying I/O States During Programming" section (SAR 34831).	1-9



Datasheet Information

Revision	Changes	Page
v2.0, Revision 1	Table 3-6 • Package Thermal Resistance was updated to include new data.	
(continued)	In EQ 4 to EQ 6, the junction temperature was changed from 110°C to 100°C.	3-8 to 3-8
	Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics are new and have replaced the Quiescent Supply Current Characteristics (IDDQ) table.	3-10 to 3-16
	In Table 3-14 • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices, the power supply for PAC9 and PAC10 were changed from VMV/VCC to VCCI.	3-22
	In Table 3-15 • Different Components Contributing to the Static Power Consumption in Fusion Devices, the power supply for PDC7 and PDC8 were changed from VMV/VCC to VCCI. PDC1 was updated from TBD to 18.	3-23
	The "QN108" table was updated to remove the duplicates of pins B12 and B34.	4-2
Preliminary v1.7 (October 2008)	The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.	
	For the VIL and VIH parameters, 0.30 * VCCI was changed to 0.35 * VCCI and 0.70 * VCCI was changed to 0.65 * VCCI in Table 2-126 • Minimum and Maximum DC Input and Output Levels.	2-193
	The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.	N/A
	The following updates were made to Table 2-141 • Minimum and Maximum DC Input and Output Levels:	2-200
	Temperature Digital Output	
	213 00 1111 1101	
	283 01 0001 1011	
	3580101100110– only the digital output was updated.Temperature 358 remains in the temperature column.	
	In Advance v1.2, the "VAREF Analog Reference Voltage" pin description was significantly updated but the change was not noted in the change table.	2-225
Advance v1.6 (August 2008)	The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA.	N/A
	The references to the <i>Peripherals User's Guide</i> in the "No-Glitch MUX (NGMUX)" section and "Voltage Regulator Power Supply Monitor (VRPSM)" section were changed to <i>Fusion Handbook</i> .	2-32, 2-42
Advance v1.5 (July 2008)	The following bullet was updated from High-Voltage Input Tolerance: ±12 V to High-Voltage Input Tolerance: 10.5 V to 12 V.	I
	The following bullet was updated from Programmable 1, 3, 10, 30 μ A and 25 mA Drive Strengths to Programmable 1, 3, 10, 30 μ A and 20 mA Drive Strengths.	I