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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/u1afs250-fg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Temperature Grade Offerings

Fusion Devices	AFS090	AFS250	AFS600	AFS1500		
ARM Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500		
Pigeon Point Devices			P1AFS600 ³	P1AFS1500 ³		
MicroBlade Devices		U1AFS250 ⁴	U1AFS600 ⁴	U1AFS1500 ⁴		
QN108 ⁵	C, I	-	-	_		
QN180 ⁵	C, I	C, I	-	-		
PQ208	-	C, I	C, I	-		
FG256	C, I	C, I	C, I	C, I		
FG484	-	-	C, I	C, I		
FG676	-	-	-	C, I		

Notes:

1. C = Commercial Temperature Range: 0°C to 85°C Junction

2. I = Industrial Temperature Range: -40°C to 100°C Junction

3. Pigeon Point devices are only offered in FG484 and FG256.

4. MicroBlade devices are only offered in FG256.

5. Package not available.

Speed Grade and Temperature Grade Matrix

	Std. ¹	-1	-2 ²
C ³	\checkmark	\checkmark	\checkmark
l ⁴	\checkmark	\checkmark	\checkmark

Notes:

1. MicroBlade devices are only offered in standard speed grade.

2. Pigeon Point devices are only offered in –2 speed grade.

3. C = Commercial Temperature Range: 0°C to 85°C Junction

4. I = Industrial Temperature Range: -40°C to 100°C Junction

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/index.php?option=com_content&id=137&lang=en&view=article.

Cortex-M1, Pigeon Point, and MicroBlade Fusion Device Information

This datasheet provides information for all Fusion (AFS), Cortex-M1 (M1), Pigeon Point (P1), and MicroBlade (U1) devices. The remainder of the document will only list the Fusion (AFS) devices. Please apply relevant information to M1, P1, and U1 devices when appropriate. Please note the following:

- Cortex-M1 devices are offered in the same speed grades and packages as basic Fusion devices.
- Pigeon Point devices are only offered in –2 speed grade and FG484 and FG256 packages.
- MicroBlade devices are only offered in standard speed grade and the FG256 package.

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Figure 2-4 • Combinatorial Timing Model and Waveforms



Figure 2-10 • Very-Long-Line Resources

VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, Table 2-7, and Table 2-8 on page 2-17 present minimum and maximum global clock delays within the device Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

 Table 2-5 • AFS1500 Global Resource Timing

 Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	_	2	_	1	S	Unite	
Farameter	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.53	1.75	1.74	1.99	2.05	2.34	ns
t _{RCKH}	Input High Delay for Global Clock	1.53	1.79	1.75	2.04	2.05	2.40	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-6 • AFS600 Global Resource Timing

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Paramotor	Description	-	2	-	-1	S	Units		
Falailletei	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	onito	
t _{RCKL}	Input Low Delay for Global Clock	1.27	1.49	1.44	1.70	1.69	2.00	ns	
t _{RCKH}	Input High Delay for Global Clock	1.26	1.54	1.44	1.75	1.69	2.06	ns	
t _{RCKMPWH}	RCKMPWH Minimum Pulse Width High for Global Clock							ns	
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns	
t _{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.36	ns	

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

CCC and PLL Characteristics

Timing Characteristics

Table 2-12 • Fusion CCC/PLL Specification

Parameter	Min.	Тур.	Max.	Unit
Clock Conditioning Circuitry Input Frequency fIN_CCC	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f _{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		160 ³		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F _{CCC_OUT}	Max Pea	k-to-Peak Po	eriod Jitter	
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	1.00%		1.00%	
24 MHz to 100 MHz	1.50%		1.50%	
100 MHz to 250 MHz	2.25%		2.25%	
250 MHz to 350 MHz	3.50%		3.50%	
Acquisition Time LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁴ LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1,2}	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 ^{1, 2}	0.025		5.56	ns
Delay Range in Block: Fixed Delay ^{1, 2}		2.2		ns

Notes:

1. This delay is a function of voltage and temperature. See Table 3-7 on page 3-9 for deratings.

2. $T_J = 25^{\circ}C$, VCC = 1.5 V

3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

4. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.

Program Operation

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, the total programming (including erase) time per page of the eNVM is 6.8 ms. While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified. Program errors include the following:

- 1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
- 2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
- Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
- 4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
- 5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
- 6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
- 7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in Figure 2-36.



Figure 2-36 • FB Program Waveform

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.



Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.



Figure 2-47 • Fusion RAM Block with Embedded FIFO Controller

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage-monitoring capabilities unique in the FPGA industry. The Analog Quad comprises three analog input pads— Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-66), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.



Figure 2-66 • Analog Quad Direct Connect

The Analog Quad offers a wide variety of prescaling options to enable the ADC to resolve the input signals. Figure 2-67 shows the path through the Analog Quad for a signal that is to be prescaled prior to conversion. The ADC internal reference voltage and the prescaler factors were selected to make both prescaling and postscaling of the signals easy binary calculations (refer to Table 2-57 on page 2-130 for details). When an analog input pad is configured with a prescaler, there will be a 1 M Ω resistor to ground. This occurs even when the device is in power-down mode. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, analog inputs are pulled down to ground through a 1 M Ω resistor. The gate driver output is floating (or tristated), and there is no extra current on VCC33A.

These scaling factors hold true whether the particular pad is configured to accept a positive or negative voltage. Note that whereas the AV and AC pads support the same prescaling factors, the AT pad supports a reduced set of prescaling factors and supports positive voltages only.



To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least t_{CMSLO} in order to discharge the previous measurement. Then CMSTB must be asserted high for at least t_{CMSET} prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is de-asserted by the AB macro. Note that the minimum sample time cannot be less than t_{CMSHI} . Figure 2-71 shows the timing diagram of CMSTB in relationship with the ADC control signals.



Figure 2-71 • Timing Diagram for Current Monitor Strobe

Figure 2-72 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050 Ω sense resistor, The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$||| = (ADC \times V_{AREF}) / (10 \times 2^{N} \times R_{sense})$$

EQ 3

where

I is the current flowing through the sense resistor

ADC is the result from the ADC

VAREF is the Reference voltage

N is the number of bits

Rsense is the resistance of the sense resistor



Figure 2-72 • Positive Current Monitor

Care must be taken when choosing the right resistor for current measurement application. Note that because of the 10× amplification, the maximum measurable difference between the AV and AC pads is V_{AREF} / 10. A larger AV-to-AC voltage drop will result in ADC saturation; that is, the digital code put out by the ADC will stay fixed at the full scale value. Therefore, the user must select the external sense resistor appropriately. Table 2-38 shows recommended resistor values for different current measurement ranges. When choosing resistor values for a system, there is a trade-off between measurement accuracy and power consumption. Choosing a large resistor will increase the voltage drop and hence increase accuracy of the measurement; however the larger voltage drop dissipates more power (P = I² × R).

The Current Monitor is a unipolar system, meaning that the differential voltage swing must be from 0 V to $V_{AREF}/10$. Therefore, the Current Monitor only supports differential voltage where $|V_{AV}-V_{AC}|$ is greater than 0 V. This results in the requirement that the potential of the AV pad must be larger than the potential of the AC pad. This is straightforward for positive voltage systems. For a negative voltage system, it means that the AV pad must be "more negative" than the AC pad. This is shown in Figure 2-73.

In this case, both the AV pad and the AC pad are configured for negative operations and the output of the differential amplifier still falls between 0 V and V_{AREF} as required.

Current Range	Recommended Minimum Resistor Value (Ohms)
> 5 mA – 10 mA	10 – 20
> 10 mA – 20 mA	5 – 10
> 20 mA – 50 mA	2.5 – 5
> 50 mA – 100 mA	1 – 2
> 100 mA – 200 mA	0.5 – 1
> 200 mA – 500 mA	0.3 – 0.5
> 500 mA – 1 A	0.1 – 0.2
> 1 A – 2 A	0.05 – 0.1
> 2 A – 4 A	0.025 – 0.05
> 4 A – 8 A	0.0125 – 0.025
> 8 A – 12 A	0.00625 – 0.02

Table 2-37 • Recommended Resistor for Different Current Range Measurement



Device Architecture

Refer to Table 2-46 on page 2-109 and the "Acquisition Time or Sample Time Control" section on page 2-107

$$t_{sample} = (2 + STC) \times t_{ADCCLK}$$

EQ 20

STC: Sample Time Control value (0–255)

t_{SAMPLE} is the sample time

Table 2-46 • STC Bits Function

Name	Bits	Function
STC	[7:0]	Sample time control

Sample time is computed based on the period of ADCCLK.

Distribution Phase

The second phase is called the distribution phase. During distribution phase, the ADC computes the equivalent digital value from the value stored in the input capacitor. In this phase, the output signal SAMPLE goes back to '0', indicating the sample is completed; but the BUSY signal remains '1', indicating the ADC is still busy for distribution. The distribution time depends strictly on the number of bits. If the ADC is configured as a 10-bit ADC, then 10 ADCCLK cycles are needed. EQ 8 describes the distribution time.

$$t_{distrib} = N \times t_{ADCCLK}$$

EQ 21

N: Number of bits

Post-Calibration Phase

The last phase is the post-calibration phase. This is an optional phase. The post-calibration phase takes two ADCCLK cycles. The output BUSY signal will remain '1' until the post-calibration phase is completed. If the post-calibration phase is skipped, then the BUSY signal goes to '0' after distribution phase. As soon as BUSY signal goes to '0', the DATAVALID signal goes to '1', indicating the digital result is available on the RESULT output signals. DATAVAILD will remain '1' until the next ADCSTART is asserted. Microsemi recommends enabling post-calibration to compensate for drift and temperature-dependent effects. This ensures that the ADC remains consistent over time and with temperature. The post-calibration phase is enabled by bit 3 of the Mode register. EQ 9 describes the post-calibration time.

$$t_{post-cal} = MODE[3] \times (2 \times t_{ADCCLK})$$

EQ 22

EQ 23

MODE[3]: Bit 3 of the Mode register, described in Table 2-41 on page 2-106.

The calculation for the conversion time for the ADC is summarized in EQ 23.

 $t_{conv} = t_{sync_read} + t_{sample} + t_{distrib} + t_{post-cal} + t_{sync_write}$

t_{conv}: conversion time

 t_{sync_read} : maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK} .

t_{sample}: Sample time

t_{distrib}: Distribution time

tpost-cal: Post-calibration time

 t_{sync_write} : Maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK} .

Intra-Conversion

Performing a conversion during power-up calibration is possible but should be avoided, since the performance is not guaranteed, as shown in Table 2-49 on page 2-117. This is described as intra-conversion. Figure 2-92 on page 2-113 shows intra-conversion, (conversion that starts during power-up calibration).

Injected Conversion

A conversion can be interrupted by another conversion. Before the current conversion is finished, a second conversion can be started by issuing a pulse on signal ADCSTART. When a second conversion is issued before the current conversion is completed, the current conversion would be dropped and the ADC would start the second conversion on the rising edge of the SYSCLK. This is known as injected conversion. Since the ADC is synchronous, the minimum time to issue a second conversion is two clock cycles of SYSCLK after the previous one. Figure 2-93 on page 2-113 shows injected conversion, (conversion that starts before a previously started conversion is finished). The total time for calibration still remains 3,840 ADCCLK cycles.

ADC Example

This example shows how to choose the correct settings to achieve the fastest sample time in 10-bit mode for a system that runs at 66 MHz. Assume the acquisition times defined in Table 2-44 on page 2-108 for 10-bit mode, which gives 0.549 µs as a minimum hold time.

The period of SYSCLK: $t_{SYSCLK} = 1/66$ MHz = 0.015 μ s

Choosing TVC between 1 and 33 will meet the maximum and minimum period for the ADCCLK requirement. A higher TVC leads to a higher ADCCLK period.

The minimum TVC is chosen so that $t_{distrib}$ and $t_{post-cal}$ can be run faster. The period of ADCCLK with a TVC of 1 can be computed by EQ 24.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK} = 4 \times (1 + 1) \times 0.015 \ \mu s = 0.12 \ \mu s$$

EQ 24

The STC value can now be computed by using the minimum sample/hold time from Table 2-44 on page 2-108, as shown in EQ 25.

STC =
$$\frac{t_{sample}}{t_{ADCCLK}} - 2 = \frac{0.549 \ \mu s}{0.12 \ \mu s} - 2 = 4.575 - 2 = 2.575$$

EQ 25

You must round up to 3 to accommodate the minimum sample time requirement. The actual sample time, t_{sample} , with an STC of 3, is now equal to 0.6 μ s, as shown in EQ 26

$$t_{sample} = (2 + STC) \times t_{ADCCLK} = (2 + 3) \times t_{ADCCLK} = 5 \times 0.12 \ \mu s = 0.6 \ \mu s$$

EQ 26

Microsemi recommends post-calibration for temperature drift over time, so post-calibration is enabled. The post-calibration time, $t_{post-cal}$, can be computed by EQ 27. The post-calibration time is 0.24 µs.

$$t_{post-cal} = 2 \times t_{ADCCLK} = 0.24 \ \mu s$$

EQ 27

The distribution time, $t_{distrib}$, is equal to 1.2 µs and can be computed as shown in EQ 28 (N is number of bits, referring back to EQ 8 on page 2-94).

$$_{\text{distrib}} = N \times t_{\text{ADCCLK}} = 10 \times 0.12 = 1.2 \, \mu \text{s}$$

t

EQ 28

The total conversion time can now be summated, as shown in EQ 29 (referring to EQ 23 on page 2-109).

 $t_{sync_read} + t_{sample} + t_{distrib} + t_{post-cal} + t_{sync_write} = (0.015 + 0.60 + 1.2 + 0.24 + 0.015) \ \mu s = 2.07 \ \mu s = EQ \ 29$

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-4. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-105. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.





Solution 4



Figure 2-106 • Solution 4



Device Architecture

Table 2-85 • Fusion Pro I/O Attributes vs. I/O Standard Applications

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3	3	3	3	3
PCI (3.3 V)			3		3	3	3	3		
PCI-X (3.3 V)	3		3		3	3	3	3		
GTL+ (3.3 V)			3		3	3	3	3		3
GTL+ (2.5 V)			3		3	3	3	3		3
GTL (3.3 V)			3		3	3	3	3		3
GTL (2.5 V)			3		3	3	3	3		3
HSTL Class I			3		3	3	3	3		3
HSTL Class II			3		3	3	3	3		3
SSTL2 Class I and II			3		3	3	3	3		3
SSTL3 Class I and II			3		3	3	3	3		3
LVDS, BLVDS, M-LVDS			3			3	3	3		3
LVPECL						3	3	3		3

Parameter	Description	Conditions	Temp.	Min	Тур	Мах	Unit
ICC ¹	1.5 V quiescent current	Operational standby ⁴ ,	T _J = 25°C		5	7.5	mA
		VCC = 1.575 V	T _J = 85°C		6.5	20	mA
			T _J = 100°C		14	48	mA
		Standby mode ⁵ or Sleep mode ⁶ , V _{CC} = 0 V			0	0	μA
ICC33 ²	3.3 V analog supplies current	Operational standby ⁴ , VCC33 = 3.63 V	T _J = 25°C		9.8	12	mA
			T _J = 85°C		9.8	12	mA
			T _J = 100°C		10.7	15	mA
		Operational standby, only	T _J = 25°C		0.30	2	mA
		output ON, VCC33 = 3.63 V	T _J = 85°C		0.30	2	mA
			T _J = 100°C		0.45	2	mA
		Standby mode ⁵ ,	T _J = 25°C		2.9	2.9	mA
		VCC33 = 3.63 V	T _J = 85°C		2.9	3.0	mA
			T _J = 100°C		3.5	6	mA
		Sleep mode ⁶ , VCC33 = 3.63 V	T _J = 25°C		17	18	μΑ
			T _J = 85°C		18	20	μA
			T _J = 100°C		24	25	μA
ICCI ³	I/O quiescent current	Operational standby ⁶ ,	T _J = 25°C		260	437	μΑ
		$V \cup U X = 3.03 V$	T _J = 85°C		260	437	μΑ
			T _J = 100°C		260	437	μA
IJTAG	JTAG I/O quiescent current	Operational standby ⁴ ,	T _J = 25°C		80	100	μΑ
		VJTAG = 3.63 V	T _J = 85°C		80	100	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V			0	0	μA
IPP	Programming supply current	Non-programming mode, VPUMP = 3.63 V	T _J = 25°C		37	80	μA
			T _J = 85°C		37	80	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V			0	0	μA

Notes:

1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, and ICCI2.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

FG484			FG484			
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function	
H13	GND	GND	K4	IO75NDB4V0	IO110NDB4V0	
H14	VCCIB1	VCCIB1	K5	GND	GND	
H15	GND	GND	K6	NC	IO104NDB4V0	
H16	GND	GND	K7	NC	IO111NDB4V0	
H17	NC	IO53NDB2V0	K8	GND	GND	
H18	IO38PDB2V0	IO57PDB2V0	K9	VCC	VCC	
H19	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0	K10	GND	GND	
H20	VCCIB2	VCCIB2	K11	VCC	VCC	
H21	IO37NDB2V0	IO54NDB2V0	K12	GND	GND	
H22	IO37PDB2V0	IO54PDB2V0	K13	VCC	VCC	
J1	NC	IO112PPB4V0	K14	GND	GND	
J2	IO76NDB4V0	IO113NDB4V0	K15	GND	GND	
J3	GFB2/IO74PDB4V0	GFB2/IO109PDB4V0	K16	IO40NDB2V0	IO60NDB2V0	
J4	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0	K17	NC	IO58PDB2V0	
J5	NC	IO112NPB4V0	K18	GND	GND	
J6	NC	IO104PDB4V0	K19	NC	IO68NPB2V0	
J7	NC	IO111PDB4V0	K20	IO41NDB2V0	IO61NDB2V0	
J8	VCCIB4	VCCIB4	K21	GND	GND	
J9	GND	GND	K22	IO42NDB2V0	IO56NDB2V0	
J10	VCC	VCC	L1	IO73NDB4V0	IO108NDB4V0	
J11	GND	GND	L2	VCCOSC	VCCOSC	
J12	VCC	VCC	L3	VCCIB4	VCCIB4	
J13	GND	GND	L4	XTAL2	XTAL2	
J14	VCC	VCC	L5	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0	
J15	VCCIB2	VCCIB2	L6	VCCIB4	VCCIB4	
J16	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0	L7	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0	
J17	NC	IO58NDB2V0	L8	VCCIB4	VCCIB4	
J18	IO38NDB2V0	IO57NDB2V0	L9	GND	GND	
J19	IO39NDB2V0	IO59NDB2V0	L10	VCC	VCC	
J20	GCC2/IO41PDB2V0	GCC2/IO61PDB2V0	L11	GND	GND	
J21	NC	IO55PSB2V0	L12	VCC	VCC	
J22	IO42PDB2V0	IO56PDB2V0	L13	GND	GND	
K1	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0	L14	VCC	VCC	
K2	GND	GND	L15	VCCIB2	VCCIB2	
K3	IO74NDB4V0	IO109NDB4V0	L16	IO48PDB2V0	IO70PDB2V0	

Fusion Family of Mixed Signal FPGAs

FG676			FG676	FG676		
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	
R21	IO72NDB2V0	U5	VCCIB4	V15	AC5	
R22	IO72PDB2V0	U6	IO91PDB4V0	V16	NC	
R23	GND	U7	IO91NDB4V0	V17	GNDA	
R24	IO71PDB2V0	U8	IO92PDB4V0	V18	IO77PPB2V0	
R25	VCCIB2	U9	GND	V19	IO74PDB2V0	
R26	IO67NDB2V0	U10	GND	V20	VCCIB2	
T1	GND	U11	VCC33A	V21	IO82NDB2V0	
T2	NC	U12	GNDA	V22	GDA2/IO82PDB2V0	
Т3	GFA1/IO105PDB4V0	U13	VCC33A	V23	GND	
T4	GFA0/IO105NDB4V0	U14	GNDA	V24	GDC1/IO79PDB2V0	
T5	IO101NDB4V0	U15	VCC33A	V25	VCCIB2	
Т6	IO96PDB4V0	U16	GNDA	V26	NC	
Τ7	IO96NDB4V0	U17	VCC	W1	GND	
Т8	IO99NDB4V0	U18	GND	W2	IO94PPB4V0	
Т9	IO97NDB4V0	U19	IO74NDB2V0	W3	IO98PDB4V0	
T10	VCCIB4	U20	GDA0/IO81NDB2V0	W4	IO98NDB4V0	
T11	VCC	U21	GDB0/IO80NDB2V0	W5	GEC1/IO90PDB4V0	
T12	GND	U22	VCCIB2	W6	GEC0/IO90NDB4V0	
T13	VCC	U23	IO75NDB2V0	W7	GND	
T14	GND	U24	IO75PDB2V0	W8	VCCNVM	
T15	VCC	U25	NC	W9	VCCIB4	
T16	GND	U26	NC	W10	VCC15A	
T17	VCCIB2	V1	NC	W11	GNDA	
T18	IO83NDB2V0	V2	VCCIB4	W12	AC4	
T19	IO78NDB2V0	V3	IO100PPB4V0	W13	VCC33A	
T20	GDA1/IO81PDB2V0	V4	GND	W14	GNDA	
T21	GDB1/IO80PDB2V0	V5	IO95PDB4V0	W15	AG5	
T22	IO73NDB2V0	V6	IO95NDB4V0	W16	GNDA	
T23	IO73PDB2V0	V7	VCCIB4	W17	PUB	
T24	IO71NDB2V0	V8	IO92NDB4V0	W18	VCCIB2	
T25	NC	V9	GNDNVM	W19	TDI	
T26	GND	V10	GNDA	W20	GND	
U1	NC	V11	NC	W21	IO84NDB2V0	
U2	NC	V12	AV4	W22	GDC2/IO84PDB2V0	
U3	IO102PDB4V0	V13	NC	W23	IO77NPB2V0	
U4	IO102NDB4V0	V14	AV5	W24	GDC0/IO79NDB2V0	

Revision	Changes	Page		
Revision 3 (continued)	The "RC Oscillator" section was revised to correct a sentence that did not differentiate accuracy for commercial and industrial temperature ranges, which is given in Table 2-9 • Electrical Characteristics of RC Oscillator (SAR 33722).			
	Figure 2-57 • FIFO Read and Figure 2-58 • FIFO Write are new (SAR 34840).			
	The first paragraph of the "Offset" section was removed; it was intended to be replaced by the paragraph following it (SAR 22647).			
	IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions (SAR 39813).	2-164		
	The drive strength, IOL, and IOH for 3.3 V GTL and 2.5 V GTL were changed from 25 mA to 20 mA in the following tables (SAR 37373):			
	Table 2-86 Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions,	2-164		
	Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings	2-167		
	Table 2-96 • I/O Output Buffer Maximum Resistances 1	2-169		
	Table 2-138 • Minimum and Maximum DC Input and Output Levels	2-199		
	Table 2-141 • Minimum and Maximum DC Input and Output Levels	2-200		
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34800): "It uses a 5 V–tolerant input buffer and push-pull output buffer."			
	Corrected the inadvertent error in maximum values for LVPECL VIH and VIL and revised them to "3.6" in Table 2-171 • Minimum and Maximum DC Input and Output Levels, making these consistent with Table 3-1 • Absolute Maximum Ratings, and Table 3-4 • Overshoot and Undershoot Limits 1 (SAR 37687).	2-211		
	The maximum frequency for global clock parameter was removed from Table 2-5 • AFS1500 Global Resource Timing through Table 2-8 • AFS090 Global Resource Timing because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36955).	2-16 to 2-17		
Revision 2 (March 2012)	The phrase "without debug" was removed from the "Soft ARM Cortex-M1 Fusion Devices (M1)" section (SAR 21390).	I		
	The "In-System Programming (ISP) and Security" section, "Security" section, "Flash Advantages" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34679).	l, 1-2, 2-228		
	The Y security option and Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34721).	III		
	The "Specifying I/O States During Programming" section is new (SAR 34693).	1-9		
	The following information was added before Figure 2-17 • XTLOSC Macro:	2-20		
	In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating (SAR 24119).			
	Table 2-12 • Fusion CCC/PLL Specification was updated. A note was added indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34814).	2-28		



Datasheet Information

Revision	Changes	Page
Advance v1.0 (continued)	This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to V_{CC33A} .	3-8
Advance v0.9 (October 2007)	In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126	II
	In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pin: B25	3-2
	In the "180-Pin QFN" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS090: B29 AFS250: B29	3-4
	In the "208-Pin PQFP" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS090: 102 AFS250: 102	3-8
	In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14	3-12
Advance v0.9 (continued)	In the "484-Pin FBGA" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS600: AB18 AFS1500: AB18	3-20
	In the "676-Pin FBGA" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS1500: AD20	3-28
Advance v0.8 (June 2007)	Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC.	2-20, 2-21
	Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added.	2-25
	The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator.	2-22
	Table 2-11 \cdot Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of I _{DYNXTAL} for 0.032–0.2 MHz to 0.19.	2-24
	The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR.	2-41
	The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR.	2-41