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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/u1afs250-fgg256">https://www.e-xfl.com/product-detail/microchip-technology/u1afs250-fgg256</a>

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

## Core Architecture

### VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

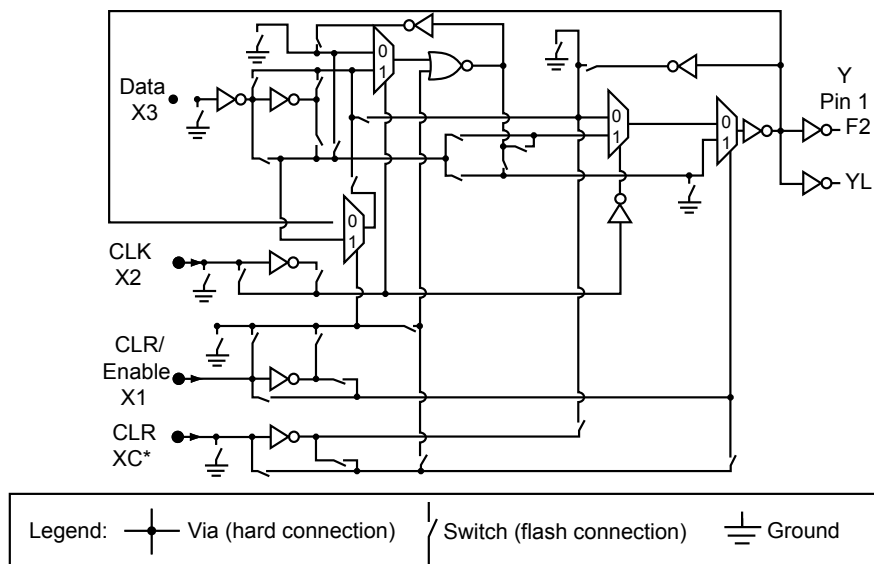
As illustrated in [Figure 2-2](#), there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources ([Figure 2-2](#)).



*Note:* \*This input can only be connected to the global clock distribution network.

**Figure 2-2 • Fusion Core VersaTile**

## CCC and PLL Characteristics

### Timing Characteristics

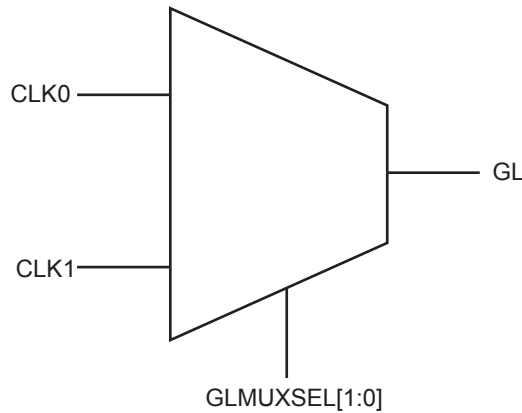
**Table 2-12 • Fusion CCC/PLL Specification**

Parameter	Min.	Typ.	Max.	Unit
Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$	0.75		350	MHz
Delay Increments in Programmable Delay Blocks <sup>1, 2</sup>		160 <sup>3</sup>		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	1.00%		1.00%	
24 MHz to 100 MHz	1.50%		1.50%	
100 MHz to 250 MHz	2.25%		2.25%	
250 MHz to 350 MHz	3.50%		3.50%	
Acquisition Time	LockControl = 0		300	μs
	LockControl = 1		6.0	ms
Tracking Jitter <sup>4</sup>	LockControl = 0		1.6	ns
	LockControl = 1		0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 <sup>1, 2</sup>	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 <sup>1, 2</sup>	0.025		5.56	ns
Delay Range in Block: Fixed Delay <sup>1, 2</sup>		2.2		ns

**Notes:**

1. This delay is a function of voltage and temperature. See [Table 3-7 on page 3-9](#) for deratings.
2.  $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 1.5\text{ V}$
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
4. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.

The NGMUX macro is simplified to show the two clock options that have been selected by the GLMUXCFG[1:0] bits. [Figure 2-25](#) illustrates the NGMUX macro. During design, the two clock sources are connected to CLK0 and CLK1 and are controlled by GLMUXSEL[1:0] to determine which signal is to be passed through the MUX.

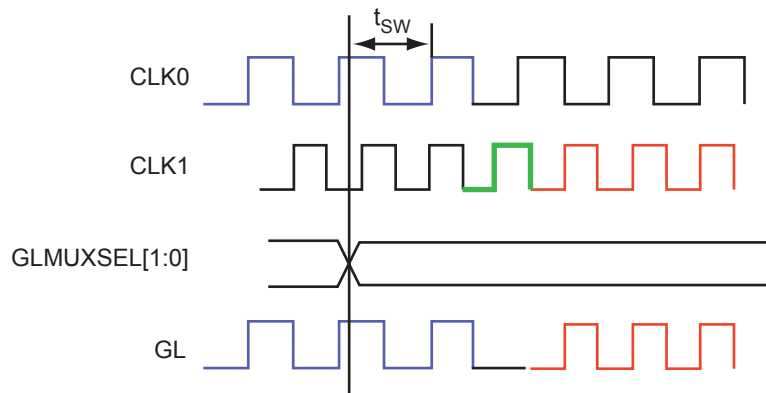


**Figure 2-25 • NGMUX Macro**

The sequence of switching between two clock sources (from CLK0 to CLK1) is as follows ([Figure 2-26](#)):

- GLMUXSEL[1:0] transitions to initiate a switch.
- GL drives one last complete CLK0 positive pulse (i.e., one rising edge followed by one falling edge).
- From that point, GL stays Low until the second rising edge of CLK1 occurs.
- At the second CLK1 rising edge, GL will begin to continuously deliver the CLK1 signal.
- Minimum  $t_{sw} = 0.05$  ns at 25°C (typical conditions)

For examples of NGMUX operation, refer to the [Fusion FPGA Fabric User Guide](#).



**Figure 2-26 • NGMUX Waveform**

Data operations are performed in widths of 1 to 4 bytes. A write to a location in a page that is not already in the Page Buffer will cause the page to be read from the FB Array and stored in the Page Buffer. The block that was addressed during the write will be put into the Block Buffer, and the data written by WD will overwrite the data in the Block Buffer. After the data is written to the Block Buffer, the Block Buffer is then written to the Page Buffer to keep both buffers in sync. Subsequent writes to the same block will overwrite the Block Buffer and the Page Buffer. A write to another block in the page will cause the addressed block to be loaded from the Page Buffer, and the write will be performed as described previously.

The data width can be selected dynamically via the DATAWIDTH input bus. The truth table for the data width settings is detailed in [Table 2-21](#). The minimum resolvable address is one 8-bit byte. For data widths greater than 8 bits, the corresponding address bits are ignored—when DATAWIDTH = 0 (2 bytes), ADDR[0] is ignored, and when DATAWIDTH = '10' or '11' (4 bytes), ADDR[1:0] are ignored. Data pins are LSB-oriented and unused WD data pins must be grounded.

**Table 2-21 • Data Width Settings**

DATAWIDTH[1:0]	Data Width
00	1 byte [7:0]
01	2 byte [15:0]
10, 11	4 bytes [31:0]

## Flash Memory Block Protection

### Page Loss Protection

When the PAGELOSSPROTECT pin is set to logic 1, it prevents writes to any page other than the current page in the Page Buffer until the page is either discarded or programmed.

A write to another page while the current page is Page Loss Protected will return a STATUS of '11'.

### Overwrite Protection

Any page that is Overwrite Protected will result in the STATUS being set to '01' when an attempt is made to either write, program, or erase it. To set the Overwrite Protection state for a page, set the OVERWRITEPROTECT pin when a Program operation is undertaken. To clear the Overwrite Protect state for a given page, an Unprotect Page operation must be performed on the page, and then the page must be programmed with the OVERWRITEPROTECT pin cleared to save the new page.

### LOCKREQUEST

The LOCKREQUEST signal is used to give the user interface control over simultaneous access of the FB from both the User and JTAG interfaces. When LOCKREQUEST is asserted, the JTAG interface will hold off any access attempts until LOCKREQUEST is deasserted.

## Flash Memory Block Operations

### FB Operation Priority

The FB provides for priority of operations when multiple actions are requested simultaneously. [Table 2-22](#) shows the priority order (priority 0 is the highest).

**Table 2-22 • FB Operation Priority**

Operation	Priority
System Initialization	0
FB Reset	1
Read	2
Write	3
Erase Page	4
Program	5
Unprotect Page	6
Discard Page	7

## SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

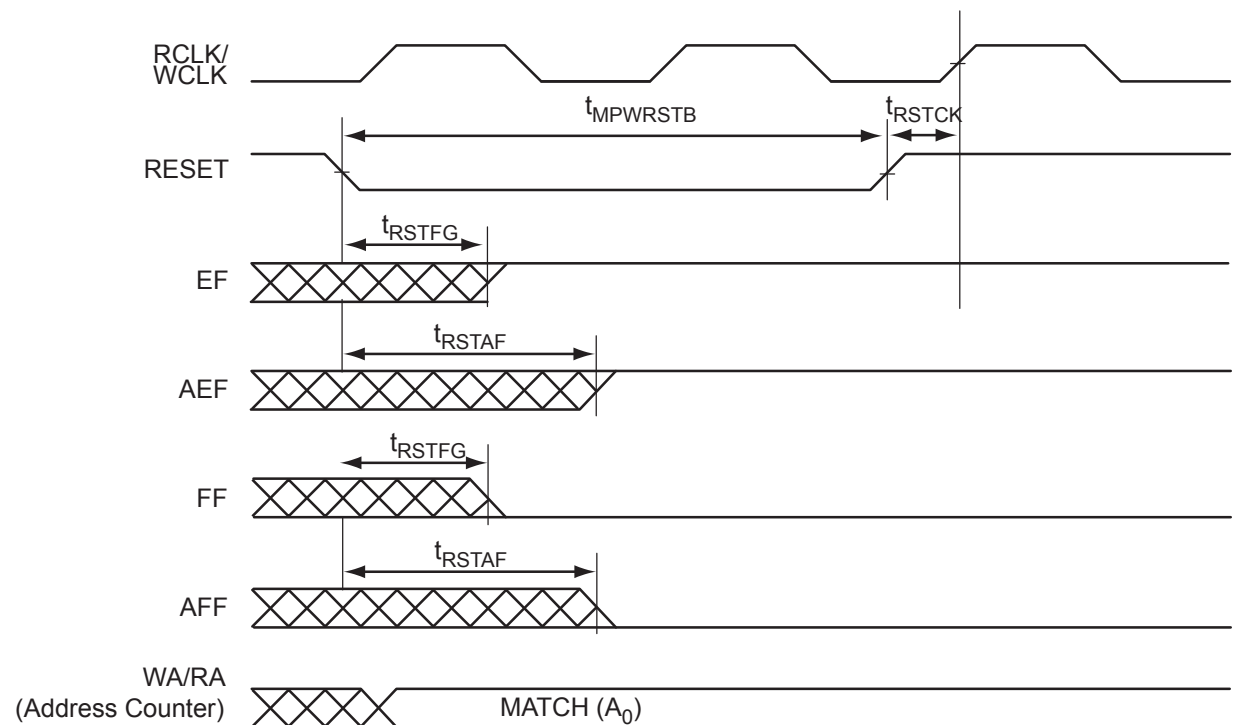
During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to [Figure 2-47](#) for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

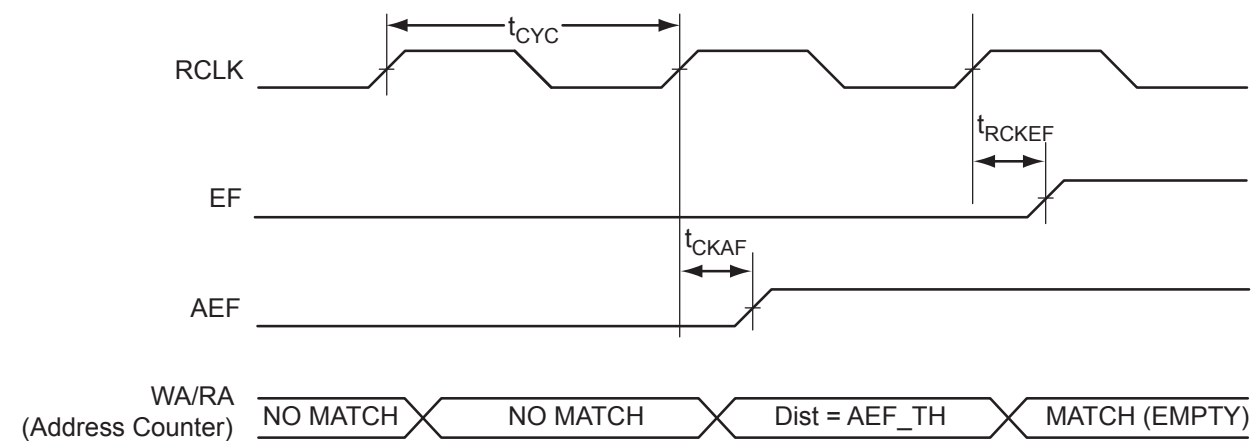
Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in [Table 2-27 on page 2-58](#).

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.



**Figure 2-59 • FIFO Reset**



**Figure 2-60 • FIFO EMPTY Flag and AEMPTY Flag Assertion**

## Analog System Characteristics

**Table 2-49 • Analog Channel Specifications**  
Commercial Temperature Range Conditions,  $T_J = 85^\circ\text{C}$  (unless noted otherwise),  
Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
<b>Voltage Monitor Using Analog Pads AV, AC and AT (using prescaler)</b>						
	Input Voltage (Prescaler)	Refer to <a href="#">Table 3-2 on page 3-3</a>				
VINAP	Uncalibrated Gain and Offset Errors	Refer to <a href="#">Table 2-51 on page 2-122</a>				
	Calibrated Gain and Offset Errors	Refer to <a href="#">Table 2-52 on page 2-123</a>				
	Bandwidth <sup>1</sup>				100	KHz
	Input Resistance	Refer to <a href="#">Table 3-3 on page 3-4</a>				
	Scaling Factor	Prescaler modes ( <a href="#">Table 2-57 on page 2-130</a> )				
	Sample Time		10			$\mu\text{s}$
<b>Current Monitor Using Analog Pads AV and AC</b>						
VRSM <sup>1</sup>	Maximum Differential Input Voltage				VAREF / 10	mV
	Resolution	Refer to <a href="#">"Current Monitor" section</a>				
	Common Mode Range				- 10.5 to +12	V
CMRR	Common Mode Rejection Ratio	DC – 1 KHz		60		dB
		1 KHz - 10 KHz		50		dB
		> 10 KHz		30		dB
$t_{\text{CMSHI}}$	Strobe High time		ADC conv. time		200	$\mu\text{s}$
$t_{\text{CMSHI}}$	Strobe Low time		5			$\mu\text{s}$
$t_{\text{CMSHI}}$	Settling time		0.02			$\mu\text{s}$
	Accuracy	Input differential voltage > 50 mV			-2 – (0.05 x VRSM) to +2 + (0.05 x VRSM)	mV

### Notes:

1. VRSM is the maximum voltage drop across the current sense resistor.
2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.
3. VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.
4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
5. The temperature offset is a fixed positive value.
6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the [Fusion FPGA Fabric User Guide](#).

**Table 2-49 • Analog Channel Specifications (continued)**  
**Commercial Temperature Range Conditions,  $T_J = 85^\circ\text{C}$  (unless noted otherwise),**  
**Typical:  $V_{CC33A} = 3.3\text{ V}$ ,  $V_{CC} = 1.5\text{ V}$**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
<b>Temperature Monitor Using Analog Pad AT</b>						
External Temperature Monitor (external diode 2N3904, $T_J = 25^\circ\text{C}$ ) <sup>4</sup>	Resolution	8-bit ADC		4		$^\circ\text{C}$
		10-bit ADC		1		$^\circ\text{C}$
		12-bit ADC		0.25		$^\circ\text{C}$
	Systematic Offset <sup>5</sup>	AFS090, AFS250, AFS600, AFS1500, uncalibrated <sup>7</sup>		5		$^\circ\text{C}$
		AFS090, AFS250, AFS600, AFS1500, calibrated <sup>7</sup>		$\pm 5$		$^\circ\text{C}$
	Accuracy			$\pm 3$	$\pm 5$	$^\circ\text{C}$
	External Sensor Source Current	High level, TMSTBx = 0		10		$\mu\text{A}$
		Low level, TMSTBx = 1		100		$\mu\text{A}$
	Max Capacitance on AT pad				1.3	nF
Internal Temperature Monitor	Resolution	8-bit ADC	4			$^\circ\text{C}$
		10-bit ADC	1			$^\circ\text{C}$
		12-bit ADC	0.25			$^\circ\text{C}$
	Systematic Offset <sup>5</sup>	AFS090 <sup>7</sup>		5		$^\circ\text{C}$
		AFS250, AFS600, AFS1500 <sup>7</sup>		11		$^\circ\text{C}$
	Accuracy			$\pm 3$	$\pm 5$	$^\circ\text{C}$
$t_{\text{TMSHI}}$	Strobe High time		10		105	$\mu\text{s}$
$t_{\text{TMSLO}}$	Strobe Low time		5			$\mu\text{s}$
$t_{\text{TMSSET}}$	Settling time		5			$\mu\text{s}$

**Notes:**

1.  $V_{\text{RSM}}$  is the maximum voltage drop across the current sense resistor.
2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as  $V_{\text{IND}}$  does not exceed these limits.
3.  $V_{\text{IND}}$  is limited to  $V_{\text{CC33A}} + 0.2$  to allow reaching 10 MHz input frequency.
4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
5. The temperature offset is a fixed positive value.
6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the [Fusion FPGA Fabric User Guide](#).

**Table 2-51 • Uncalibrated Analog Channel Accuracy\***  
**Worst-Case Industrial Conditions, T<sub>J</sub> = 85°C**

		Total Channel Error (LSB)			Channel Input Offset Error (LSB)			Channel Input Offset Error (mV)			Channel Gain Error (%FSR)		
Analog Pad	Prescaler Range (V)	Neg. Max.	Med.	Pos. Max.	Neg. Max	Med.	Pos. Max.	Neg. Max.	Med.	Pos. Max.	Min.	Typ.	Max.
<b>Positive Range</b>		<b>ADC in 10-Bit Mode</b>											
AV, AC	16	-22	-2	12	-11	-2	14	-169	-32	224	3	0	-3
	8	-40	-5	17	-11	-5	21	-87	-40	166	2	0	-4
	4	-45	-9	24	-16	-11	36	-63	-43	144	2	0	-4
	2	-70	-19	33	-33	-20	66	-66	-39	131	2	0	-4
	1	-25	-7	5	-11	-3	26	-11	-3	26	3	-1	-3
	0.5	-41	-12	8	-12	-7	38	-6	-4	19	3	-1	-3
	0.25	-53	-14	19	-20	-14	40	-5	-3	10	5	0	-4
	0.125	-89	-29	24	-40	-28	88	-5	-4	11	7	0	-5
AT	16	-3	9	15	-4	0	4	-64	5	64	1	0	-1
	4	-10	2	15	-11	-2	11	-44	-8	44	1	0	-1
<b>Negative Range</b>		<b>ADC in 10-Bit Mode</b>											
AV, AC	16	-35	-10	9	-24	-6	9	-383	-96	148	5	-1	-6
	8	-65	-19	12	-34	-12	9	-268	-99	75	5	-1	-5
	4	-86	-28	21	-64	-24	19	-254	-96	76	5	-1	-6
	2	-136	-53	37	-115	-42	39	-230	-83	78	6	-2	-7
	1	-98	-35	8	-39	-8	15	-39	-8	15	10	-3	-10
	0.5	-121	-46	7	-54	-14	18	-27	-7	9	10	-4	-11
	0.25	-149	-49	19	-72	-16	40	-18	-4	10	14	-4	-12
	0.125	-188	-67	38	-112	-27	56	-14	-3	7	16	-5	-14

*Note:* \*Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.

**Table 2-68 • I/O Bank Support by Device**

I/O Bank	AFS090	AFS250	AFS600	AFS1500
Standard I/O	N	N	–	–
Advanced I/O	E, W	E, W	E, W	E, W
Pro I/O	–	–	N	N
Analog Quad	S	S	S	S

*Note:* E = East side of the device  
 W = West side of the device  
 N = North side of the device  
 S = South side of the device

**Table 2-69 • Fusion VCCI Voltages and Compatible Standards**

VCCI (typical)	Compatible Standards
3.3 V	LVTTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II),* GTL+ 3.3, GTL 3.3,* LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II),* GTL+ 2.5,* GTL 2.5,* LVDS, BLVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I),* HSTL (Class II)*

*Note:* \*I/O standard supported by Pro I/O banks.

**Table 2-70 • Fusion VREF Voltages and Compatible Standards\***

VREF (typical)	Compatible Standards
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

*Note:* \*I/O standards supported by Pro I/O banks.

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 k $\Omega$  (or lower) output drive resistance at hot insertion, and 1 k $\Omega$  (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

1. Grounds
2. Powers, I/Os, other pins

## Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks and standard I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If Standard I/O banks are used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the standard I/O buffers do not have built-in I/O clamp diodes.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull down resistor and driven in the opposite direction. A small static current is induced on each IO pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Please refer to [Table 2-95 on page 2-169](#), [Table 2-96 on page 2-169](#), and [Table 2-97 on page 2-171](#) for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTTL 3.3 V, pull-up resistor is ~45 k $\Omega$  and the resulting current is equal to  $3.3 \text{ V} / 45 \text{ k}\Omega = 73 \text{ }\mu\text{A}$  for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven low
- Input buffers with pull-down, driven high
- Bidirectional buffers with pull-up, driven low
- Bidirectional buffers with pull-down, driven high
- Output buffers with pull-up, driven low
- Output buffers with pull-down, driven high
- Tristate buffers with pull-up, driven low
- Tristate buffers with pull-down, driven high

## 5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTTL or 3.3 V LVCMOS mode, Fusion I/Os can directly drive signals into 5 V TTL receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both 3.3 V LVTTTL and 3.3 V LVCMOS modes exceed the VIL = 0.8 V and VIH = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

## Simultaneously Switching Outputs and PCB Layout

- Simultaneously switching outputs (SSOs) can produce signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and VCCI dip noise. These two noise types are caused by rapidly changing currents through GND and VCCI package pin inductances during switching activities:
- Ground bounce noise voltage =  $L(\text{GND}) * di/dt$
- VCCI dip noise voltage =  $L(\text{VCCI}) * di/dt$

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTTL/LVCMOS inputs, LVTTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to be considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

## I/O Register Specifications

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

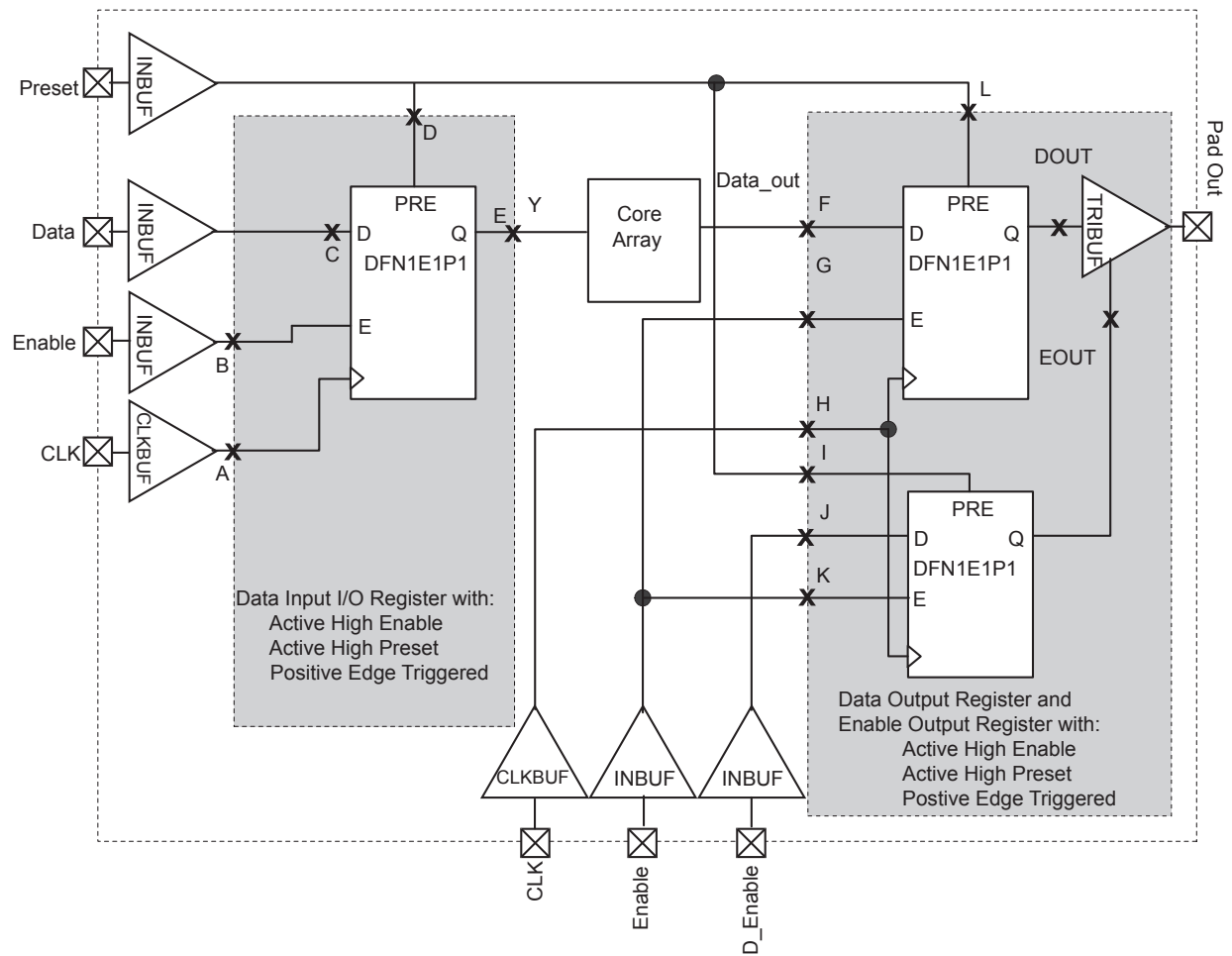


Figure 2-137 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

**Table 2-175 • Parameter Definitions and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
$t_{OCLKQ}$	Clock-to-Q of the Output Data Register	HH, DOUT
$t_{OSUD}$	Data Setup Time for the Output Data Register	FF, HH
$t_{OHD}$	Data Hold Time for the Output Data Register	FF, HH
$t_{OSUE}$	Enable Setup Time for the Output Data Register	GG, HH
$t_{OHE}$	Enable Hold Time for the Output Data Register	GG, HH
$t_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	HH, EOUT
$t_{OESUD}$	Data Setup Time for the Output Enable Register	JJ, HH
$t_{OEHD}$	Data Hold Time for the Output Enable Register	JJ, HH
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	KK, HH
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
$t_{ICLKQ}$	Clock-to-Q of the Input Data Register	AA, EE
$t_{ISUD}$	Data Setup Time for the Input Data Register	CC, AA
$t_{IHD}$	Data Hold Time for the Input Data Register	CC, AA
$t_{ISUE}$	Enable Setup Time for the Input Data Register	BB, AA
$t_{IHE}$	Enable Hold Time for the Input Data Register	BB, AA
$t_{ICLR2Q}$	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note:* \*See Figure 2-138 on page 2-214 for more information.

## 3 – DC and Power Characteristics

### General Specifications

#### Operating Conditions

Stresses beyond those listed in [Table 3-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in [Table 3-2](#) on [page 3-3](#).

**Table 3-1 • Absolute Maximum Ratings**

Symbol	Parameter	Commercial	Industrial	Units
VCC	DC core supply voltage	–0.3 to 1.65	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	–0.3 to 3.75	V
VI	I/O input voltage <sup>1</sup>	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)		V
VCC33A	+3.3 V power supply	–0.3 to 3.75 <sup>2</sup>	–0.3 to 3.75 <sup>2</sup>	V
VCC33PMP	+3.3 V power supply	–0.3 to 3.75 <sup>2</sup>	–0.3 to 3.75 <sup>2</sup>	V
VAREF	Voltage reference for ADC	–0.3 to 3.75	–0.3 to 3.75	V
VCC15A	Digital power supply for the analog system	–0.3 to 1.65	–0.3 to 1.65	V
VCCNVM	Embedded flash power supply	–0.3 to 1.65	–0.3 to 1.65	V
VCCOSC	Oscillator power supply	–0.3 to 3.75	–0.3 to 3.75	V

**Notes:**

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 3-4](#) on [page 3-4](#).
2. Analog data not valid beyond 3.65 V.
3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
4. For flash programming and retention maximum limits, refer to [Table 3-5](#) on [page 3-5](#). For recommended operating limits refer to [Table 3-2](#) on [page 3-3](#).

**Table 3-2 • Recommended Operating Conditions<sup>1</sup>**

Symbol	Parameter <sup>2</sup>		Commercial	Industrial	Units
T <sub>J</sub>	Junction temperature		0 to +85	−40 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming mode <sup>3</sup>	3.15 to 3.45	3.15 to 3.45	V
		Operation <sup>4</sup>	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VCC33PMP	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VAREF	Voltage reference for ADC		2.527 to 2.593	2.527 to 2.593	V
VCC15A <sup>5</sup>	Digital power supply for the analog system		1.425 to 1.575	1.425 to 1.575	V
VCCNVM	Embedded flash power supply		1.425 to 1.575	1.425 to 1.575	V
VCCOSC	Oscillator power supply		2.97 to 3.63	2.97 to 3.63	V
AV, AC <sup>6</sup>	Unpowered, ADC reset asserted or unconfigured		−10.5 to 12.0	−10.5 to 11.6	V
	Analog input (+16 V to +2 V prescaler range)		−0.3 to 12.0	−0.3 to 11.6	V
	Analog input (+1 V to + 0.125 V prescaler range)		−0.3 to 3.6	−0.3 to 3.6	V
	Analog input (−16 V to −2 V prescaler range)		−10.5 to 0.3	−10.5 to 0.3	V
	Analog input (−1 V to −0.125 V prescaler range)		−3.6 to 0.3	−3.6 to 0.3	V
	Analog input (direct input to ADC)		−0.3 to 3.6	−0.3 to 3.6	V
	Digital input		−0.3 to 12.0	−0.3 to 11.6	V
AG <sup>6</sup>	Unpowered, ADC reset asserted or unconfigured		−10.5 to 12.0	−10.5 to 11.6	V
	Low Current Mode (1 μA, 3 μA, 10 μA, 30 μA)		−0.3 to 12.0	−0.3 to 11.6	V
	Low Current Mode (−1 μA, −3 μA, −10 μA, −30 μA)		−10.5 to 0.3	−10.5 to 0.3	V
	High Current Mode <sup>7</sup>		−10.5 to 12.0	−10.5 to 11.6	V
AT <sup>6</sup>	Unpowered, ADC reset asserted or unconfigured		−0.3 to 15.5	−0.3 to 14.5	V
	Analog input (+16 V, +4 V prescaler range)		−0.3 to 15.5	−0.3 to 14.5	V
	Analog input (direct input to ADC)		−0.3 to 3.6	−0.3 to 3.6	V
	Digital input		−0.3 to 15.5	−0.3 to 14.5	V

**Notes:**

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-85 on page 2-157](#).
2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
3. The programming temperature range supported is T<sub>ambient</sub> = 0°C to 85°C.
4. VPUMP can be left floating during normal operation (not programming mode).
5. Violating the V<sub>CC15A</sub> recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.
6. The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.
7. The AG pad should also conform to the limits as specified in [Table 2-48 on page 2-114](#).

**Table 3-5 • FPGA Programming, Storage, and Operating Limits**

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. $T_J = 0^{\circ}\text{C}$ Max. $T_J = 85^{\circ}\text{C}$	FPGA/FlashROM	500	20 years
		Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years
Industrial	Min. $T_J = -40^{\circ}\text{C}$ Max. $T_J = 100^{\circ}\text{C}$	FPGA/FlashROM	500	20 years
		Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every Fusion device. These circuits ensure easy transition from the powered off state to the powered up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 3-1 on page 3-6](#).

There are five regions to consider during power-up.

Fusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 3-1](#)).
2. VCCI > VCC – 0.75 V (typical).
3. Chip is in the operating mode.

### VCCI Trip Point:

Ramping up:  $0.6\text{ V} < \text{trip\_point\_up} < 1.2\text{ V}$

Ramping down:  $0.5\text{ V} < \text{trip\_point\_down} < 1.1\text{ V}$

### VCC Trip Point:

Ramping up:  $0.6\text{ V} < \text{trip\_point\_up} < 1.1\text{ V}$

Ramping down:  $0.5\text{ V} < \text{trip\_point\_down} < 1\text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

## Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

## PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see [Figure 3-1 on page 3-6](#) for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ( $0.75\text{ V} \pm 0.25\text{ V}$ ), the PLL output lock signal goes low and/or the output clock is lost.

### Theta-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

where

$\theta_{JA} = 19.00^\circ\text{C/W}$  (taken from Table 3-6 on page 3-7).

$T_A = 75.00^\circ\text{C}$

$$\text{Maximum Power Allowed} = \frac{100.00^\circ\text{C} - 75.00^\circ\text{C}}{19.00^\circ\text{C/W}} = 1.3 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

### Theta-JB

Junction-to-board thermal resistance ( $\theta_{JB}$ ) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

### Theta-JC

Junction-to-case thermal resistance ( $\theta_{JC}$ ) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

### Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent  $T_a$  and  $T_j$  are given as follows:

$T_J = 100.00^\circ\text{C}$

$T_A = 70.00^\circ\text{C}$

From the datasheet:

$\theta_{JA} = 17.00^\circ\text{C/W}$

$\theta_{JC} = 8.28^\circ\text{C/W}$

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6

### RAM Dynamic Contribution— $P_{MEMORY}$

#### Operating Mode

$$P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE-CLOCK})$$

$N_{BLOCKS}$  is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$  is the memory read clock frequency.

$\beta_2$  is the RAM enable rate for read operations—guidelines are provided in [Table 3-17 on page 3-27](#).

$\beta_3$  the RAM enable rate for write operations—guidelines are provided in [Table 3-17 on page 3-27](#).

$F_{WRITE-CLOCK}$  is the memory write clock frequency.

#### Standby Mode and Sleep Mode

$$P_{MEMORY} = 0 \text{ W}$$

### PLL/CCC Dynamic Contribution— $P_{PLL}$

#### Operating Mode

$$P_{PLL} = PAC13 * F_{CLKOUT}$$

$F_{CLKIN}$  is the input clock frequency.

$F_{CLKOUT}$  is the output clock frequency.<sup>1</sup>

#### Standby Mode and Sleep Mode

$$P_{PLL} = 0 \text{ W}$$

### Nonvolatile Memory Dynamic Contribution— $P_{NVM}$

#### Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

$$P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * PAC15 * F_{READ-NVM} \text{ when } F_{READ-NVM} \leq 33 \text{ MHz,}$$

$$P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * (PAC16 + PAC17 * F_{READ-NVM} \text{ when } F_{READ-NVM} > 33 \text{ MHz}$$

$N_{NVM-BLOCKS}$  is the number of NVM blocks used in the design (2 in AFS600).

$\beta_4$  is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state).

$F_{READ-NVM}$  is the NVM read clock frequency.

#### Standby Mode and Sleep Mode

$$P_{NVM} = 0 \text{ W}$$

### Crystal Oscillator Dynamic Contribution— $P_{XTL-OSC}$

#### Operating Mode

$$P_{XTL-OSC} = PAC18$$

#### Standby Mode

$$P_{XTL-OSC} = PAC18$$

#### Sleep Mode

$$P_{XTL-OSC} = 0 \text{ W}$$

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ( $P_{AC14} * F_{CLKOUT}$  product) to the total PLL contribution.

Revision	Changes	Page
Advance v0.6 (continued)	The "Analog-to-Digital Converter Block" section was updated with the following statement: "All results are MSB justified in the ADC."	2-99
	The information about the ADCSTART signal was updated in the "ADC Description" section.	2-102
	Table 2-46 · Analog Channel Specifications was updated.	2-118
	Table 2-47 · ADC Characteristics in Direct Input Mode was updated.	2-121
	Table 2-51 · ACM Address Decode Table for Analog Quad was updated.	2-127
	In Table 2-53 · Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated.	2-130
	The "Introduction" section was updated to include information about digital inputs, outputs, and buffers.	2-133
	In Table 2-69 · Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features: Single-ended receiver Voltage-referenced differential receiver LVDS/LVPECL differential receiver features	2-137
	The "User I/O Naming Convention" section was updated to include "V" and "Z" descriptions	2-159
	The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and VCCI pins within a given I/O bank.	2-185
	The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090.	3-8