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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

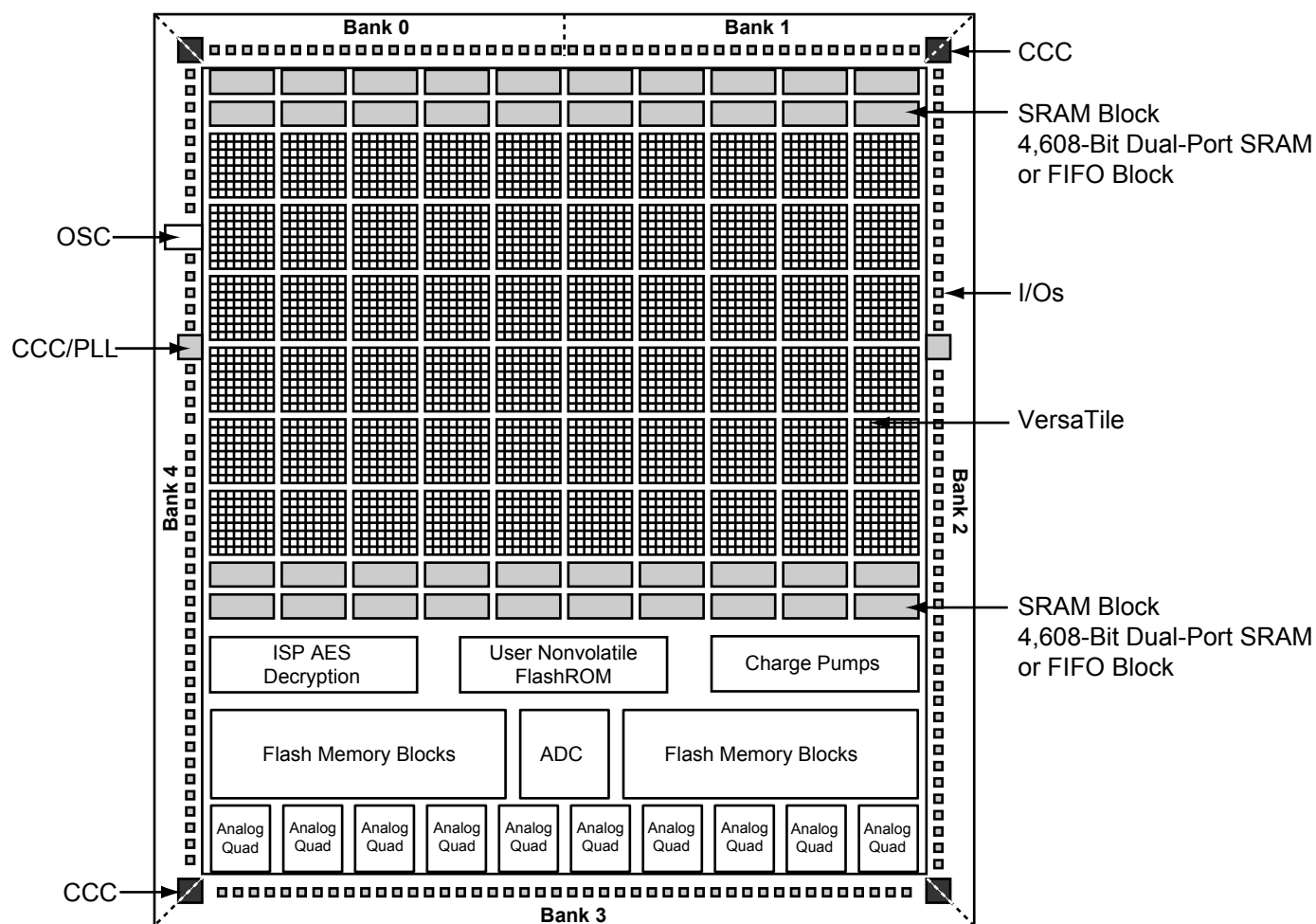
### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/u1afs250-fgg256i">https://www.e-xfl.com/product-detail/microchip-technology/u1afs250-fgg256i</a>

## Fusion Device Architecture Overview



**Figure 1 • Fusion Device Architecture Overview (AFS600)**

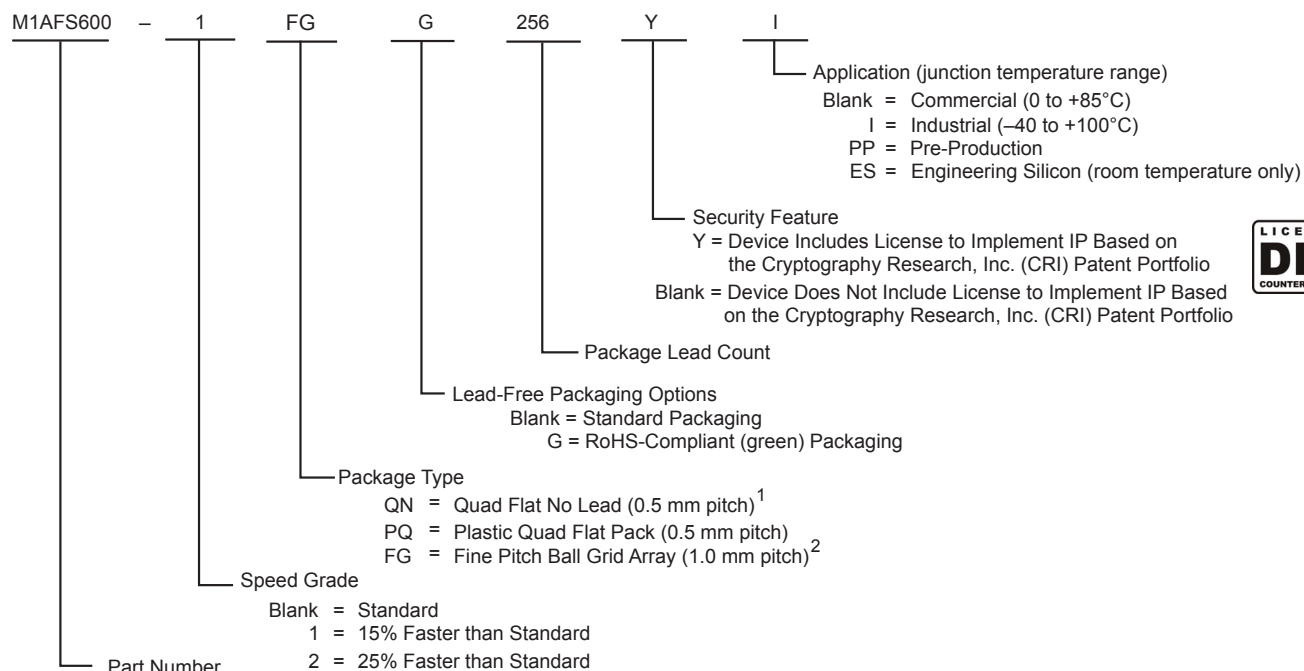
### Package I/Os: Single-/Double-Ended (Analog)

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
ARM Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500
Pigeon Point Devices			P1AFS600 <sup>1</sup>	P1AFS1500 <sup>1</sup>
MicroBlade Devices		U1AFS250 <sup>2</sup>	U1AFS600 <sup>2</sup>	U1AFS1500 <sup>2</sup>
QN108 <sup>3</sup>	37/9 (16)			
QN180 <sup>3</sup>	60/16 (20)	65/15 (24)		
PQ208 <sup>4</sup>		93/26 (24)	95/46 (40)	
FG256	75/22 (20)	114/37 (24)	119/58 (40)	119/58 (40)
FG484			172/86 (40)	223/109 (40)
FG676				252/126 (40)

**Notes:**

1. Pigeon Point devices are only offered in FG484 and FG256.
2. MicroBlade devices are only offered in FG256.
3. Package not available.
4. Fusion devices in the same package are pin compatible with the exception of the PQ208 package (AFS250 and AFS600).

## Product Ordering Codes



### Fusion Devices

AFS090 = 90,000 System Gates  
AFS250 = 250,000 System Gates  
AFS600 = 600,000 System Gates  
AFS1500 = 1,500,000 System Gates

### ARM-Enabled Fusion Devices

M1AFS250 = 250,000 System Gates  
M1AFS600 = 600,000 System Gates  
M1AFS1500 = 1,500,000 System Gates

### Pigeon Point Devices

P1AFS600 = 600,000 System Gates  
P1AFS1500 = 1,500,000 System Gates

### MicroBlade Devices

U1AFS250 = 250,000 System Gates  
U1AFS600 = 600,000 System Gates  
U1AFS1500 = 1,500,000 System Gates

### Notes:

- For Fusion devices, Quad Flat No Lead packages are only offered as RoHS compliant, QNG packages.
- MicroBlade and Pigeon Point devices only support FG packages.

## Fusion Device Status

Fusion	Status	Cortex-M1	Status	Pigeon Point	Status	MicroBlade	Status
AFS090	Production						
AFS250	Production	M1AFS250	Production			U1AFS250	Production
AFS600	Production	M1AFS600	Production	P1AFS600	Production	U1AFS600	Production
AFS1500	Production	M1AFS1500	Production	P1AFS1500	Production	U1AFS1500	Production

### Timing Characteristics

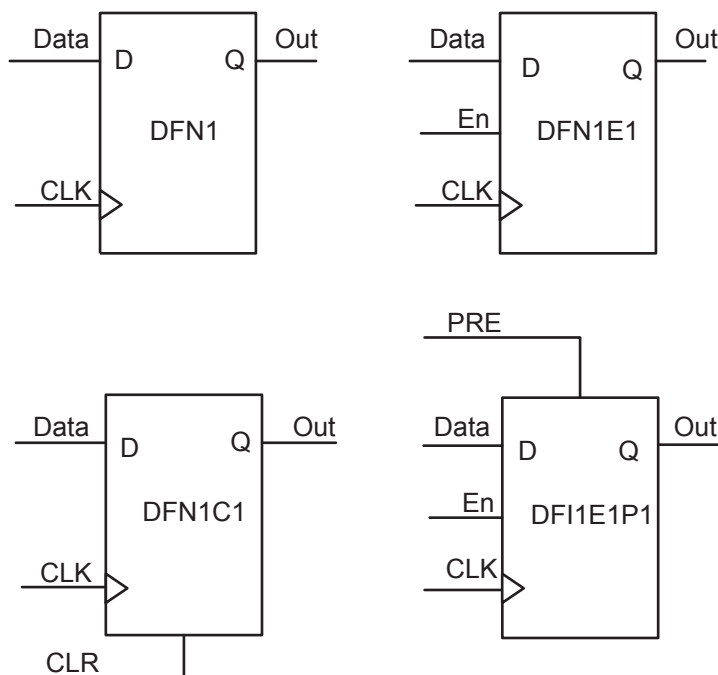
**Table 2-1 • Combinatorial Cell Propagation Delays**  
Commercial Temperature Range Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	Units
INV	$Y = !A$	$t_{PD}$	0.40	0.46	0.54	ns
AND2	$Y = A \cdot B$	$t_{PD}$	0.47	0.54	0.63	ns
NAND2	$Y = !(A \cdot B)$	$t_{PD}$	0.47	0.54	0.63	ns
OR2	$Y = A + B$	$t_{PD}$	0.49	0.55	0.65	ns
NOR2	$Y = !(A + B)$	$t_{PD}$	0.49	0.55	0.65	ns
XOR2	$Y = A \oplus B$	$t_{PD}$	0.74	0.84	0.99	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	$t_{PD}$	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	$t_{PD}$	0.87	1.00	1.17	ns
MUX2	$Y = A \text{ IS } + B \text{ S}$	$t_{PD}$	0.51	0.58	0.68	ns
AND3	$Y = A \cdot B \cdot C$	$t_{PD}$	0.56	0.64	0.75	ns

*Note:* For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

### Sample VersaTile Specifications—Sequential Module

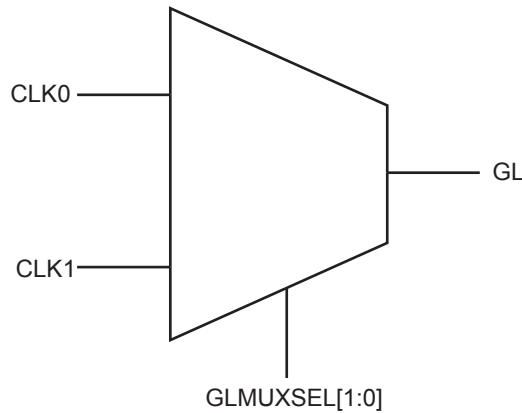
The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library ([Figure 2-5](#)). For more details, refer to the [IGLOO](#), [ProASIC3](#), [SmartFusion](#) and [Fusion Macro Library Guide](#).



**Figure 2-5 • Sample of Sequential Cells**



The NGMUX macro is simplified to show the two clock options that have been selected by the GLMUXCFG[1:0] bits. [Figure 2-25](#) illustrates the NGMUX macro. During design, the two clock sources are connected to CLK0 and CLK1 and are controlled by GLMUXSEL[1:0] to determine which signal is to be passed through the MUX.

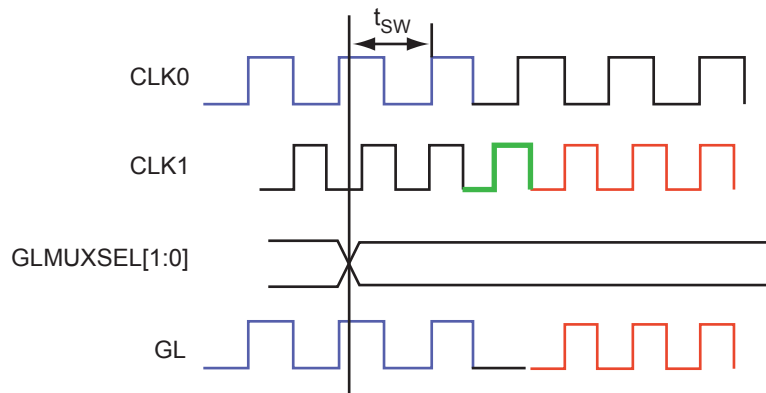


**Figure 2-25 • NGMUX Macro**

The sequence of switching between two clock sources (from CLK0 to CLK1) is as follows ([Figure 2-26](#)):

- GLMUXSEL[1:0] transitions to initiate a switch.
- GL drives one last complete CLK0 positive pulse (i.e., one rising edge followed by one falling edge).
- From that point, GL stays Low until the second rising edge of CLK1 occurs.
- At the second CLK1 rising edge, GL will begin to continuously deliver the CLK1 signal.
- Minimum  $t_{sw} = 0.05$  ns at 25°C (typical conditions)

For examples of NGMUX operation, refer to the [Fusion FPGA Fabric User Guide](#).

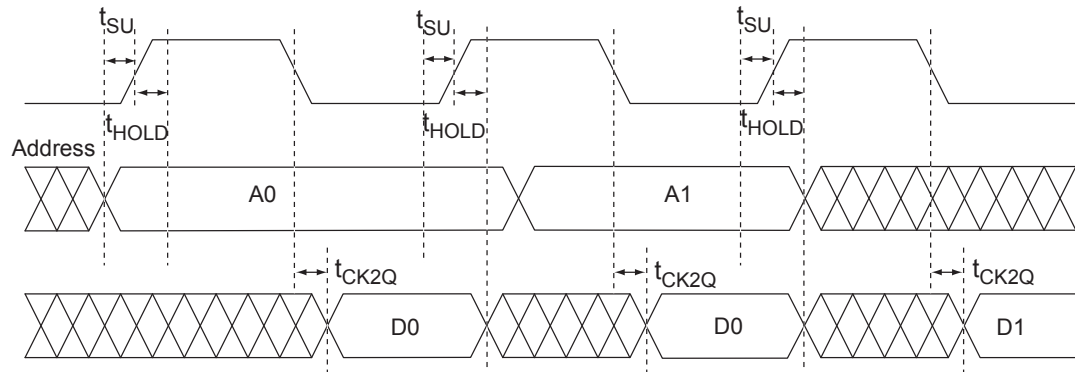


**Figure 2-26 • NGMUX Waveform**

		4 LSB of ADDR (READ)															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bank Number 3 MSB of ADDR (READ)	7																
	6																
	5																
	4																
	3																
	2																
	1																
	0																

**Figure 2-45 • FlashROM Architecture**

### FlashROM Characteristics



**Figure 2-46 • FlashROM Timing Diagram**

**Table 2-26 • FlashROM Access Time**

Commercial Temperature Range Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
$t_{SU}$	Address Setup Time	0.53	0.61	0.71	ns
$t_{HOLD}$	Address Hold Time	0.00	0.00	0.00	ns
$t_{CK2Q}$	Clock to Out	21.42	24.40	28.68	ns
$F_{MAX}$	Maximum Clock frequency	15.00	15.00	15.00	MHz

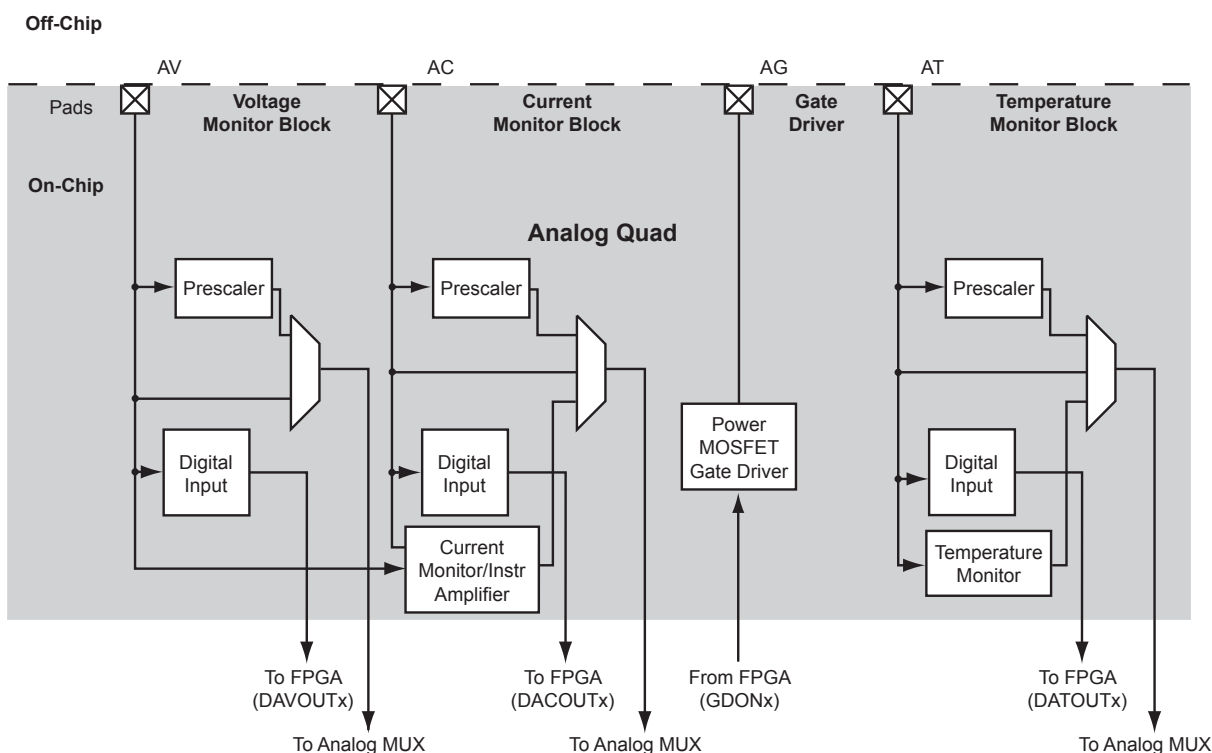
The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

The third part of the Analog Quad is called the Gate Driver Block, and its output pin is named AG. This section is used to drive an external FET. There are two modes available: a High Current Drive mode and a Current Source Control mode. Both negative and positive voltage polarities are available, and in the current source control mode, four different current levels are available.

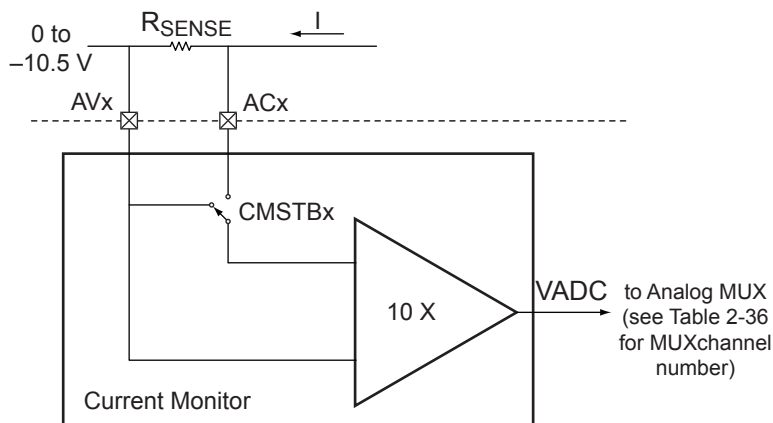
The fourth section of the Analog Quad is called the Temperature Monitor Block, and its input pin name is AT. This block is similar to the Voltage Monitor Block, except that it has an additional function: it can be used to monitor the temperature of an external diode-connected transistor. It has a modified prescaler and is limited to positive voltages only.

The Analog Quad can be configured during design time by Libero SoC; however, the ACM can be used to change the parameters of any of these I/Os during runtime. This type of change is referred to as a context switch. The Analog Quad is a modular structure that is replicated to generate the analog I/O resources. Each Fusion device supports between 5 and 10 Analog Quads.

The analog pads are numbered to clearly identify both the type of pad (voltage, current, gate driver, or temperature pad) and its corresponding Analog Quad (AV0, AC0, AG0, AT0, AV1, ..., AC9, AG9, and AT9). There are three types of input pads (AVx, ACx, and ATx) and one type of analog output pad (AGx). Since there can be up to 10 Analog Quads on a device, there can be a maximum of 30 analog input pads and 10 analog output pads.



**Figure 2-65 • Analog Quad**



**Figure 2-73 • Negative Current Monitor**

### Terminology

#### Accuracy

The accuracy of Fusion Current Monitor is  $\pm 2$  mV minimum plus 5% of the differential voltage at the input. The input accuracy can be translated to error at the ADC output by using EQ 4. The 10 V/V gain is the gain of the Current Monitor Circuit, as described in the "Current Monitor" section on page 2-86. For 8-bit mode,  $N = 8$ ,  $V_{AREF} = 2.56$  V, zero differential voltage between AV and AC, the Error ( $E_{ADC}$ ) is equal to 2 LSBs.

$$E_{ADC} = (2mV + 0.05|V_{AV} - V_{AC}|) \times (10V)/V \times \frac{2^N}{V_{AREF}}$$

EQ 4

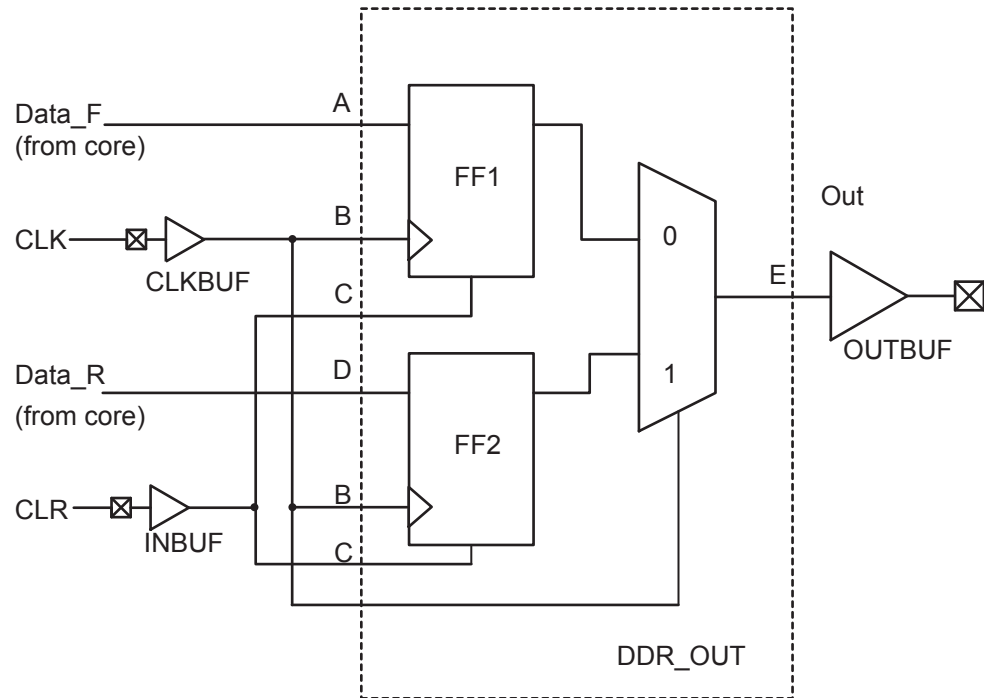
where

$N$  is the number of bits

$V_{AREF}$  is the Reference voltage

$V_{AV}$  is the voltage at AV pad

$V_{AC}$  is the voltage at AC pad



**Figure 2-102 • DDR Output Support in Fusion Devices**

## Electrostatic Discharge (ESD) Protection

Fusion devices are tested per JEDEC Standard JESD22-A114-B.

Fusion devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to VCCI. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the Off state, except when transient voltage is significantly above VCCI or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to [Table 2-75](#) and [Table 2-76 on page 2-143](#) for more information about I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

**Table 2-75 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities**

I/O Assignment	Clamp Diode		Hot Insertion		5 V Input Tolerance <sup>1</sup>		Input Buffer	Output Buffer
	Standard I/O	Advanced I/O	Standard I/O	Advanced I/O	Standard I/O	Advanced I/O		
3.3 V LVTTTL/LVCMOS	No	Yes	Yes	No	Yes <sup>1</sup>	Yes <sup>1</sup>	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	N/A	Yes	N/A	No	N/A	Yes <sup>1</sup>	Enabled/Disabled	
LVCMOS 2.5 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V	N/A	Yes	N/A	No	N/A	Yes <sup>2</sup>	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
Differential, LVDS/BLVDS/M-LVDS/ LVPECL <sup>3</sup>	N/A	Yes	N/A	No	N/A	No	Enabled/Disabled	

**Notes:**

1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.
2. Can be implemented with an external resistor and an internal clamp diode.
3. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.

**Table 2-76 • Fusion Pro I/O – Hot-Swap and 5 V Input Tolerance Capabilities**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Input Tolerance	Input Buffer	Output Buffer
3.3 V LVTTTL/LVCMOS	No	Yes	Yes <sup>1</sup>	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes <sup>1</sup>	Enabled/Disabled	
LVCMOS 2.5 V <sup>3</sup>	No	Yes	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V <sup>3</sup>	Yes	No	Yes <sup>2</sup>	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/BLVDS/M-LVDS/LVPECL <sup>4</sup>	No	Yes	No	Enabled/Disabled	

**Notes:**

1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.
2. Can be implemented with an external resistor and an internal clamp diode.
3. In the [SmartGen](#), [FlashROM](#), [Flash Memory System Builder](#), and [Analog System Builder User Guide](#), select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V I/O standard.
4. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.

## I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. [Table 2-84](#) and [Table 2-85](#) list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

**Table 2-84 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)*	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3
PCI (3.3 V)			3		3	3
PCI-X (3.3 V)	3		3		3	3
LVDS, BLVDS, M-LVDS			3			3
LVPECL						3

**Note:** \* This feature does not apply to the standard I/O banks, which are the north I/O banks of AFS090 and AFS250 devices



### Summary of I/O Timing Characteristics – Default I/O Software Settings

**Table 2-90 • Summary of AC Measuring Points**  
Applicable to All I/O Bank Types

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

**Table 2-91 • I/O AC Parameter Definitions**

Parameter	Definition
t <sub>DP</sub>	Data to Pad delay through the Output Buffer
t <sub>PY</sub>	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t <sub>DOUT</sub>	Data to Output Buffer delay through the I/O interface
t <sub>EOUT</sub>	Enable to Output Buffer Tristate Control delay through the I/O interface
t <sub>DIN</sub>	Input Buffer to Data delay through the I/O interface
t <sub>PYS</sub>	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t <sub>HZ</sub>	Enable to Pad delay through the Output Buffer—High to Z
t <sub>ZH</sub>	Enable to Pad delay through the Output Buffer—Z to High
t <sub>LZ</sub>	Enable to Pad delay through the Output Buffer—Low to Z
t <sub>ZL</sub>	Enable to Pad delay through the Output Buffer—Z to Low
t <sub>ZHS</sub>	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t <sub>ZLS</sub>	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

**Table 2-96 • I/O Output Buffer Maximum Resistances <sup>1</sup> (continued)**

Standard	Drive Strength	R <sub>PULL-DOWN</sub> (ohms) <sup>2</sup>	R <sub>PULL-UP</sub> (ohms) <sup>3</sup>
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	17 mA	27	31
SSTL2 (II)	21 mA	13	15
SSTL3 (I)	16 mA	44	69
SSTL3 (II)	24 mA	18	32
<b>Applicable to Advanced I/O Banks</b>			
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:  
<http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2.  $R_{(PULL-DOWN-MAX)} = V_{OLspec} / I_{OLspec}$
3.  $R_{(PULL-UP-MAX)} = (V_{CCI}max - V_{OHspec}) / I_{OHspec}$

**Table 2-123 • 1.8 V LVCMOS High Slew**

Commercial Temperature Range Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ ,  
Worst-Case  $V_{CCI} = 1.7\text{ V}$   
Applicable to Advanced I/Os

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	–1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	–2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	–1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	–2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
8 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	–1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	–2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
12 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	–1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	–2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	–1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	–2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

*Note:* For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

**Table 2-124 • 1.8 V LVCMOS Low Slew**

Commercial Temperature Range Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ ,  
Worst-Case  $V_{CCI} = 1.7\text{ V}$   
Applicable to Standard I/Os

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	0.66	15.01	0.04	1.20	0.43	13.15	15.01	1.99	1.99	ns
	–1	0.56	12.77	0.04	1.02	0.36	11.19	12.77	1.70	1.70	ns
	–2	0.49	11.21	0.03	0.90	0.32	9.82	11.21	1.49	1.49	ns
4 mA	Std.	0.66	10.10	0.04	1.20	0.43	9.55	10.10	2.41	2.37	ns
	–1	0.56	8.59	0.04	1.02	0.36	8.13	8.59	2.05	2.02	ns
	–2	0.49	7.54	0.03	0.90	0.32	7.13	7.54	1.80	1.77	ns

*Note:* For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

## Differential I/O Characteristics

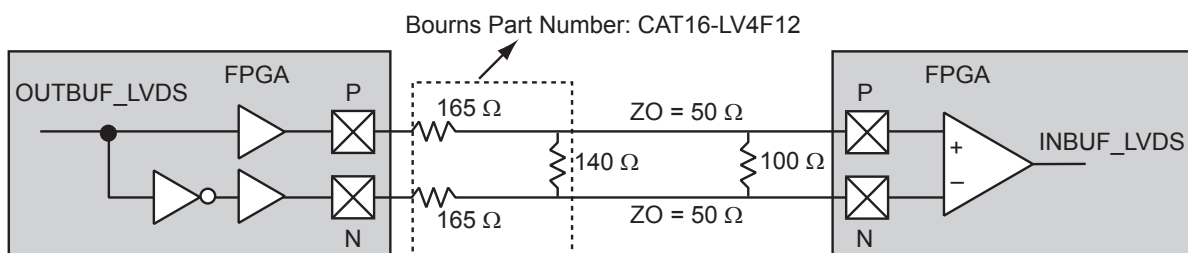
Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

### LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-134](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.



**Figure 2-134 • LVDS Circuit Diagram and Board-Level Implementation**

**Table 2-168 • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Input High Voltage	1.25	1.425	1.6	V
IOL <sup>1</sup>	Output Low Voltage	0.65	0.91	1.16	mA
IOH <sup>1</sup>	Output High Voltage	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIL <sup>2,3</sup>	Input Low Voltage			10	μA
IIH <sup>2,4</sup>	Input High Voltage			10	μA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

#### Notes:

1. IOL/IOH defined by VODIFF/(Resistor Network)
2. Currents are measured at 85°C junction temperature.
3. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
4. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.



**Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings<sup>1</sup>**

	C <sub>LOAD</sub> (pF)	V <sub>CCI</sub> (V)	Static Power PDC8 (mW) <sup>2</sup>	Dynamic Power PAC10 (μW/MHz) <sup>3</sup>
<b>Applicable to Pro I/O Banks</b>				
<b>Single-Ended</b>				
3.3 V LVTTTL/LVCMOS	35	3.3	—	474.70
2.5 V LVCMOS	35	2.5	—	270.73
1.8 V LVCMOS	35	1.8	—	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	—	104.55
3.3 V PCI	10	3.3	—	204.61
3.3 V PCI-X	10	3.3	—	204.61
<b>Voltage-Referenced</b>				
3.3 V GTL	10	3.3	—	24.08
2.5 V GTL	10	2.5	—	13.52
3.3 V GTL+	10	3.3	—	24.10
2.5 V GTL+	10	2.5	—	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
<b>Differential</b>				
LVDS	—	2.5	7.70	89.62
LVPECL	—	3.3	19.42	168.02
<b>Applicable to Advanced I/O Banks</b>				
<b>Single-Ended</b>				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	—	468.67
2.5 V LVCMOS	35	2.5	—	267.48
1.8 V LVCMOS	35	1.8	—	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	—	103.12
3.3 V PCI	10	3.3	—	201.02
3.3 V PCI-X	10	3.3	—	201.02

**Notes:**

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.
2. PDC8 is the static power (where applicable) measured on V<sub>CCI</sub>.
3. PAC10 is the total dynamic power measured on V<sub>CC</sub> and V<sub>CCI</sub>.

FG256				
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function
H3	XTAL2	XTAL2	XTAL2	XTAL2
H4	XTAL1	XTAL1	XTAL1	XTAL1
H5	GNDOSC	GNDOSC	GNDOSC	GNDOSC
H6	VCCOSC	VCCOSC	VCCOSC	VCCOSC
H7	VCC	VCC	VCC	VCC
H8	GND	GND	GND	GND
H9	VCC	VCC	VCC	VCC
H10	GND	GND	GND	GND
H11	GDC0/IO38NDB1V0	IO51NDB1V0	IO47NDB2V0	IO69NDB2V0
H12	GDC1/IO38PDB1V0	IO51PDB1V0	IO47PDB2V0	IO69PDB2V0
H13	GDB1/IO39PDB1V0	GCA1/IO49PDB1V0	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
H14	GDB0/IO39NDB1V0	GCA0/IO49NDB1V0	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
H15	GCA0/IO36NDB1V0	GCB0/IO48NDB1V0	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
H16	GCA1/IO36PDB1V0	GCB1/IO48PDB1V0	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
J1	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
J2	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
J3	IO43NDB3V0	GFB0/IO67NDB3V0	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
J4	GEC2/IO43PDB3V0	GFB1/IO67PDB3V0	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0
J5	NC	GFC0/IO68NDB3V0	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
J6	NC	GFC1/IO68PDB3V0	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0
J7	GND	GND	GND	GND
J8	VCC	VCC	VCC	VCC
J9	GND	GND	GND	GND
J10	VCC	VCC	VCC	VCC
J11	GDC2/IO41NPB1V0	IO56NPB1V0	IO56NPB2V0	IO83NPB2V0
J12	NC	GDB0/IO53NPB1V0	GDB0/IO53NPB2V0	GDB0/IO80NPB2V0
J13	NC	GDA1/IO54PDB1V0	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
J14	GDA0/IO40PDB1V0	GDC1/IO52PPB1V0	GDC1/IO52PPB2V0	GDC1/IO79PPB2V0
J15	NC	IO50NPB1V0	IO51NSB2V0	IO77NSB2V0
J16	GDA2/IO40NDB1V0	GDC0/IO52NPB1V0	GDC0/IO52NPB2V0	GDC0/IO79NPB2V0
K1	NC	IO65NPB3V0	IO67NPB4V0	IO92NPB4V0
K2	VCCIB3	VCCIB3	VCCIB4	VCCIB4
K3	NC	IO65PPB3V0	IO67PPB4V0	IO92PPB4V0
K4	NC	IO64PDB3V0	IO65PDB4V0	IO96PDB4V0
K5	GND	GND	GND	GND
K6	NC	IO64NDB3V0	IO65NDB4V0	IO96NDB4V0
K7	VCC	VCC	VCC	VCC
K8	GND	GND	GND	GND

Revision	Changes	Page
v2.0, Revision 1 (continued)	Table 3-6 • Package Thermal Resistance was updated to include new data.	3-7
	In EQ 4 to EQ 6, the junction temperature was changed from 110°C to 100°C.	3-8 to 3-8
	Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics are new and have replaced the Quiescent Supply Current Characteristics (IDDQ) table.	3-10 to 3-16
	In Table 3-14 • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices, the power supply for PAC9 and PAC10 were changed from VMV/VCC to VCCI.	3-22
	In Table 3-15 • Different Components Contributing to the Static Power Consumption in Fusion Devices, the power supply for PDC7 and PDC8 were changed from VMV/VCC to VCCI. PDC1 was updated from TBD to 18.	3-23
	The "QN108" table was updated to remove the duplicates of pins B12 and B34.	4-2
Preliminary v1.7 (October 2008)	The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.	
	For the VIL and VIH parameters, 0.30 * VCCI was changed to 0.35 * VCCI and 0.70 * VCCI was changed to 0.65 * VCCI in Table 2-126 • Minimum and Maximum DC Input and Output Levels.	2-193
	The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.	N/A
	The following updates were made to Table 2-141 • Minimum and Maximum DC Input and Output Levels: Temperature                  Digital Output 213                                  00 1111 1101 283                                  01 0001 1011 358                                  01 0110 0110 – only the digital output was updated. Temperature 358 remains in the temperature column.	2-200
	In Advance v1.2, the "VAREF Analog Reference Voltage" pin description was significantly updated but the change was not noted in the change table.	2-225
Advance v1.6 (August 2008)	The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA.	N/A
	The references to the <i>Peripherals User's Guide</i> in the "No-Glitch MUX (NGMUX)" section and "Voltage Regulator Power Supply Monitor (VRPSM)" section were changed to <i>Fusion Handbook</i> .	2-32, 2-42
Advance v1.5 (July 2008)	The following bullet was updated from High-Voltage Input Tolerance: ±12 V to High-Voltage Input Tolerance: 10.5 V to 12 V.	I
	The following bullet was updated from Programmable 1, 3, 10, 30 µA and 25 mA Drive Strengths to Programmable 1, 3, 10, 30 µA and 20 mA Drive Strengths.	I



Revision	Changes	Page
Advance v1.0 (continued)	This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to $V_{CC33A}$ .	3-8
Advance v0.9 (October 2007)	In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126	II
	In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pin: B25	3-2
	In the "180-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS090: B29 AFS250: B29	3-4
	In the "208-Pin PQFP" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS090: 102 AFS250: 102	3-8
	In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14	3-12
Advance v0.9 (continued)	In the "484-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS600: AB18 AFS1500: AB18	3-20
	In the "676-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to $V_{CC33A}$ for the following pins: AFS1500: AD20	3-28
Advance v0.8 (June 2007)	Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC.	2-20, 2-21
	Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added.	2-25
	The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator.	2-22
	Table 2-11 • Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of $I_{DYNXTAL}$ for 0.032–0.2 MHz to 0.19.	2-24
	The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR.	2-41
	The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR.	2-41