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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/u1afs600-fg256

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Flash Memory Block Diagram

A simplified diagram of the flash memory block is shown in Figure 2-33.





The logic consists of the following sub-blocks:

Flash Array

Contains all stored data. The flash array contains 64 sectors, and each sector contains 33 pages of data.

Page Buffer

A page-wide volatile register. A page contains 8 blocks of data and an AUX block.

- Block Buffer
 - Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic

The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

Program Operation

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, the total programming (including erase) time per page of the eNVM is 6.8 ms. While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified. Program errors include the following:

- 1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
- 2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
- Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
- 4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
- 5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
- 6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
- 7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in Figure 2-36.



Figure 2-36 • FB Program Waveform

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.



Device Architecture

The following error indications are possible for Read operations:

- 1. STATUS = '01' when a single-bit data error was detected and corrected within the block addressed.
- 2. STATUS = '10' when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in Table 2-23, and the definition of the page status bits is shown in Table 2-24.

Table 2-23 • Page Status Read Data Format

31	8	7	4	3	2	1	0
Write (Count	Rese	erved	Over Threshold	Read Protected	Write Protected	Overwrite Protected

Table 2-24 • Page Status Bit Definition

Page Status Bit(s)	Definition
31–8	The number of times the page addressed has been programmed/erased
7–4	Reserved; read as 0
3	Over Threshold indicator (see the "Program Operation" section on page 2-46)
2	Read Protected; read protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
1	Write Protected; write protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
0	Overwrite Protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a Program operation. The page cannot be written without first performing an Unprotect Page operation.

		By	te Nı	umbe	er in	Banl	c	4 LSB of ADDR (READ)									
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ba 3 N	7																
<u>N</u>	6																
0 of	5																
AD	4																
	3																
R R	2																
	1																
9	0																

Figure 2-45 • FlashROM Architecture

FlashROM Characteristics



Figure 2-46 • FlashROM Timing Diagram

Table 2-26 • FlashROM Access Time

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{SU}	Address Setup Time	0.53	0.61	0.71	ns
t _{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t _{CK2Q}	Clock to Out	21.42	24.40	28.68	ns
F _{MAX}	Maximum Clock frequency	15.00	15.00	15.00	MHz



SRAM and **FIFO**

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-47 for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18 , 512×9 , $1k \times 4$, $2k \times 2$, and $4k \times 1$. For example, the write size can be set to 256×18 and the read size to 512×9 .

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-27 on page 2-58.

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.



	VAREF		
	ADCGNDREF		
	AV0	DAVOUT0	
	AC0	DACOUT0	
	ΔΤΟ		
	•	DAIOUIU	
	• • •		
	AV9	DAVOUT9	
	AC9	DACOU19	
	AT9	DATOUT9	
	ATRETURN01		
	•	AG0	
	Å TRETURN9	AG1	
	DENAV0	•	
		<u>م</u>	
		A09	
	DEINATU		
	•		
	DENAV0		
	DENAC0		
	DENAT0		
	CMSTB0		
	•		
	ĊSMTB9		
	GDONO		
	CDON0		
	GDON9		
	IMSTBO		
	•		
	TMSTB9		
	MODE[3:0]	BUSY	
	TVC[7:0]	CALIBRATE	
	STC[7:0]	DATAVALID	
	CHNUMBER[4:0]	SAMPLE	
	TMSTINT	RESULTI11:01	
	ADCSTART	RTCMATCH	
	PWRDWN	RICXILSEL	
	ADCRESET	RTCPSMMATCH	
	RTCCLK		
	SYSCLK		
	ACMIVEN	ACMRDATA[7:0]	
<u> </u>	ACMRESET		
	ACMWDATA		
	ACMADDR		
	ACMCLK		
	AE	3	

Figure 2-64 • Analog Block Macro

Signal Name	Number of Bits	Direction	Function	Location of Details
AG6	1	Output		Analog Quad
AT6	1	Input		Analog Quad
ATRETURN67	1	Input	Temperature monitor return shared by Analog Quads 6 and 7	Analog Quad
AV7	1	Input	Analog Quad 7	Analog Quad
AC7	1	Input		Analog Quad
AG7	1	Output		Analog Quad
AT7	1	Input		Analog Quad
AV8	1	Input	Analog Quad 8	Analog Quad
AC8	1	Input		Analog Quad
AG8	1	Output		Analog Quad
AT8	1	Input		Analog Quad
ATRETURN89	1	Input	Temperature monitor return shared by Analog Quads 8 and 9	Analog Quad
AV9	1	Input	Analog Quad 9	Analog Quad
AC9	1	Input		Analog Quad
AG9	1	Output		Analog Quad
AT9	1	Input		Analog Quad
RTCMATCH	1	Output	МАТСН	RTC
RTCPSMMATCH	1	Output	MATCH connected to VRPSM	RTC
RTCXTLMODE[1:0]	2	Output	Drives XTLOSC RTCMODE[1:0] pins	RTC
RTCXTLSEL	1	Output	Drives XTLOSC MODESEL pin	RTC
RTCCLK	1	Input	RTC clock input	RTC

Table 2-36 • Analog Block Pin Description (continued)

Analog Quad

With the Fusion family, Microsemi introduces the Analog Quad, shown in Figure 2-65 on page 2-81, as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending it to the ADC for conversion into a digital signal. To maximize the usefulness of the Analog Quad, the analog input signals can also be configured as LVTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block, and its input pin is named AV. It contains a twochannel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler can be configured to accept analog signals between -12 V and 0 or between 0 and +12 V. The prescaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin can also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than 1 Ω) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage that can then be read using the ADC.

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage-monitoring capabilities unique in the FPGA industry. The Analog Quad comprises three analog input pads— Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-66), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.



Figure 2-66 • Analog Quad Direct Connect

The Analog Quad offers a wide variety of prescaling options to enable the ADC to resolve the input signals. Figure 2-67 shows the path through the Analog Quad for a signal that is to be prescaled prior to conversion. The ADC internal reference voltage and the prescaler factors were selected to make both prescaling and postscaling of the signals easy binary calculations (refer to Table 2-57 on page 2-130 for details). When an analog input pad is configured with a prescaler, there will be a 1 M Ω resistor to ground. This occurs even when the device is in power-down mode. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, analog inputs are pulled down to ground through a 1 M Ω resistor. The gate driver output is floating (or tristated), and there is no extra current on VCC33A.

These scaling factors hold true whether the particular pad is configured to accept a positive or negative voltage. Note that whereas the AV and AC pads support the same prescaling factors, the AT pad supports a reduced set of prescaling factors and supports positive voltages only.



Device Architecture

ADC Description

The Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of features for different use models. Figure 2-80 shows a block diagram of the Fusion ADC.

- · Configurable resolution: 8-bit, 10-bit, and 12-bit mode
- DNL: 0.6 LSB for 10-bit mode
- INL: 0.4 LSB for 10-bit mode
- No missing code
- Internal VAREF = 2.56 V
- Maximum Sample Rate = 600 Ksps
- Power-up calibration and dynamic calibration after every sample to compensate for temperature drift over time



Figure 2-80 • ADC Simplified Block Diagram

ADC Theory of Operation

An analog-to-digital converter is used to capture discrete samples of a continuous analog voltage and provide a discrete binary representation of the signal. Analog-to-digital converters are generally characterized in three ways:

- Input voltage range
- Resolution
- Bandwidth or conversion rate

The input voltage range of an ADC is determined by its reference voltage (VREF). Fusion devices include an internal 2.56 V reference, or the user can supply an external reference of up to 3.3 V. The following examples use the internal 2.56 V reference, so the full-scale input range of the ADC is 0 to 2.56 V.

The resolution (LSB) of the ADC is a function of the number of binary bits in the converter. The ADC approximates the value of the input voltage using 2n steps, where n is the number of bits in the converter. Each step therefore represents VREF÷ 2n volts. In the case of the Fusion ADC configured for 12-bit operation, the LSB is 2.56 V / 4096 = 0.625 mV.

Finally, bandwidth is an indication of the maximum number of conversions the ADC can perform each second. The bandwidth of an ADC is constrained by its architecture and several key performance characteristics.

Analog MUX Channel	Signal	Analog Quad Number			
16	AV5				
17	AC5	Analog Quad 5			
18	AT5				
19	AV6				
20	AC6	Analog Quad 6			
21	AT6				
22	AV7				
23	AC7	Analog Quad 7			
24	AT7				
25	AV8				
26	AC8	Analog Quad 8			
27	AT8				
28	AV9				
29	AC9	Analog Quad 9			
30	AT9				
31	Internal temperature monitor				

Table 2-40 • Analog MUX Channels (continued)

The ADC can be powered down independently of the FPGA core, as an additional control or for powersaving considerations, via the PWRDWN pin of the Analog Block. The PWRDWN pin controls only the comparators in the ADC.

ADC Modes

The Fusion ADC can be configured to operate in 8-, 10-, or 12-bit modes, power-down after conversion, and dynamic calibration. This is controlled by MODE[3:0], as defined in Table 2-41 on page 2-106.

The output of the ADC is the RESULT[11:0] signal. In 8-bit mode, the Most Significant 8 Bits RESULT[11:4] are used as the ADC value and the Least Significant 4 Bits RESULT[3:0] are logical '0's. In 10-bit mode, RESULT[11:2] are used the ADC value and RESULT[1:0] are logical 0s.

Name	Bits	Function
MODE	3	 0 – Internal calibration after every conversion; two ADCCLK cycles are used after the conversion. 1 – No calibration after every conversion
MODE	2	0 – Power-down after conversion 1 – No Power-down after conversion
MODE	1:0	00 – 10-bit 01 – 12-bit 10 – 8-bit 11 – Unused

User I/Os

Introduction

Fusion devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-68, Table 2-69, Table 2-70, and Table 2-71 on page 2-135 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V–tolerant. See the "5 V Input Tolerance" section on page 2-144 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-5 for more information. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, digital inputs are tristated, digital outputs are tristated, and digital bibufs (input/output) are tristated.

I/O Tile

The Fusion I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-99 on page 2-133). The registers can also be used to support the JESD-79C DDR standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-139 for more information).

As depicted in Figure 2-100 on page 2-138, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-138 for more information.

I/O Banks and I/O Standards Compatibility

The digital I/Os are grouped into I/O voltage banks. There are three digital I/O banks on the AFS090 and AFS250 devices and four digital I/O banks on the AFS600 and AFS1500 devices. Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159 show the bank configuration by device. The north side of the I/O in the AFS600 and AFS1500 devices comprises two banks of Pro I/Os. The Pro I/Os support a wide number of voltage-referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all Microsemi digital I/Os. Each I/O voltage bank has dedicated I/O supply and ground voltages (VCCI/GNDQ for input buffers and VCCI/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-69 and Table 2-70 on page 2-134 show the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Package Pin Assignments" on page 4-1 and the "User I/O Naming Convention" section on page 2-158.

Each Pro I/O bank is divided into minibanks. Any user I/O in a VREF minibank (a minibank is the region of scope of a VREF pin) can be configured as a VREF pin (Figure 2-99 on page 2-133). Only one VREF pin is needed to control the entire VREF minibank. The location and scope of the VREF minibanks can be determined by the I/O name. For details, see the "User I/O Naming Convention" section on page 2-158.

Table 2-70 on page 2-134 shows the I/O standards supported by Fusion devices and the corresponding voltage levels.

I/O standards are compatible if the following are true:

- Their VCCI values are identical.
- If both of the standards need a VREF, their VREF values must be identical (Pro I/O only).



Figure 2-102 • DDR Output Support in Fusion Devices

Timing Characteristics

Table 2-128 • 1.5 V LVCMOS Low Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Pro I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	-1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	-2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	-1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	-2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
8 mA	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	-1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	-2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
12 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	-1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	-2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-129 • 1.5 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Pro I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOU} T	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	-1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	-2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	-1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	-2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
8 mA	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	-1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	-2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
12 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	-1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	-2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-132 • 1.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	12.33	0.04	1.42	0.43	11.79	12.33	2.45	2.32	ns
	-1	0.56	10.49	0.04	1.21	0.36	10.03	10.49	2.08	1.98	ns
	-2	0.49	9.21	0.03	1.06	0.32	8.81	9.21	1.83	1.73	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-133 • 1.5 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Standard I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	7.65	0.04	1.42	0.43	6.31	7.65	2.45	2.45	ns
	-1	0.56	6.50	0.04	1.21	0.36	5.37	6.50	2.08	2.08	ns
	-2	0.49	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • AFS1500 Quiescent Supply Current Characteristics

Parameter	Description	Conditions	Temp.	Min.	Тур.	Max.	Unit
ICC ¹	1.5 V quiescent current	Operational standby ⁴ ,	T _J = 25°C		20	40	mA
		VCC = 1.575 V	T _J = 85°C		32	65	mA
			T _J = 100°C		59	120	mA
		Standby mode ⁵ or Sleep mode ⁶ , VCC = 0 V			0	0	μA
ICC33 ²	3.3 V analog supplies	Operational standby ⁴ ,	T _J = 25°C		9.8	13	mA
	current	VCC33 = 3.63 V	T _J = 85°C		10.7	14	mA
			T _J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T _J = 25°C		0.31	2	mA
			T _J = 85°C		0.35	2	mA
			T _J = 100°C		0.45	2	mA
		Standby mode ⁵ , VCC33 = 3.63 V	T _J = 25°C		2.9	3.6	mA
			T _J = 85°C		2.9	4	mA
			T _J = 100°C		3.3	6	mA
		Sleep mode ⁶ , VCC33 = 3.63 V	T _J = 25°C		17	19	μA
			T _J = 85°C		18	20	μA
			T _J = 100°C		24	25	μA
ICCI ³	I/O quiescent current	Operational standby ⁴ ,	T _J = 25°C		417	649	μA
		Standby mode, and Sleep Mode ^o , VCCIx = 3.63 V	T _J = 85°C		417	649	μA
			T _J = 100°C		417	649	μA

Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.



 $P_{S-CELL} = 0 W$ $P_{C-CELL} = 0 W$ $P_{NET} = 0 W$ $P_{LOGIC} = 0 W$

I/O Input and Output Buffer Contribution—P_{I/O}

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

 $F_{CLK} = 50 \text{ MHz}$ Number of input pins used: N_{INPUTS} = 30 Number of output pins used: N_{OUTPUTS} = 40 Estimated I/O buffer toggle rate: α_2 = 0.1 (10%) Estimated IO buffer enable rate: β_1 = 1 (100%)

Operating Mode

$$\begin{split} \mathsf{P}_{\mathsf{INPUTS}} &= \mathsf{N}_{\mathsf{INPUTS}} * (\alpha_2 \,/\, 2) * \mathsf{PAC9} * \mathsf{F}_{\mathsf{CLK}} \\ \mathsf{P}_{\mathsf{INPUTS}} &= 30 * (0.1 \,/\, 2) * 0.01739 * 50 \\ \mathsf{P}_{\mathsf{INPUTS}} &= 1.30 \text{ mW} \end{split}$$

$$\begin{split} \mathsf{P}_{\text{OUTPUTS}} &= \mathsf{N}_{\text{OUTPUTS}} * (\alpha_2 / 2) * \beta_1 * \mathsf{PAC10} * \mathsf{F}_{\text{CLK}} \\ \mathsf{P}_{\text{OUTPUTS}} &= 40 * (0.1 / 2) * 1 * 0.4747 * 50 \\ \mathsf{P}_{\text{OUTPUTS}} &= 47.47 \text{ mW} \end{split}$$

 $P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$ $P_{I/O} = 1.30 \text{ mW} + 47.47 \text{ mW}$

P_{I/O} = 48.77 mW

Standby Mode and Sleep Mode

 $P_{INPUTS} = 0 W$

 $P_{OUTPUTS} = 0 W$ $P_{I/O} = 0 W$

RAM Contribution—P_{MEMORY}

Frequency of Read Clock: $F_{READ-CLOCK} = 10 \text{ MHz}$ Frequency of Write Clock: $F_{WRITE-CLOCK} = 10 \text{ MHz}$ Number of RAM blocks: $N_{BLOCKS} = 20$ Estimated RAM Read Enable Rate: $\beta_2 = 0.125 (12.5\%)$ Estimated RAM Write Enable Rate: $\beta_3 = 0.125 (12.5\%)$

Operating Mode

$$\begin{split} \mathsf{P}_{\mathsf{MEMORY}} &= (\mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{PAC11} * \beta_2 * \mathsf{F}_{\mathsf{READ-CLOCK}}) + (\mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{PAC12} * \beta_3 * \mathsf{F}_{\mathsf{WRITE-CLOCK}}) \\ \mathsf{P}_{\mathsf{MEMORY}} &= (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10) \\ \mathsf{P}_{\mathsf{MEMORY}} &= 1.38 \text{ mW} \end{split}$$

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W



4 – Package Pin Assignments

QN108



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

🌜 Microsemi.

Package Pin Assignments

FG676			FG676	FG676			
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	Pin Number	AFS1500 Function		
L17	VCCIB2	N1	NC	P11	VCC		
L18	GCB2/IO60PDB2V0	N2	NC	P12	GND		
L19	IO58NDB2V0	N3	IO108NDB4V0	P13	VCC		
L20	IO57NDB2V0	N4	VCCOSC	P14	GND		
L21	IO59NDB2V0	N5	VCCIB4	P15	VCC		
L22	GCC2/IO61PDB2V0	N6	XTAL2	P16	GND		
L23	IO55PPB2V0	N7	GFC1/IO107PDB4V0	P17	VCCIB2		
L24	IO56PDB2V0	N8	VCCIB4	P18	IO70NDB2V0		
L25	IO55NPB2V0	N9	GFB1/IO106PDB4V0	P19	VCCIB2		
L26	GND	N10	VCCIB4	P20	IO69NDB2V0		
M1	NC	N11	GND	P21	GCA0/IO64NDB2V0		
M2	VCCIB4	N12	VCC	P22	VCCIB2		
M3	GFC2/IO108PDB4V0	N13	GND	P23	GCB0/IO63NDB2V0		
M4	GND	N14	VCC	P24	GCB1/IO63PDB2V0		
M5	IO109NDB4V0	N15	GND	P25	IO66NDB2V0		
M6	IO110NDB4V0	N16	VCC	P26	IO67PDB2V0		
M7	GND	N17	VCCIB2	R1	NC		
M8	IO104NDB4V0	N18	IO70PDB2V0	R2	VCCIB4		
M9	IO111NDB4V0	N19	VCCIB2	R3	IO103NDB4V0		
M10	GND	N20	IO69PDB2V0	R4	GND		
M11	VCC	N21	GCA1/IO64PDB2V0	R5	IO101PDB4V0		
M12	GND	N22	VCCIB2	R6	IO100NPB4V0		
M13	VCC	N23	GCC0/IO62NDB2V0	R7	GND		
M14	GND	N24	GCC1/IO62PDB2V0	R8	IO99PDB4V0		
M15	VCC	N25	IO66PDB2V0	R9	IO97PDB4V0		
M16	GND	N26	IO65NDB2V0	R10	GND		
M17	GND	P1	NC	R11	GND		
M18	IO60NDB2V0	P2	NC	R12	VCC		
M19	IO58PDB2V0	P3	IO103PDB4V0	R13	GND		
M20	GND	P4	XTAL1	R14	VCC		
M21	IO68NPB2V0	P5	VCCIB4	R15	GND		
M22	IO61NDB2V0	P6	GNDOSC	R16	VCC		
M23	GND	P7	GFC0/IO107NDB4V0	R17	GND		
M24	IO56NDB2V0	P8	VCCIB4	R18	GDB2/IO83PDB2V0		
M25	VCCIB2	P9	GFB0/IO106NDB4V0	R19	IO78PDB2V0		
M26	IO65PDB2V0	P10	VCCIB4	R20	GND		

Fusion Family of Mixed Signal FPGAs

Revision	Changes	Page
Advance v0.8 (continued)	This sentence was updated in the "No-Glitch MUX (NGMUX)" section to delete GLA: The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC).	2-32
	In Table 2-13 • NGMUX Configuration and Selection Table, 10 and 11 were deleted.	2-32
	The method to enable sleep mode was updated for bit 0 in Table 2-16 • RTC Control/Status Register.	2-38
	S2 was changed to D2 in Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access) for RD[31:0] was updated.	2-51
	The definitions for bits 2 and 3 were updated in Table 2-24 • Page Status Bit Definition.	2-52
	Figure 2-46 • FlashROM Timing Diagram was updated.	2-58
	Table 2-26 • FlashROM Access Time is new.	2-58
	Figure 2-55 • Write Access After Write onto Same Address, Figure 2-56 • Read Access After Write onto Same Address, and Figure 2-57 • Write Access After Read onto Same Address are new.	2-68– 2-70
	Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated.	2-71, 2-72
	The VAREF and SAMPLE functions were updated in Table 2-36 • Analog Block Pin Description.	2-82
	The title of Figure 2-72 • Timing Diagram for Current Monitor Strobe was updated to add the word "positive."	2-91
	The "Gate Driver" section was updated to give information about the switching rate in High Current Drive mode.	2-94
	The "ADC Description" section was updated to include information about the SAMPLE and BUSY signals and the maximum frequencies for SYSCLK and ADCCLK. EQ 2 was updated to add parentheses around the entire expression in the denominator.	2-102
	Table 2-46 \cdot Analog Channel Specifications and Table 2-47 \cdot ADC Characteristics in Direct Input Mode were updated.	2-118, 2-121
	The note was removed from Table 2-55 • Analog Multiplexer Truth Table—AV ($x = 0$), AC ($x = 1$), and AT ($x = 3$).	2-131
	Table 2-63 • Internal Temperature Monitor Control Truth Table is new.	2-132
	The "Cold-Sparing Support" section was updated to add information about cases where current draw can occur.	2-143
	Figure 2-104 • Solution 4 was updated.	2-147
	Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings was updated.	2-153
	The "GNDA Ground (analog)" section and "GNDAQ Ground (analog quiet)" section were updated to add information about maximum differential voltage.	2-224
	The "V _{AREF} Analog Reference Voltage" section and "VPUMP Programming Supply Voltage" section were updated.	2-226
	The "V_{CCPLA/B} PLL Supply Voltage" section was updated to include information about the east and west PLLs.	2-225
	The V _{COMPLF} pin description was deleted.	N/A
	The "Axy Analog Input/Output" section was updated with information about grounding and floating the pin.	2-226



Datasheet Information

Revision	Changes	Page		
Advance v0.5	The low power modes of operation were updated and clarified.			
(June 2006)	The AFS1500 digital I/O count was updated in Table 1 • Fusion Family.	i		
	The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double- Ended (Analog)" table.	ii		
	The "Voltage Regulator Power Supply Monitor (VRPSM)" was updated.	2-36		
	Figure 2-45 • FlashROM Timing Diagram was updated.	2-53		
	The "256-Pin FBGA" table for the AFS1500 is new.	3-12		
Advance v0.4 (April 2006)	The G was moved in the "Product Ordering Codes" section.	III		
Advance v0.3	The "Features and Benefits" section was updated.	I		
(April 2006)	The "Fusion Family" table was updated.	I		
	The "Package I/Os: Single-/Double-Ended (Analog)" table was updated.	П		
	The "Product Ordering Codes" table was updated.	Ш		
	The "Temperature Grade Offerings" table was updated.	IV		
	The "General Description" section was updated to include ARM information.	1-1		
	Figure 2-46 • FlashROM Timing Diagram was updated.	2-58		
	The "FlashROM" section was updated.	2-57		
	The "RESET" section was updated.	2-61		
	The "RESET" section was updated.	2-64		
	Figure 2-27 · Real-Time Counter System was updated.	2-35		
	Table 2-19 • Flash Memory Block Pin Names was updated.	2-43		
	Figure 2-33 • Flash Memory Block Diagram was updated to include AUX block information.	2-45		
	Figure 2-34 • Flash Memory Block Organization was updated to include AUX block information.	2-46		
	The note in the "Program Operation" section was updated.	2-48		
	Figure 2-76 • Gate Driver Example was updated.	2-95		
	The "Analog Quad ACM Description" section was updated.	2-130		
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94		
	Figure 2-65 • Analog Block Macro was updated.	2-81		
	Figure 2-65 • Analog Block Macro was updated.	2-81		
	The "Analog Quad" section was updated.	2-84		
	The "Voltage Monitor" section was updated.	2-86		
	The "Direct Digital Input" section was updated.	2-89		
	The "Current Monitor" section was updated.	2-90		
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94		