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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9402fbd-557

- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Watchdog timer with separate on-chip oscillator, nominal 400 kHz, calibrated to ±5 %, requiring no external components. The watchdog prescaler is selectable from eight values.
- High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- Switching on the fly among internal RC oscillator, watchdog oscillator, external clock source provides optimal support of minimal power active mode with fast switching to maximum performance.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 µA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open-drain, push-pull, input-only.
- High current sourcing/sinking (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Port 'input pattern match' detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC9402 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P1.5/$\overline{\text{RST}}$	11	I	**P1.5** — Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$** — External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.
P1.6	10	I/O	**P1.6** — Port 1 bit 6. High current source.
P1.7	9	I/O	**P1.7** — Port 1 bit 7. High current source.
P2.0 to P2.3, P2.5		I/O	**Port 2:** Port 2 is an 5-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.14.1 "Port configurations" and Table 12 "Static electrical characteristics" for details. All pins have Schmitt trigger inputs. Port 2 also provides various special functions as described below:
P2.0	6	I/O	**P2.0** — Port 2 bit 0.
P2.1	7	I/O	**P2.1** — Port 2 bit 1.
P2.2/MOSI	18	I/O	**P2.2** — Port 2 bit 2.
		I/O	**MOSI** — SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	19	I/O	**P2.3** — Port 2 bit 3.
		I/O	**MISO** — When configured as master, this pin is input, when configured as slave, this pin is output.
P2.5/SPICLK	20	I/O	**P2.5** — Port 2 bit 5.
		I/O	**SPICLK** — SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.14.1 "Port configurations" and Table 12 "Static electrical characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	14	I/O	**P3.0** — Port 3 bit 0.
		O	**XTAL2** — Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
		O	**CLKOUT** — CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	13	I/O	**P3.1** — Port 3 bit 1.
		I	**XTAL1** — Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
SDA_LCD	63	I/O	**SDA LCD** — I^{2}C-bus data signal for the LCD controller.
SCL_LCD	64	I/O	**SCL LCD** — I^{2}C-bus clock signal for the LCD controller.
BP0 to BP3	27 to 30	O	**BP0 to BP3:** LCD backplane outputs.

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[2]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[2]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	I2PD	SPPD	SPD	-	00[2]	0000 0000
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	BOIF	BOF	POF	R_BK	R_WD	R_SF	R_EX		[3]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[2][4]	011x xx00
RTCH	Real-time clock register high	D2H									00[4]	0000 0000
RTCL	Real-time clock register low	D3H									00[4]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
		Bit address	9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000

Table 5. Extended special function registers[1]

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	-	BOICFG1	BOICFG0	[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	-	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	[3]	
RTCDATH	Real-time clock data register high	FFBFH									00	0000 0000
RTCDATL	Real-time clock data register low	FFBEH									00	0000 0000

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.

7.8 CPU Clock (CCLK) wake-up delay

The P89LPC9402 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 1024 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is the internal RC oscillator, the delay is 200 μs to 300 μs. If the clock source is watchdog oscillator or external clock, the delay is 32 OSCCLK cycles.

7.9 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.10 Low power select

The P89LPC9402 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

7.11 Memory organization

The various P89LPC9402 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.
- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.
- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

7.14.1 Port configurations

All but three I/O port pins on the P89LPC9402 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open-drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.
2. P1.2 (SCL/T0) and P1.3 (SDA/$\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

7.14.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC9402 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.14.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.14.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

7.14.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt trigger input that also has a glitch suppression circuit.The P89LPC9402 device has high current source on eight pins in push-pull mode. See Table 11 “Limiting values”.

7.14.2 Port 0 analog functions

The P89LPC9402 incorporates two analog comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

7.14.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC9402 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 12 "Static electrical characteristics" for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.15 Power monitoring functions

The P89LPC9402 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

7.15.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. Enhanced brownout detection has 3 independent functions: BOD reset, BOD interrupt and BOD FLASH.

BOD reset is always on except in total Power-down mode. It could not be disabled in software. BOD interrupt may be enabled or disabled in software. BOD FLASH is always on, except in Power-down modes and could not be disabled in software.

BOD reset and BOD interrupt, each has four trip voltage levels. BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are used as trip point configuration bits of BOD reset. BOICFG1 bit and BOICFG0 bit in register BODCFG are used as trip point configuration bits of BOD interrupt. BOD reset voltage should be lower than BOD interrupt trip point. BOD FLASH is used for flash programming/erase protection and has only 1 trip voltage of 2.4 V. Please refer to P89LPC9402 *User manual* for detail configurations.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage and is negated when V_{DD} rises above the brownout trip voltage.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 12 "Static electrical characteristics" for specifications.

7.18.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.18.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.18.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.18.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

7.18.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.19 RTC/system timer

The P89LPC9402 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator. Only power-on reset and watchdog reset will reset the RTC and its associated SFRs to the default state.

The 16-bit loadable counter portion of the RTC is readable by reading the RTCDATL and RTCDATH registers.

7.20 UART

The P89LPC9402 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC9402 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^1/_{16}$ of the CPU clock frequency.

7.22 SPI

The P89LPC9402 provides another high-speed serial communication interface, the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 4.5 Mbit/s can be supported in Master mode or up to 3 Mbit/s in Slave mode. It has a transfer completion flag and write collision flag protection.

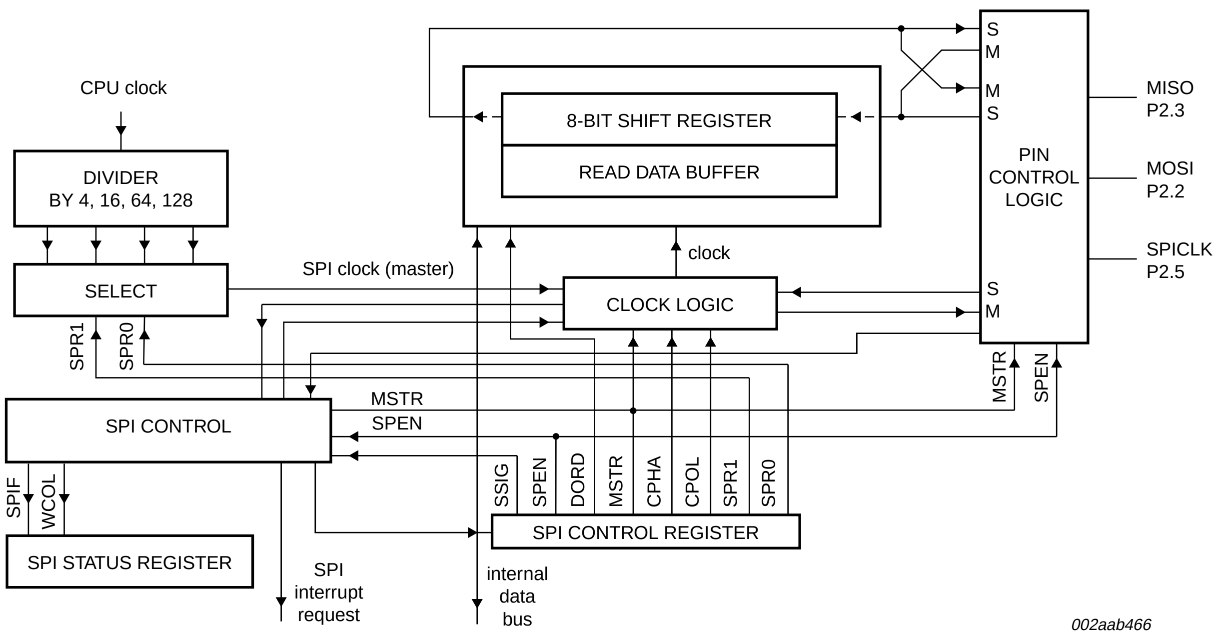


Fig 11. SPI block diagram

The SPI interface has three pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.

Typical connections are shown in Figure 12 through Figure 14.

7.23 Analog comparators

Two analog comparators are provided on the P89LPC9402. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 15. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 μs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

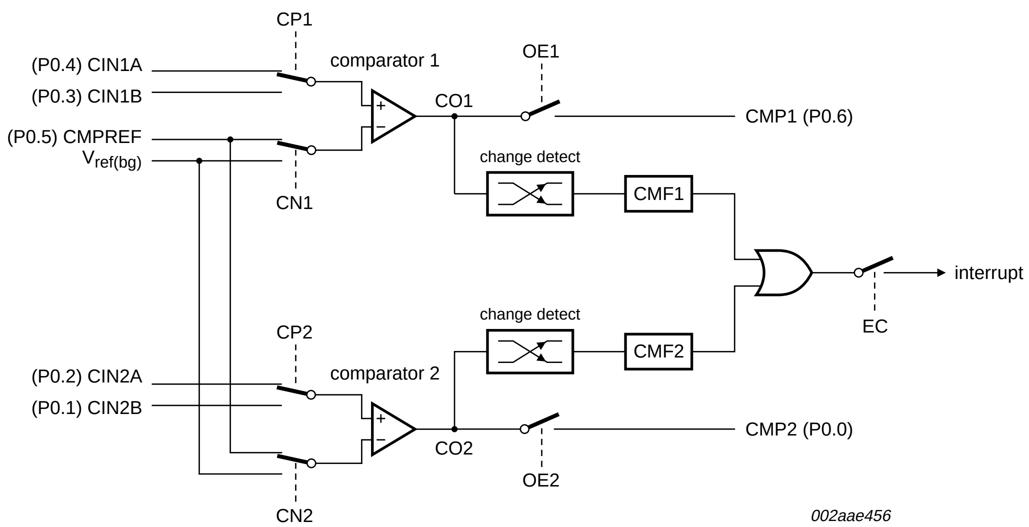


Fig 15. Comparator input and output connections

7.23.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is 1.23 V ± 10 %.

7.23.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

7.23.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

7.24 Keypad interrupt

The Keypad Interrupt (KBI) function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

7.27.5 Timing

The LCD controller timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock.

Frame frequency = $f_{osc(LCD)}/24$.

7.27.6 Display register

A display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs, and each column of the display RAM.

7.27.7 Segment outputs

The LCD drive section includes 32 segment outputs S0 to S31. The segment output signals are generated according to the multiplexed backplane signals and the display latch data. When less than 32 segment outputs are required, the unused segment outputs should be left open-circuit.

7.27.8 Backplane outputs

The LCD drive section has four backplane outputs BP0 to BP3. The backplane output signals are generated in based on the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit. In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.27.9 Display RAM

The display RAM is a static 32 $\times$ 4-bit RAM which stores LCD data. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 32 segments for backplane 0 (BP0). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

7.27.10 Data pointer

The Display RAM is addressed using the data pointer. Either a single byte or a series of display bytes may be loaded into any location of the display RAM.

7.27.11 Output bank selector

The LCD controller includes a RAM bank switching feature in the static and 1:2 drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This allows display information to be prepared in an alternative bank and then selected for display when it is assembled.

7.27.12 Input bank selector

The input bank selector loads display data into the display RAM based on the selected LCD drive configuration. The BANK SELECT command can be used to load display data in bit 2 in static drive mode or in bits 2 and 3 in 1:2 mode. The input bank selector functions are independent of the output bank selector.

7.27.13 Blinker

The LCD controller has a very versatile display blinking capability. The whole display can blink at a frequency selected by the BLINK command. Each blink frequency is a multiple integer value of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected, as shown in Table 9.

An additional feature allows an arbitrary selection of LCD segments to be blinked in the static and 1:2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the BLINK command.

The entire display can be blinked at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 9. Blinking frequencies

Blink mode	Normal operating mode ratio	Normal blink frequency
Off	-	Blinking off
2 Hz	$f_{osc(LCD)}/768$	2 Hz
1 Hz	$f_{osc(LCD)}/1536$	1 Hz
0.5 Hz	$f_{osc(LCD)}/3072$	0.5 Hz

Blink modes 0.5 Hz, 1 Hz and 2 Hz, and nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency ($f_{osc(LCD)}$) of 1536 Hz at pin CLK. The oscillator frequency range is 397 Hz to 3046 Hz.

7.27.13.1 I^{2}C-bus controller

The LCD controller acts as an I^{2}C-bus slave receiver. In the P89LPC9402 the hardware subaddress inputs A0, A,1 and A2 are tied to V_{SS} setting the hardware subaddress = 0.

7.27.14 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.27.15 I^{2}C-bus slave addresses

The I^{2}C-bus slave address is 0111 0000. The LCD controller is a write-only device and will not respond to a read access.

in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

7.28.9 Power-on reset code execution

The P89LPC9402 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC9402 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 10 shows the factory default Boot Vector setting for these devices. A factory-provided bootloader is pre-programmed into the address space indicated and uses the indicated bootloader entry point to perform ISP functions. This code can be erased by the user.

Remark: Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this bootloader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.

A custom bootloader can be written with the Boot Vector set to the custom bootloader, if desired.

Table 10. Default Boot Vector values and ISP entry points

Device	Default Boot Vector	Default boot loader entry point	Default boot loader code range	1 kB sector range
P89LPC9402	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.28.10 Hardware activation of the bootloader

The bootloader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC9402 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the Boot Vector (1FH) is changed, it will no longer point to the factory preprogrammed ISP bootloader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.29 User configuration bytes

Some user-configurable features of the P89LPC9402 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1 and UCFG2. Please see the P89LPC9402 *User Manual* for additional details.

7.30 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC9402 device. Each byte corresponds to one sector. Please see the P89LPC9402 *User manual* for additional details.

Table 12. Static electrical characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0	2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage		1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, V_{DD} = 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 8 “Limiting values” on page 44 for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] Pin capacitance is characterized but not tested.

[6] Measured with port in quasi-bidirectional mode.

[7] Measured with port in high-impedance mode.

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 14. Dynamic characteristics (18 MHz) *…continued*

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 19, 20, 21, 22					
	master		$^{2}/_{CCLK}$	-	111	-	ns
	slave		$^{3}/_{CCLK}$	-	167	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 19, 20, 21, 22					
	master		$^{2}/_{CCLK}$	-	111	-	ns
	slave		$^{3}/_{CCLK}$	-	167	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 19, 20, 21, 22	100	-	100	-	ns
	master or slave						
t_{SPIDH}	SPI data hold time	see Figure 19, 20, 21, 22	100	-	100	-	ns
	master or slave						
t_{SPIA}	SPI access time	see Figure 21, 22					
	slave		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 21, 22					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 19, 20, 21, 22					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 19, 20, 21, 22	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 19, 20, 21, 22					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 19, 20, 21, 22					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

11. Other characteristics

11.1 Comparator electrical characteristics

Table 16. Comparator electrical characteristics

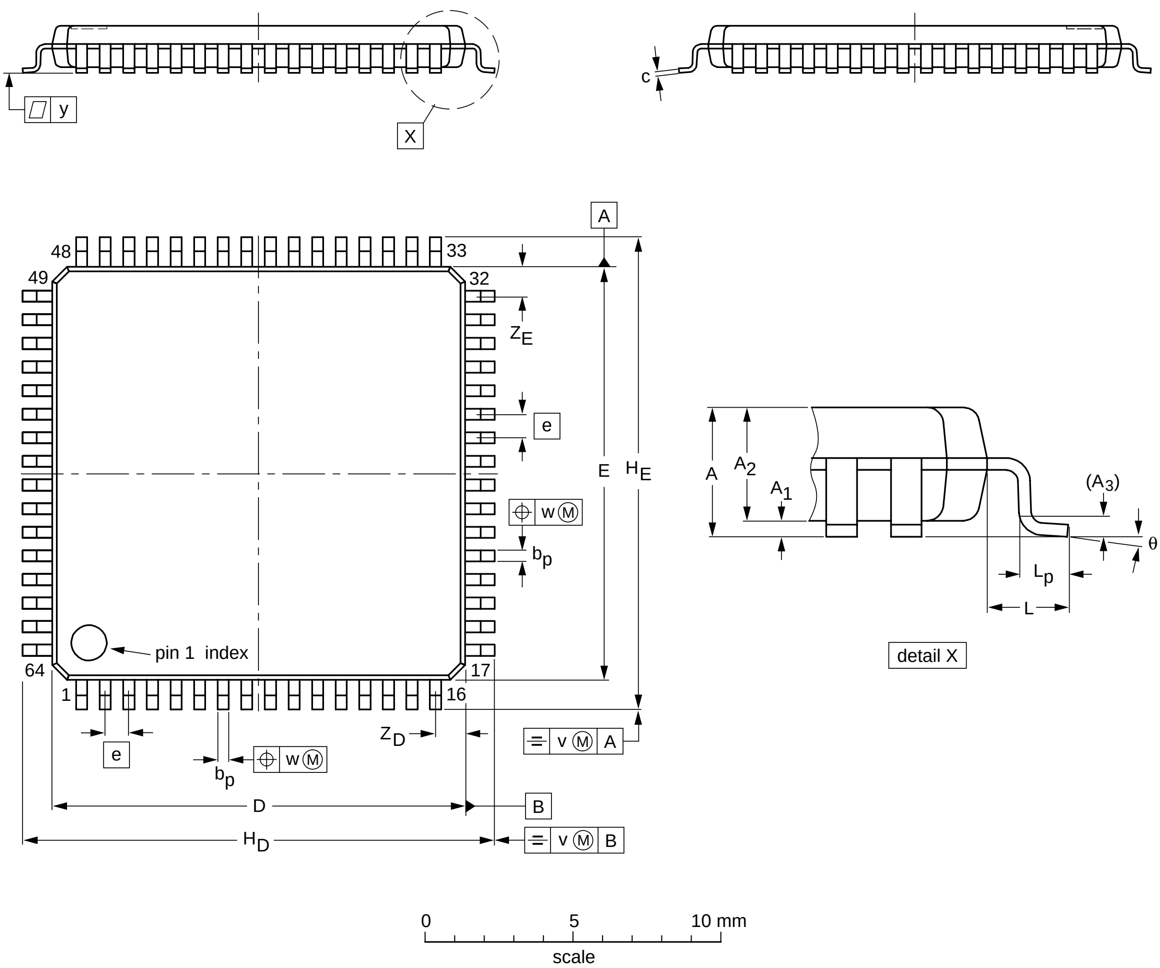
V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±20	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	µs
I_{LI}	input leakage current	0 V < V_I < V_{DD}	-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

12. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 14 x 14 x 1.4 mm **SOT791-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.09	14.1 13.9	14.1 13.9	0.8	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT791-1	136E18	MS-026	ED-7311EC			02-10-22

Fig 24. Package outline SOT791-1 (LQFP64)

13. Abbreviations

Table 17. Acronym list

Acronym	Description
BOD	Brownout Detect
CPU	Central Processing Unit
EPROM	Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
LCD	Liquid Crystal Display
LED	Light Emitting Diode
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
WDT	WatchDog Timer

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For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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