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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128a1-aur

1. Ordering Information

Ordering Code	Flash (B)	E^2	SRAM	Speed (MHz)	Power Supply	Package[1][2][3]	Temp
ATxmega128A1-AU	128K + 8K	2 KB	8 KB	32	1.6 - 3.6V	100A	-40°C - 85°C
ATxmega128A1-AUR							
ATxmega64A1-AU	64K + 4K	2 KB	4 KB				
ATxmega64A1-AUR							
ATxmega128A1-CU	128K + 8K	2 KB	8 KB			100C1	
ATxmega128A1CUR							
ATxmega64A1-CU	64K + 4K	2 KB	4 KB				
ATxmega64A1-CUR							
ATxmega128A1-C7U	128K + 8K	2 KB	8 KB			100C2	
ATxmega128A1-C7UR							
ATxmega64A1-C7U	64K + 4K	2 KB	4 KB				
ATxmega64A1-C7UR							

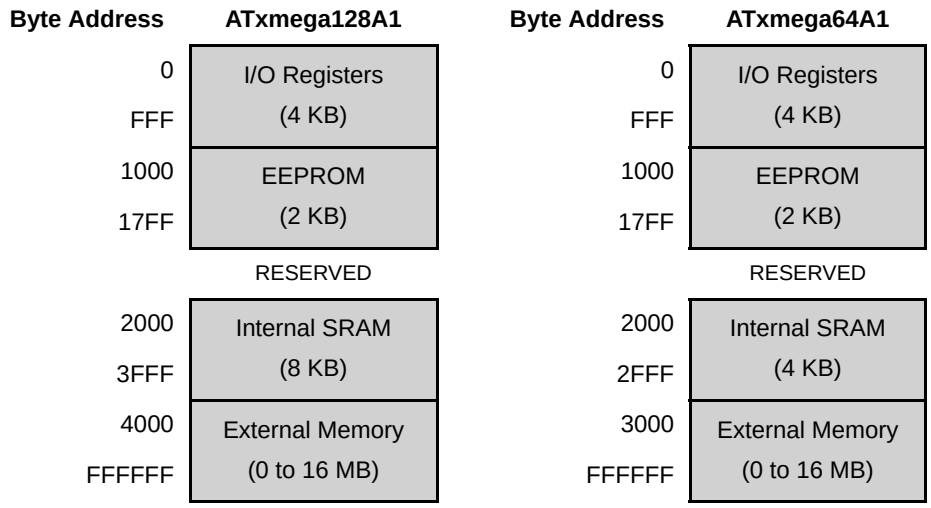
Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see “Packaging information” on page 70.

Package Type	
100A	100-lead, 14 x 14 x 1.0mm, 0.5mm lead pitch, thin profile plastic quad flat package (TQFP)
100C1	100-ball, 9 x 9 x 1.2mm body, ball pitch 0.88mm, chip ball grid array (CBGA)
100C2	100-ball, 7 x 7 x 1.0mm body, ball pitch 0.65mm, very thin fine-pitch ball grid array (VFBGA)

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	Sensor control	HVAC
Board control	Optical	Utility metering
White goods	Medical applications	

Figure 8-2. Data Memory Map (Hexadecimal address)



8.6 EEPROM

XMEGA AU devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

8.7 I/O Memory

The status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which is used to transfer data between the 32 registers in the register file and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly. In the address range 0x00 - 0x1F, single- cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules in XMEGA A1U is shown in the “Peripheral Module Address Map” on page 62.

8.7.1 General Purpose I/O Registers

The lowest 16 I/O memory addresses are reserved as general purpose I/O registers. These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

8.8 External Memory

Four ports can be used for external memory, supporting external SRAM, SDRAM, and memory mapped peripherals such as LCD displays. Refer to “EBI – External Bus Interface” on page 47. The external memory address space will always start at the end of internal SRAM.

8.9 Data Memory and Bus Arbitration

Since the data memory is organized as four separate sets of memories, the different bus masters (CPU, DMA controller read and DMA controller write, etc.) can access different memory sections at the same time.

9. DMAC - Direct Memory Access Controller

9.1 Features

- Allows High-speed data transfer
  - From memory to peripheral
  - From memory to memory
  - From peripheral to memory
  - From peripheral to peripheral
- 4 Channels
- From 1 byte and up to 16M bytes transfers in a single transaction
- Multiple addressing modes for source and destination address
  - Increment
  - Decrement
  - Static
- 1, 2, 4, or 8 byte Burst Transfers
- Programmable priority between channels

9.2 Overview

The four-channel direct memory access (DMA) controller can transfer data between memories and peripherals, and thus offload these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention, and frees up CPU time. The four DMA channels enable up to four independent and parallel transfers.

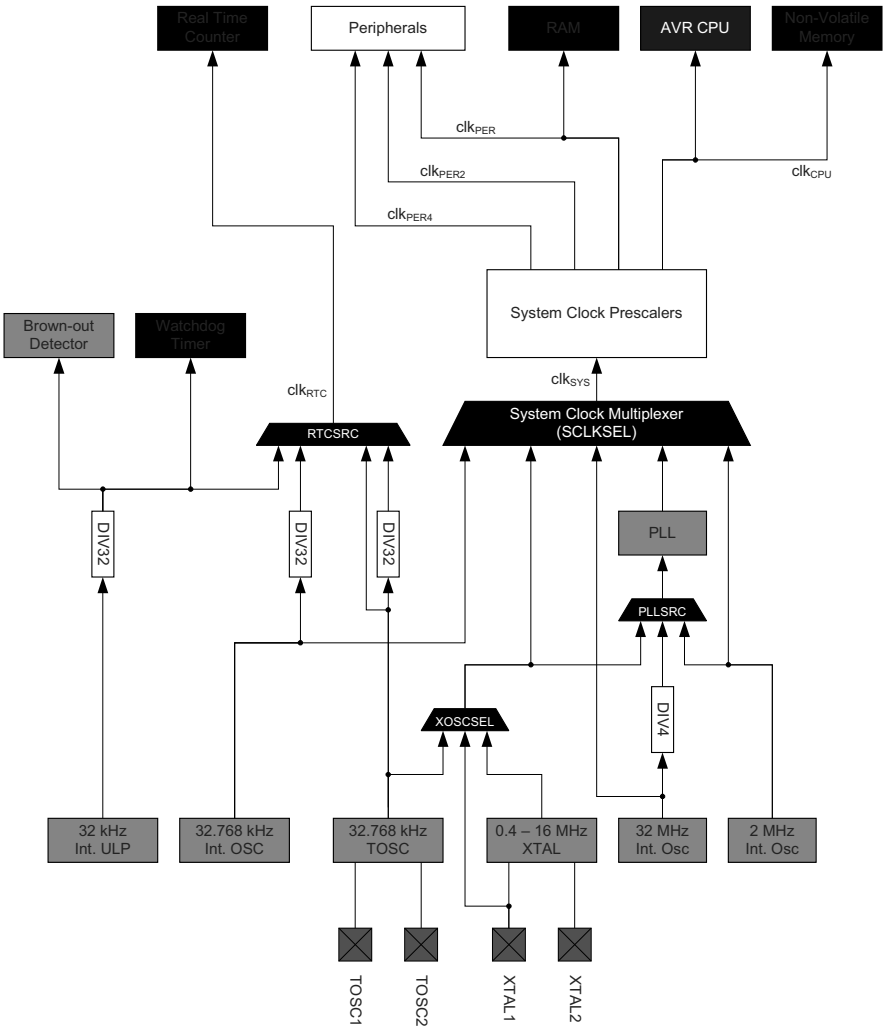
The DMA controller can move data between SRAM and peripherals, between SRAM locations and directly between peripheral registers. With access to all peripherals, the DMA controller can handle automatic transfer of data to/from communication modules. The DMA controller can also read from memory mapped EEPROM.

Data transfers are done in continuous bursts of 1, 2, 4, or 8 bytes. They build block transfers of configurable size from 1 byte to 64KB. A repeat counter can be used to repeat each block transfer for single transactions up to 16MB. Source and destination addressing can be static, incremental or decremental. Automatic reload of source and/or destination addresses can be done after each burst or block transfer, or when a transaction is complete. Application software, peripherals, and events can trigger DMA transfers.

The four DMA channels have individual configuration and control settings. This include source, destination, transfer triggers, and transaction sizes. They have individual interrupt settings. Interrupt requests can be generated when a transaction is complete or when the DMA controller detects an error on a DMA channel.

To allow for continuous transfers, two channels can be interlinked so that the second takes over the transfer when the first is finished, and vice versa.

Figure 11-1. The clock system, clock sources and clock distribution



11.3 Clock Options

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources and PLL are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

11.3.1 32 kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

12. Power Management and Sleep Modes

12.1 Features

- Power management for adjusting power consumption and functions
- 5 sleep modes
  - Idle
  - Power-down
  - Power-save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

12.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

12.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

12.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, event system and DMA controller are kept running. Any enabled interrupt will wake the device.

12.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt and asynchronous port interrupts, e.g pin change.

13.5 WDT - Watchdog Timer

13.5.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

13.6 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

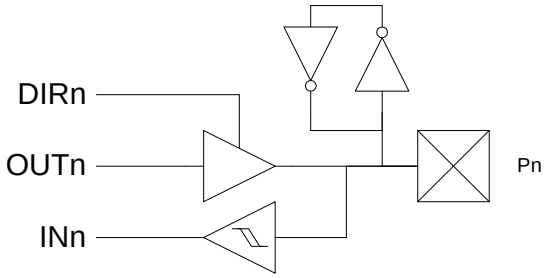
The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

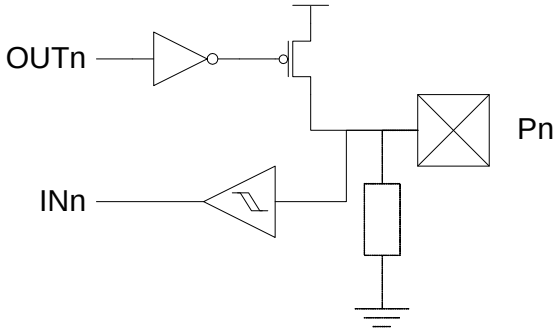
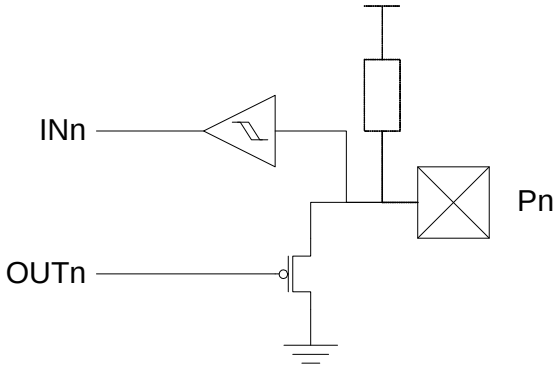


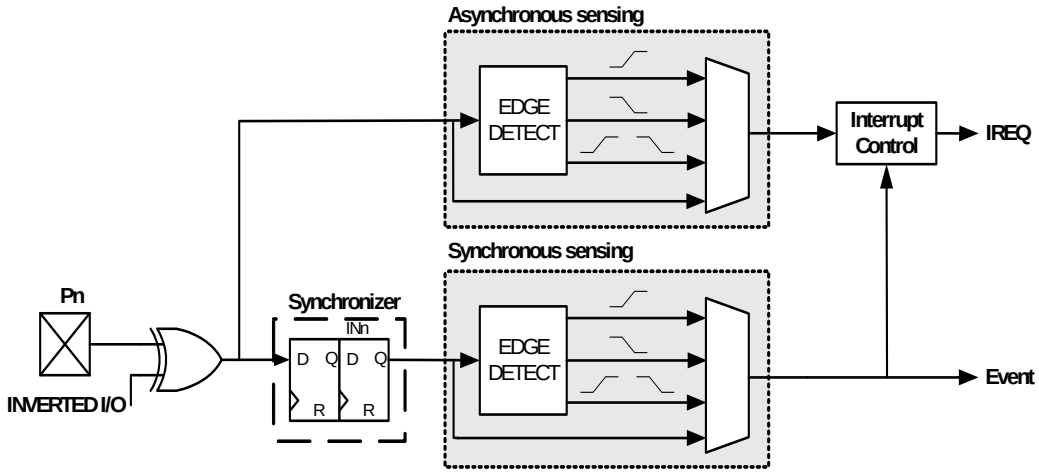
Figure 15-6. I/O configuration - Wired-AND with optional pull-up



15.4 Input sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 15-7 on page 35.

Figure 15-7. Input sensing system overview



When a pin is configured with inverted I/O the pin value is inverted before the input sensing.

15.5 Port Interrupt

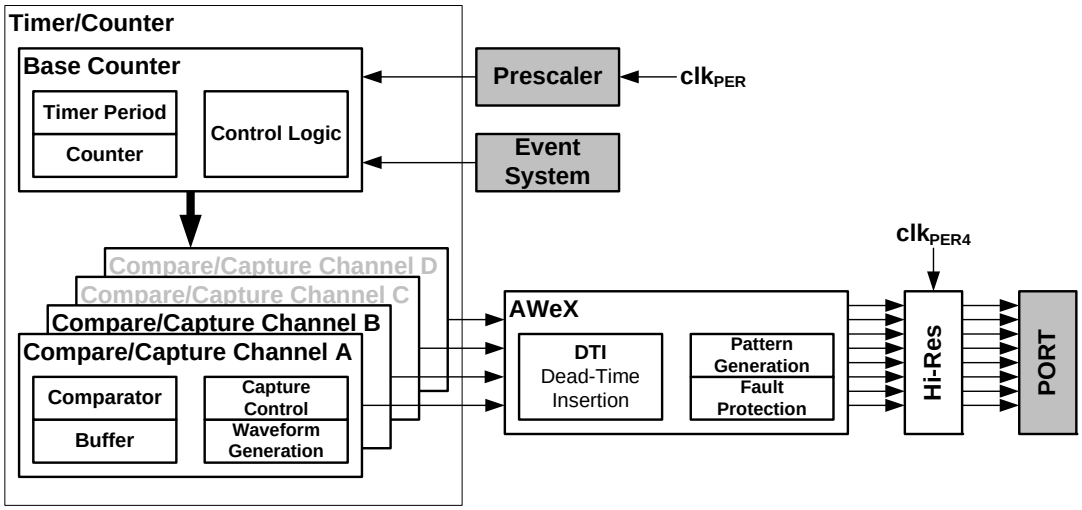
Each ports have two interrupts with seperate priority and interrupt vector. All pins on the port can be individually selected as source for each of the interrupts. The interrupts are then triggered according to the input sense configuration for each pin configured as source for the interrupt.

15.6 Alternate Port Functions

In addition to the input/output functions on all port pins, most pins have alternate functions. This means that other modules or peripherals connected to the port can use the port pins for their functions, such as communication or pulse-width modulation. “Pinout and Pin Functions” on page 55 shows which modules on peripherals that enables alternate functions on a pin, and what alternate functions that is available on a pin.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res - High Resolution Extension” on page 39 for more details.

Figure 16-1. Overview of a Timer/Counter and closely related peripherals



PORTC, PORTD, PORTE and PORTF each has one Timer/Counter 0 and one Timer/Counter1. Notation of these Timer/Counters are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1, TCE0, TCE1, TCF0, and TCF1, respectively.

18. Hi-Res - High Resolution Extension

18.1 Features

- Increases Waveform Generator resolution by 2-bits (4x)
- Supports Frequency, single- and dual-slope PWM operation
- Supports the AWeX when this is enabled and used for the same Timer/Counter

18.2 Overview

TThe high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (ClkPER4). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There are four hi-res extensions that each can be enabled for each timer/counters pair on PORTC, PORTD, PORTE and PORTF. The notation of these peripherals are HIRESC, HIRESD, HIRESE and HIRESF, respectively.

29. Programming and Debugging

29.1 Features

- Programming
  - External programming through PDI or JTAG interfaces
    - Minimal protocol overhead for fast operation
    - Built-in error detection and handling for reliable operation
  - Boot loader support for programming through any communication interface
- Debugging
  - Nonintrusive, real-time, on-chip debug system
  - No software or hardware resources required from device except pin connection
  - Program flow control
    - Go, Stop, Reset, Step Into, Step Over, Step Out, Run-to-Cursor
  - Unlimited number of user program breakpoints
  - Unlimited number of user data breakpoints, break on:
    - Data location read, write, or both read and write
    - Data location content equal or not equal to a value
    - Data location content is greater or smaller than a value
    - Data location content is within or outside a range
  - No limitation on device clock frequency
- Program and Debug Interface (PDI)
  - Two-pin interface for external programming and debugging
  - Uses the Reset pin and a dedicated pin
  - No I/O pins required during programming or debugging
- JTAG interface
  - Four-pin, IEEE Std. 1149.1 compliant interface for programming and debugging
  - Boundary scan capabilities according to IEEE Std. 1149.1 (JTAG)

29.2 Overview

The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of a device.

The PDI supports fast programming of nonvolatile memory (NVM) spaces; flash, EEPOM, fuses, lock bits, and the user signature row.

Debug is supported through an on-chip debug system that offers nonintrusive, real-time debug. It does not require any software or hardware resources except for the device pin connection. Using the Atmel tool chain, it offers complete program flow control and support for an unlimited number of program and complex data breakpoints. Application debug can be done from a C or other high-level language source code level, as well as from an assembler and disassembler level.

Programming and debugging can be done through two physical interfaces. The primary one is the PDI physical layer, which is available on all devices. This is a two-pin interface that uses the Reset pin for the clock input (PDI_CLK) and one other dedicated pin for data input and output (PDI_DATA). A JTAG interface is also available on most devices, and this can be used for programming and debugging through the four-pin JTAG interface. The JTAG interface is IEEE Std. 1149.1 compliant, and supports boundary scan. Any external programmer or on-chip debugger/emulator can be directly connected to either of these interfaces. Unless otherwise stated, all references to the PDI assume access through the PDI physical layer.

30. Pinout and Pin Functions

The pinout of XMEGA A1 is shown in “Pinout/Block Diagram” on page 3. In addition to general I/O functionality, each pin may have several functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at time.

30.1 Alternate Pin Function Description

The tables below shows the notation for all pin functions available and describes its function.

30.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

30.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

30.1.3 Analog functions

ACn	Analog Comparator input pin n
AC0OUT	Analog Comparator 0 Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

30.1.4 EBI functions

An	Address line n	
Dn	Data line n	
$\overline{CSn}$	Chip Select n	
ALEn	Address Latch Enable pin n	(SRAM)
$\overline{RE}$	Read Enable	(SRAM)
$\overline{WE}$	External Data Memory Write	(SRAM /SDRAM)
BAn	Bank Address	(SDRAM)
$\overline{CAS}$	Column Access Strobe	(SDRAM)
CKE	SDRAM Clock Enable	(SDRAM)

CLK	SDRAM Clock	(SDRAM)
$\overline{DQM}$	Data Mask Signal/Output Enable	(SDRAM)
$\overline{RAS}$	Row Access Strobe	(SDRAM)
2P	2 Port Interface	
3P	3 Port Interface	

30.1.5 Timer/Counter and AWEX functions

OCnx	Output Compare Channel x for Timer/Counter n
$\overline{OCnx}$	Inverted Output Compare Channel x for Timer/Counter n
OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

30.1.6 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
$\overline{SS}$	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

30.1.7 Oscillators, Clock and Event

n	Timer Oscillator pin n
XTALn	Input/Output for inverting Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel 0 Output

PORT C	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPIC	TWIC	CLOCKOUT	EVENTOUT
PC3	18	SYNC	OC0D	OC0BHS		TXD0					
PC4	19	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PC5	20	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	21	SYNC		OC0DLS			RXD1	MISO			
PC7	22	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT

Table 30-4. Port D - Alternate functions.

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPID	TWID	CLOCKOUT	EVENTOUT
GND	23									
VCC	24									
PD0	25	SYNC	OC0A					SDA		
PD1	26	SYNC	OC0B		XCK0			SCL		
PD2	27	SYNC/ASYNC	OC0C		RXD0					
PD3	28	SYNC	OC0D		TXD0					
PD4	29	SYNC		OC1A			$\overline{SS}$			
PD5	30	SYNC		OC1B		XCK1	MOSI			
PD6	31	SYNC				RXD1	MISO			
PD7	32	SYNC				TXD1	SCK		CLKOUT	EVOUT

Table 30-5. Port E - Alternate functions.

PORT E	PIN #	INTERRUPT	TCE0	AWEXE	TCE1	USARTE0	USARTE1	SPIE	TWIE	CLOCKOUT	EVENTOUT
GND	33										
VCC	34										
PE0	35	SYNC	OC0A	OC0ALS					SDA		
PE1	36	SYNC	OC0B	OC0AHS		XCK0			SCL		
PE2	37	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PE3	38	SYNC	OC0D	OC0BHS		TXD0					
PE4	39	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PE5	40	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PE6	41	SYNC		OC0DLS			RXD1	MISO			
PE7	42	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT

Table 30-6. Port F - Alternate functions.

PORT F	PIN #	INTERRUPT	TCF0	TCF1	USARTF0	USARTF1	SPIF	TWIF
GND	43							
VCC	44							
PF0	45	SYNC	OC0A					SDA

Base Address	Name	Description
0x04A0	TWIE	Two Wire Interface on port E
0x04B0	TWIF	Two Wire Interface on port F
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x06A0	PORTF	Port F
0x06E0	PORTH	Port H
0x0700	PORTJ	Port J
0x0720	PORTK	Port K
0x07C0	PORTQ	Port Q
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRESC	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0900	TCD0	Timer/Counter 0 on port D
0x0940	TCD1	Timer/Counter 1 on port D
0x0990	HIRESD	High Resolution Extension on port D
0x09A0	USARTD0	USART 0 on port D
0x09B0	USARTD1	USART 1 on port D
0x09C0	SPID	Serial Peripheral Interface on port D
0x0A00	TCE0	Timer/Counter 0 on port E
0x0A40	TCE1	Timer/Counter 1 on port E
0x0A80	AWEXE	Advanced Waveform Extension on port E
0x0A90	HIRESE	High Resolution Extension on port E
0x0AA0	USARTE0	USART 0 on port E
0x0AB0	USARTE1	USART 1 on port E
0x0AC0	SPIE	Serial Peripheral Interface on port E
0x0B00	TCF0	Timer/Counter 0 on port F

32. Instruction Set Summary

Mnemonics	Operands	Description	Operation			Flags	#Clocks
Arithmetic and Logic Instructions							
ADD	Rd, Rr	Add without Carry	Rd	←	Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd	←	Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd	←	Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd	←	Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd	←	Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd	←	Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd	←	Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd	←	Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd	←	Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd	←	Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd	←	Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd	←	Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd	←	Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One’s Complement	Rd	←	$FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two’s Complement	Rd	←	$00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd	←	Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd	←	Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd	←	Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd	←	Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd	←	Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd	←	Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd	←	$FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0	←	Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0	←	Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0	←	Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0	←	Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0	←	Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0	←	Rd x Rr<<1 (SU)	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 else if (H = 1) then R15:R0	← ←	Encrypt(R15:R0, K) Decrypt(R15:R0, K)		1/2
Branch Instructions							
RJMP	k	Relative Jump	PC	←	PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) PC(21:16)	← ←	Z, 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) PC(21:16)	← ←	Z, EIND	None	2
JMP	k	Jump	PC	←	k	None	3

Mnemonics	Operands	Description	Operation			Flags	#Clocks
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) Z	← ←	R1:R0, Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd	←	I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A)	←	Rr	None	1
PUSH	Rr	Push Register on Stack	STACK	←	Rr	None	1(1)
POP	Rd	Pop Register from Stack	Rd	←	STACK	None	2(1)
Bit and Bit-test Instructions							
LSL	Rd	Logical Shift Left	Rd(n+1) Rd(0) C	← ← ←	Rd(n), 0, Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) Rd(7) C	← ← ←	Rd(n+1), 0, Rd(0)	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) Rd(n+1) C	← ← ←	C, Rd(n), Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) Rd(n) C	← ← ←	C, Rd(n+1), Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n)	←	Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)	↔	Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s)	←	1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s)	←	0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b)	←	1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b)	←	0	None	1
BST	Rr, b	Bit Store from Register to T	T	←	Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b)	←	T	None	1
SEC		Set Carry	C	←	1	C	1
CLC		Clear Carry	C	←	0	C	1
SEN		Set Negative Flag	N	←	1	N	1
CLN		Clear Negative Flag	N	←	0	N	1
SEZ		Set Zero Flag	Z	←	1	Z	1
CLZ		Clear Zero Flag	Z	←	0	Z	1
SEI		Global Interrupt Enable	I	←	1	I	1
CLI		Global Interrupt Disable	I	←	0	I	1
SES		Set Signed Test Flag	S	←	1	S	1
CLS		Clear Signed Test Flag	S	←	0	S	1
SEV		Set Two's Complement Overflow	V	←	1	V	1
CLV		Clear Two's Complement Overflow	V	←	0	V	1
SET		Set T in SREG	T	←	1	T	1
CLT		Clear T in SREG	T	←	0	T	1
SEH		Set Half Carry Flag in SREG	H	←	1	H	1
CLH		Clear Half Carry Flag in SREG	H	←	0	H	1

34. Electrical Characteristics

34.1 Absolute Maximum Ratings*

Operating Temperature . . . . . -55°C to +125°C

Storage Temperature . . . . . -65°C to +150°C

Voltage on any Pin with respect to Ground-0.5V to V_{CC}+0.5V

Maximum Operating Voltage 3.6V

DC Current per I/O Pin. . . . . 20.0 mA

DC Current V_{CC} and GND Pins. . . . . 200.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

34.2 DC Characteristics

Table 34-1. Current consumption.

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC}	Active mode(1)	1 MHz, Ext. Clk	V_{CC} = 1.8V		365		µA
			V_{CC} = 3.0V		790		
		2 MHz, Ext. Clk	V_{CC} = 1.8V		690	800	
			V_{CC} = 3.0V		1400	1600	
		32 MHz, Ext. Clk	V_{CC} = 3.0V		18.35	20	mA
	Idle mode(1)	1 MHz, Ext. Clk	V_{CC} = 1.8V		135		µA
			V_{CC} = 3.0V		255		
		2 MHz, Ext. Clk	V_{CC} = 1.8V		270	380	
			V_{CC} = 3.0V		510	650	
		32 MHz, Ext. Clk	V_{CC} = 3.0V		8.15	9.2	mA
	Power-down mode	All Functions Disabled	V_{CC} = 3.0V		0.1		µA
		All Functions Disabled, T = 85°C	V_{CC} = 3.0V		2	5	
		ULP, WDT, Sampled BOD	V_{CC} = 1.8V		0.5		
			V_{CC} = 3.0V		0.6		
		ULP, WDT, Sampled BOD, T=85°C	V_{CC} = 3.0V		3	10	
	Power-save mode	RTC 1 kHz from Low Power 32 kHz	V_{CC} = 1.8V		0.52		µA
			V_{CC} = 3.0V		0.55		
		RTC from Low Power 32 kHz	V_{CC} = 3.0V		1.16		

35.11 PDI Speed

Figure 35-27.PDI Speed vs. V_{CC}