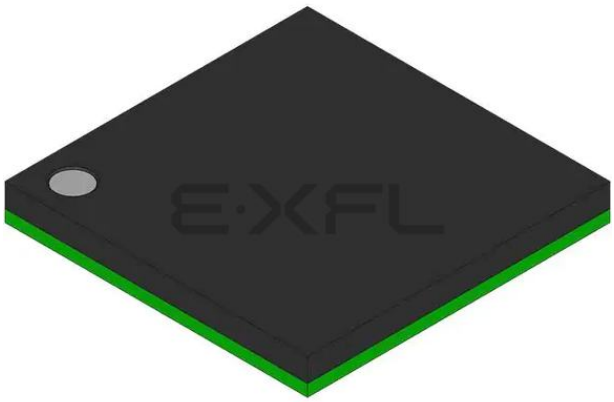

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atxmega128a1-c7u

4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended reading

- XMEGA A Manual
- XMEGA A Application Notes

This device data sheet only contains part specific information and a short description of each peripheral and module. The XMEGA A Manual describes the modules and peripherals in depth. The XMEGA A application notes contain example code and show applied use of the modules and peripherals.

The XMEGA A Manual and Application Notes are available from http://www.atmel.com/avr.

5. Capacitive touch sensing

The Atmel QTouch library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and QMatrix acquisition methods.

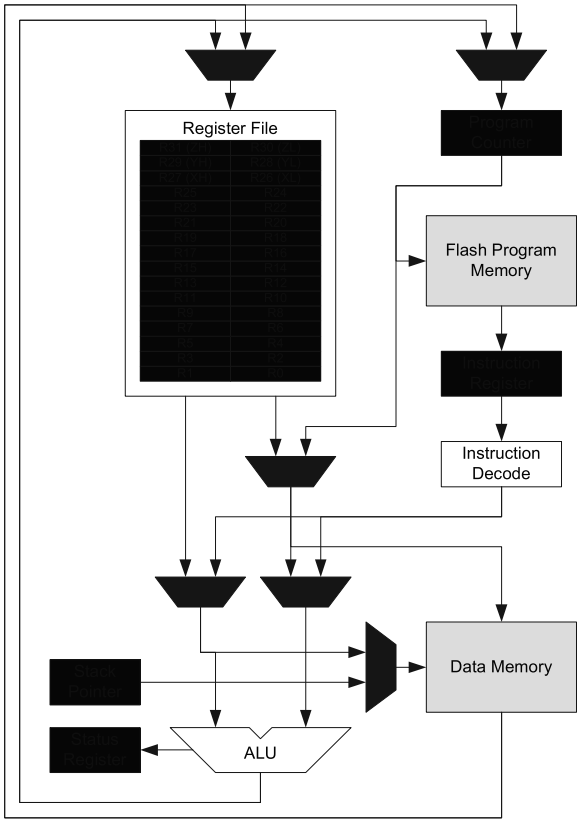
Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the QTouch library user guide - also available for download from the Atmel website.

6. Disclaimer

For devices that are not available yet, typical values contained in this datasheet are based on simulations and characterization of other AVR XMEGA microcontrollers manufactured on the same process technology. Min. and Max values will be available after the device is characterized.

Figure 7-1. Block diagram of the AVR CPU architecture.



The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers, SRAM, and external RAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for safe storing of nonvolatile data in the program memory.

The available memory size configurations are shown in “Ordering Information” on page 2. In addition each device has a flash memory signature rows for calibration data, device identification, serial number etc.

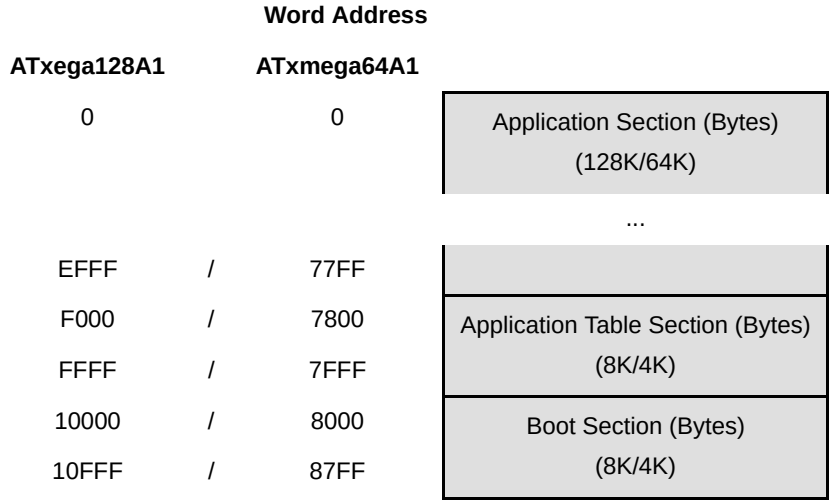
8.3 In-System Programmable Flash Program Memory

he Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 8-1. Flash Program Memory (Hexadecimal address)



8.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

8.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

8.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

8.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 76.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 8-1.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 8-1. Device ID bytes.

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega64A1	4E	96	1E
ATxmega128A1	4C	97	1E

8.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

8.4 Fuses and Lock bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, JTAG enable, and JTAG user ID.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

8.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 8-2 on page 15. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices. The address space for External Memory will always start at the end of Internal SRAM and end at address 0xFFFFFF.

11. System Clock and Clock options

11.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal Oscillators:
  - 32 MHz run-time calibrated RC oscillator
  - 2 MHz run-time calibrated RC oscillator
  - 32.768 kHz calibrated RC oscillator
  - 32 kHz Ultra Low Power (ULP) oscillator with 1 kHz ouput
- External clock options
  - 0.4 - 16 MHz Crystal Oscillator
  - 32 kHz Crystal Oscillator
  - External clock
- PLL with internal and external clock options with 1 to 31x multiplication
- Clock Prescalers with 1x to 2048x division
- Fast peripheral clock running at two and four times the CPU clock speed
- Automatic Run-Time Calibration of internal oscillators
- Crystal Oscillator failure detection

11.2 Overview

Atmel AVR XMEGA devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 11-1 on page 22 presents the principal clock system in the XMEGA A1U family devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers as described in “Power Management and Sleep Modes” on page 24.

13. System Control and Reset

13.1 Features

- Multiple reset sources for safe operation and device reset
  - Power-On Reset
  - External Reset
  - Watchdog Reset
  - Brown-Out Reset
  - PDI reset
  - Software reset
- Asynchronous reset
  - No running clock in the device is required for reset
- Reset status register

13.2 Overview

The reset system issues a microcontroller reset and sets the device to its initial state. This is for situations where operation should not start or continue, such as when the microcontroller operates below its power supply rating. If a reset source goes active, the device enters and is kept in reset until all reset sources have released their reset. The I/O pins are immediately tri-stated. The program counter is set to the reset vector location, and all I/O registers are set to their initial values. The SRAM content is kept. However, if the device accesses the SRAM when a reset occurs, the content of the accessed location can not be guaranteed.

After reset is released from all reset sources, the default oscillator is started and calibrated before the device starts running from the reset vector address. By default, this is the lowest program memory address, 0, but it is possible to move the reset vector to the lowest address in the boot section.

The reset functionality is asynchronous, and so no running system clock is required to reset the device. The software reset feature makes it possible to issue a controlled system reset from the user software.

The reset status register has individual status flags for each reset source. It is cleared at power-on reset, and shows which sources have issued a reset since the last power-on.

13.3 Reset Sequence

A reset request from any reset source will immediately reset the device and keep it in reset as long as the request is active. When all reset requests are released, the device will go through three stages before the device starts running again:

- Reset counter delay
- Oscillator startup
- Oscillator calibration

If another reset requests occurs during this process, the reset sequence will start over again.

13.4 Reset Sources

13.4.1 Power-On Reset

TA power-on reset (POR) is generated by an on-chip detection circuit. The POR is activated when the V_{CC} rises and reaches the POR threshold voltage (V_{POT}), and this will start the reset sequence.

The POR is also activated to power down the device properly when the V_{CC} falls and drops below the V_{POT} level.

The V_{POT} level is higher for falling V_{CC} than for rising V_{CC}. Consult the datasheet for POR characteristics data.

13.5 WDT - Watchdog Timer

13.5.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

13.6 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

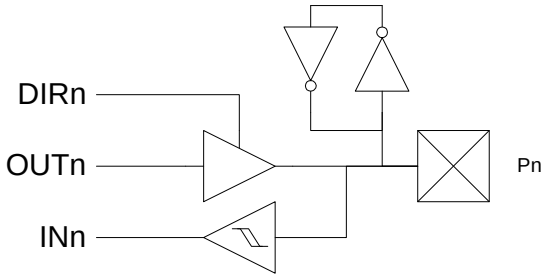
The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

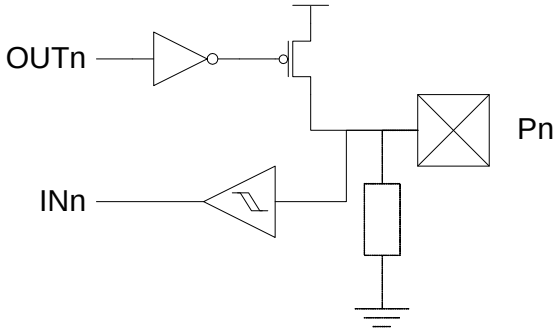
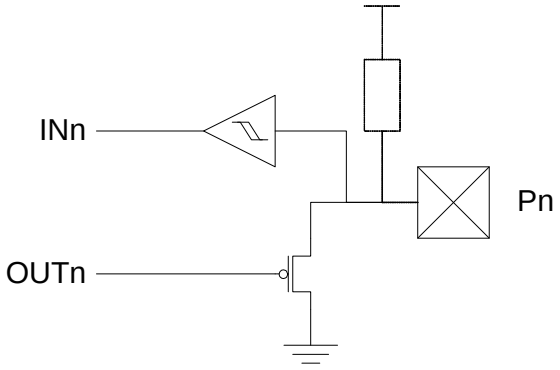


Figure 15-6. I/O configuration - Wired-AND with optional pull-up



21. SPI - Serial Peripheral Interface

21.1 Features

- Four identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

21.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC, PORTD, PORTE, and PORTF each has one SPI. Notation of these peripherals are SPIC, SPID, SPIE, and SPIF.

23. IRCOM - IR Communication Module

23.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
  - 3/16 of the baud rate period
  - Fixed pulse period, 8-bit programmable
  - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

23.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

32. Instruction Set Summary

Mnemonics	Operands	Description	Operation			Flags	#Clocks
Arithmetic and Logic Instructions							
ADD	Rd, Rr	Add without Carry	Rd	←	Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd	←	Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd	←	Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd	←	Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd	←	Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd	←	Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd	←	Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd	←	Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd	←	Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd	←	Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd	←	Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd	←	Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd	←	Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One’s Complement	Rd	←	$FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two’s Complement	Rd	←	$00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd	←	Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd	←	Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd	←	Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd	←	Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd	←	Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd	←	Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd	←	$FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0	←	Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0	←	Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0	←	Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0	←	Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0	←	Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0	←	Rd x Rr<<1 (SU)	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 else if (H = 1) then R15:R0	← ←	Encrypt(R15:R0, K) Decrypt(R15:R0, K)		1/2
Branch Instructions							
RJMP	k	Relative Jump	PC	←	PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) PC(21:16)	← ←	Z, 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) PC(21:16)	← ←	Z, EIND	None	2
JMP	k	Jump	PC	←	k	None	3

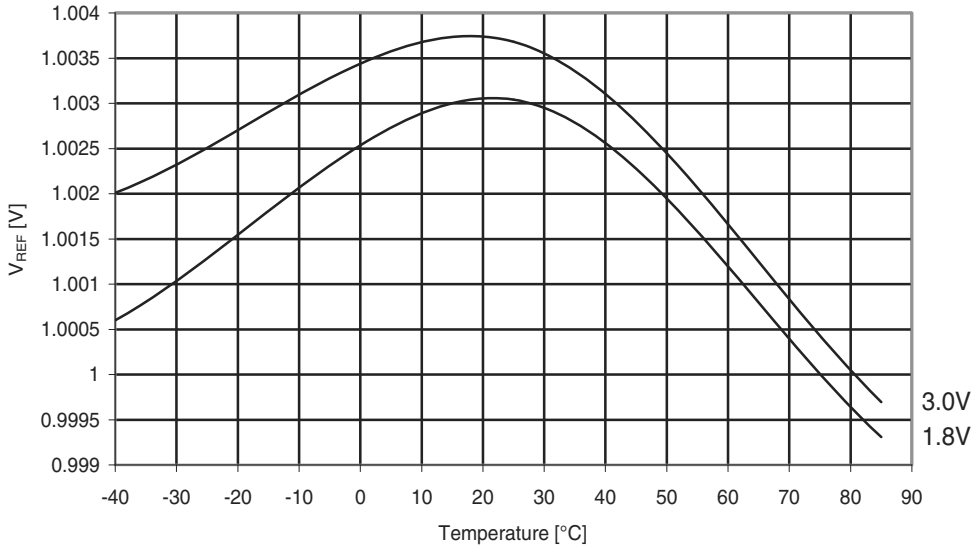
Symbol	Parameter	Condition	Min	Typ	Max	Units
	Conversion rate	V_{CC}≥2.0V			2000	ksps
		V_{CC}<2.0V			500	
	Conversion time (propagation delay)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0 or 1	5	7	8	ADC_{clk} cycles
	Sampling Time	1/2 ADC_{clk} cycle	0.25			µS
	Conversion range		0		VREF	V
AVCC	Analog Supply Voltage		V_{cc}-0.3		V_{cc}+0.3	V
VREF	Reference voltage		1.0		V_{cc}-0.6	V
	Input bandwidth	V_{CC}≥2.0V			2000	kHz
		V_{CC}<2.0V			500	
INT1V	Internal 1.00V reference			1.00		V
INTVCC	Internal V_{CC}/1.6			V_{CC}/1.6		V
SCALEDVCC	Scaled internal V_{CC}/10 input			V_{CC}/10		V
R_{AREF}	Reference input resistance			>10		MΩ
	Start-up time			12	24	ADC_{clk} cycles
	Internal input sampling speed	Temp. sensor, V_{CC}/10, Bandgap			100	ksps

Table 34-6. ADC gain stage characteristics.

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Gain error	1 to 64 gain			< ±1		%
	Offset error				< ±1		mV
Vrms	Noise level at input	64x gain	VREF = Int. 1V		0.12		mV
			VREF = Ext. 2V		0.06		
	Clock rate	Same as ADC				1000	kHz

35.8 Bandgap

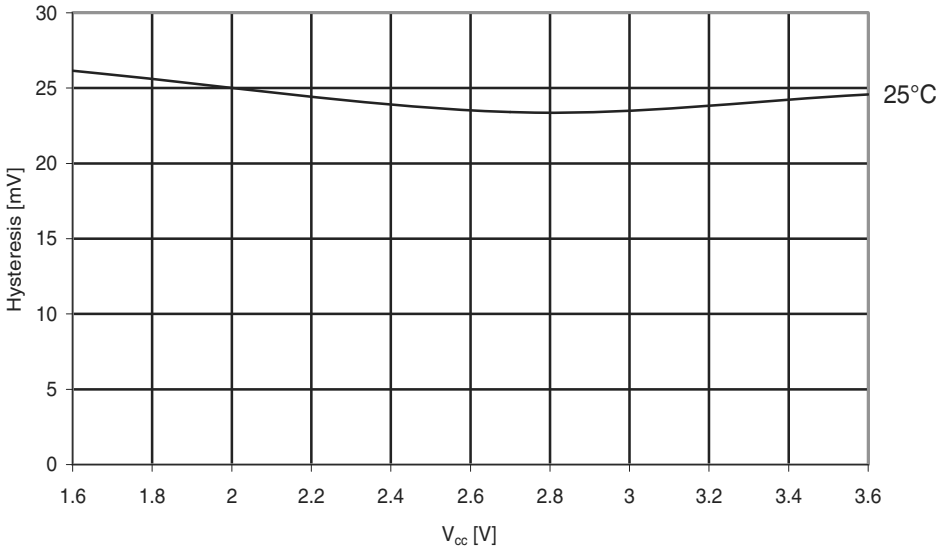
Figure 35-17.Internal 1.00V Reference vs. Temperature.



35.9 Analog Comparator

Figure 35-18.Analog Comparator Hysteresis vs. V_{CC}

High-speed, Small hysteresis



35.10 Oscillators and Wake-up Time

Figure 35-21.Internal 32.768 kHz Oscillator Frequency vs. Temperature

1.024 kHz output

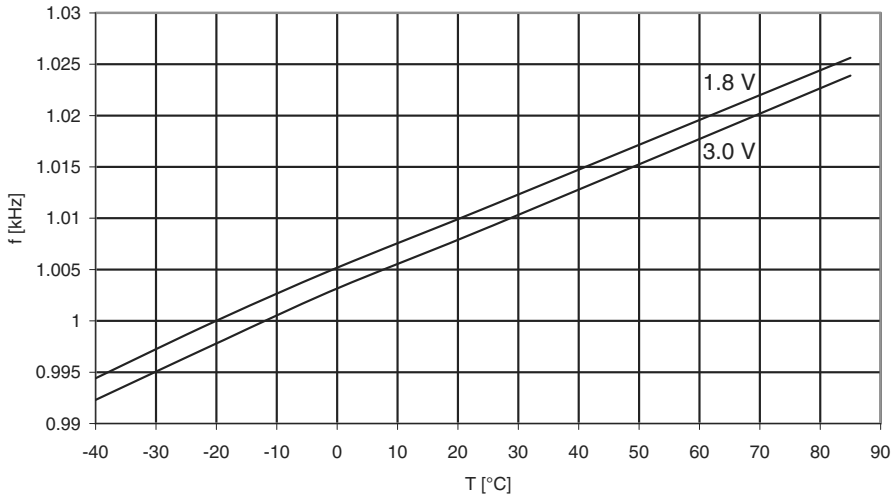
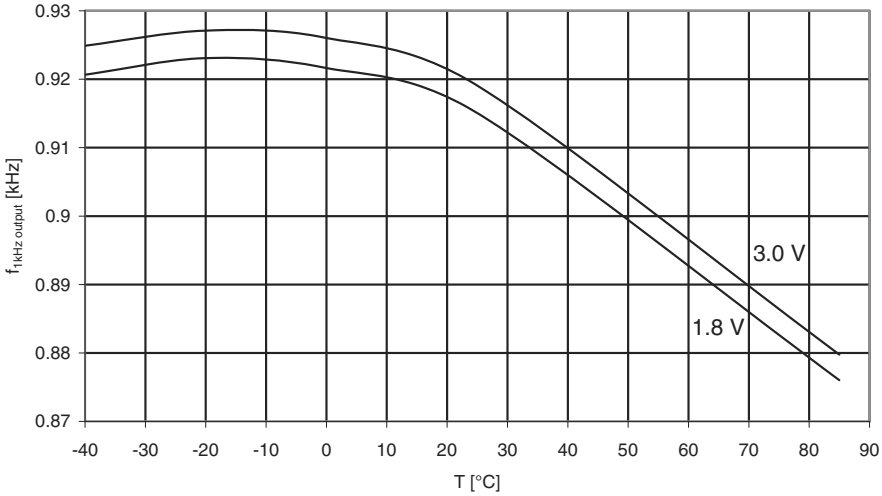


Figure 35-22.Ultra Low-Power (ULP) Oscillator Frequency vs. Temperature

1 kHz output



18. DAC has up to ±10 LSB noise in Sampled Mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

19. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto trigged conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion internal never is shorter than 1.5 µs.

20. Both DFLLs and both oscillators have to be enabled for one to work

In order to use the automatic runtime calibration for the 2 MHz or the 32 MHz internal oscillators, the DFLL for both oscillators and both oscillators have to be enabled for one to work.

Problem fix/Workaround

Enable both DFLLs and both oscillators when using automatic runtime calibration for either of the internal oscillators.

21. Access error when multiple bus masters are accessing SDRAM

If one bus master (CPU and DMA channels) is using the EBI to access an SDRAM in burst mode and another bus master is accessing the same row number in a different BANK of the SDRAM in the cycle directly after the burst access is complete, the access for the second bus master will fail.

Problem fix/Workaround

Do not put stack pointer in SDRAM and use DMA Controller in 1 byte burst mode if CPU and DMA Controller are required to access SDRAM at the same time.

22. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

23. Pending full asynchronous pin change interrupts will not wake the device

Problem fix/Workaround

Disable Flash Power Reduction mode before entering sleep mode.

29. Some NVM Commands are non-functional

The following NVM commands are non-functional:

- 0x2B Erase Flash Page
- 0x2E Write Flash Page
- 0x2F Erase & Write Flash Page
- 0x3A Flash Range CRC

Problem fix/Workaround

None for Flash Range CRC

Use separate programming commands for accessing application and boot section.

- 0x22 Erase Application Section Page
- 0x24 Write Application Section Page
- 0x25 Erase & Write Application Section Page
- 0x2A Erase Boot Loader Section Page
- 0x2C Write Boot Loader Section Page
- 0x2D Erase & Write Boot Loader Section Page

30. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768 kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA A Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

31. Setting PRHIRES bit makes PWM output unavailable

Setting the HIRES Power Reduction (PR) bit for PORTx will make any Frequency or PWM output for the corresponding Timer/Counters (TCx0 and TCx1) unavailable on the pin even if the Hi-Res is not used.

Problem fix/Workaround

Do not write the HIRES PR bit on PORTx when frequency or PWM output from TCx0/1 is used.

40. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

41. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

42. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

7. TWI, the minimum I^2C SCL low time could be violated in Master Read mode

When the TWI is in Master Read mode and issuing a Repeated Start on the bus, this will immediately release the SCL line even if one complete SCL low period has not passed. This means that the minimum SCL low time in the I^2C specification could be violated.

Problem fix/Workaround

If this causes a potential problem in the application, software must ensure that the Repeated Start is never issued before one SCL low time has passed.

8. Setting HIRES PR bit makes PWM output unavailable

Setting the HIRES Power Reduction (PR) bit for PORTx will make any Frequency or PWM output for the corresponding Timer/Counters (TCx0 and TCx1) unavailable on the pin.

Problem fix/Workaround

Do not write the HIRES PR bit on PORTx when frequency or PWM output from TCx0/1 is used.

9. EEPROM erase and write does not work with all System Clock sources

When doing EEPROM erase or Write operations with other clock sources than the 2 MHz RCOSC, Flash will be read wrongly for one or two clock cycles at the end of the EEPROM operation.

Problem fix/Workaround

Alt 1: Use the internal 2 MHz RCOSC when doing erase or write operations on EEPROM.

Alt 2: Ensure to be in sleep mode while completing erase or write on EEPROM. After starting erase or write operations on EEPROM, other interrupts should be disabled and the device put to sleep.

10. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

11. Propagation delay analog Comparator increasing to 2 ms at -40 °C

When the analog comparator is used at temperatures reaching down to -40 °C, the propagation delay will increase to ~2 ms.

Problem fix/Workaround

None