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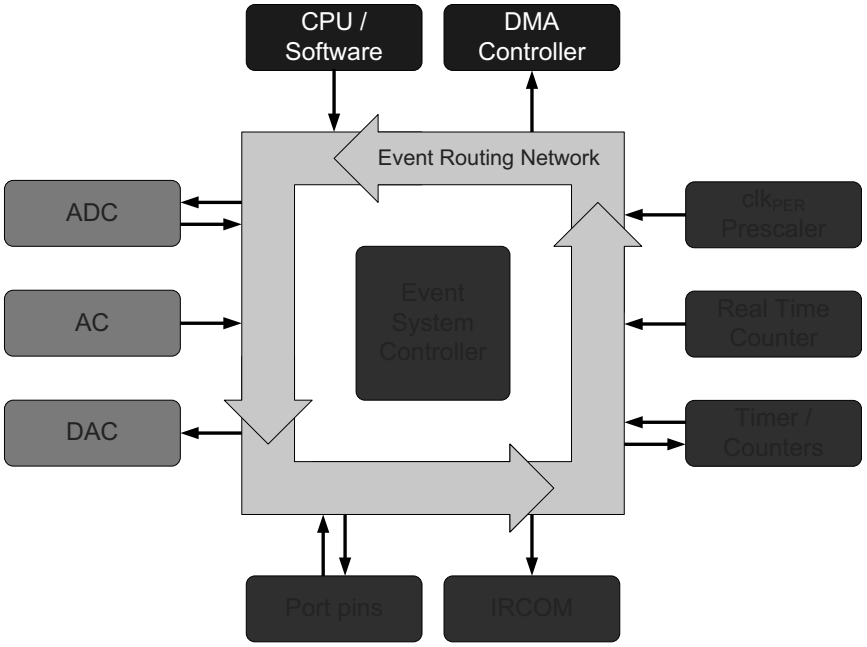
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

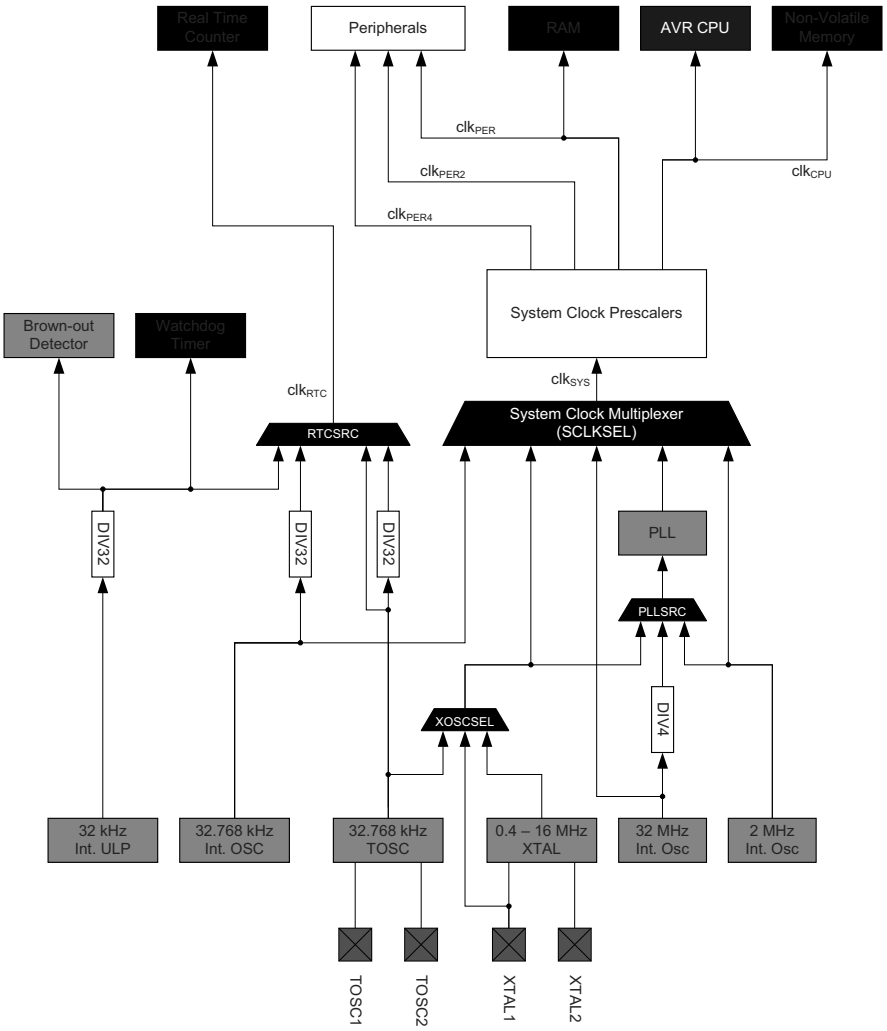
Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-CBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128a1-cur

Figure 10-1. Event system block diagram.



he event routing network consists of eight software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to eight parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

Figure 11-1. The clock system, clock sources and clock distribution



11.3 Clock Options

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources and PLL are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

11.3.1 32 kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

13.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

13.4.3 External Reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the RESET pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, V_{RST}, for longer than the minimum pulse period, t_{EXT}. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

13.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details see “WDT - Watchdog Timer” on page 28.

13.4.5 Software reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register.The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

13.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

14. Interrupts and Programmable Multilevel Interrupt Controller

14.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

14.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

14.3 Interrupt vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA A1U devices are shown in Table 14-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA AU manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 14-1. The program address is the word address.

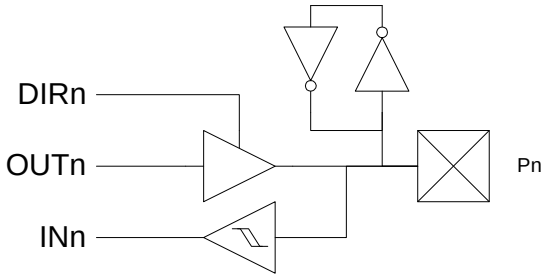
Table 14-1. Reset and Interrupt vectors

Program Address (Base Address)	Source	Interrupt Description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	PORTC_INT_base	Port C Interrupt base
0x008	PORTR_INT_base	Port R Interrupt base
0x00C	DMA_INT_base	DMA Controller Interrupt base
0x014	RTC_INT_base	Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base

15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

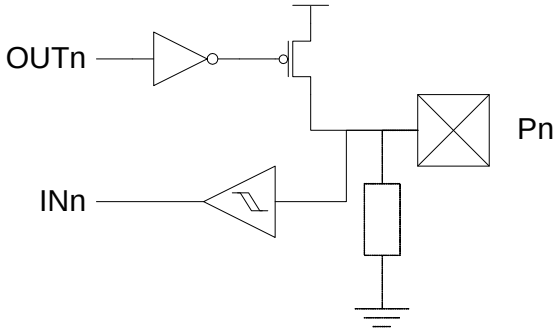
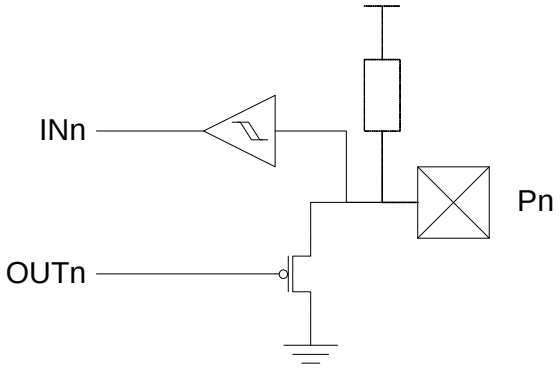


Figure 15-6. I/O configuration - Wired-AND with optional pull-up



17. AWeX - Advanced Waveform Extension

17.1 Features

- Output with complementary output from each Capture channel
- Four Dead Time Insertion (DTI) Units, one for each Capture channel
- 8-bit DTI Resolution
- Separate High and Low Side Dead-Time Setting
- Double Buffered Dead-Time
- Event Controlled Fault Protection
- Single Channel Multiple Output Operation (for BLDC motor control)
- Double Buffered Pattern Generation

17.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

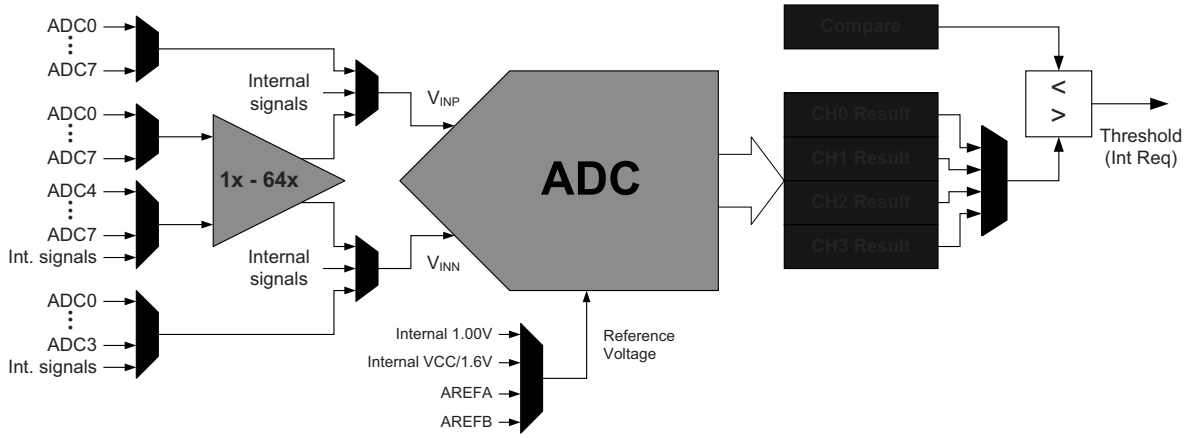
Each of the waveform generator outputs from the Timer/Counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives great flexibility in the selection of fault triggers.

The AWeX is available for TCC0 and TCE0. The notation of these are AWEXC and AWEXE.

Figure 26-1. ADC overview



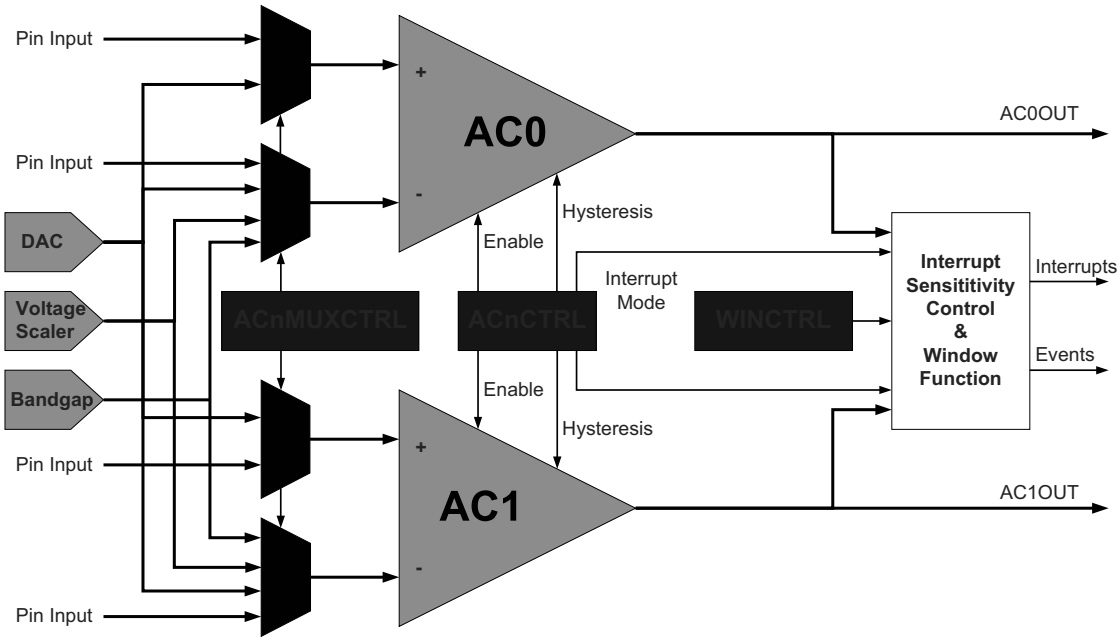
Each ADC has four MUX selection registers with a corresponding result register. This means that four channels can be sampled within 1.5 µs without any intervention by the application other than starting the conversion. The results will be available in the result registers.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5 µs for 12-bit to 2.5 µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

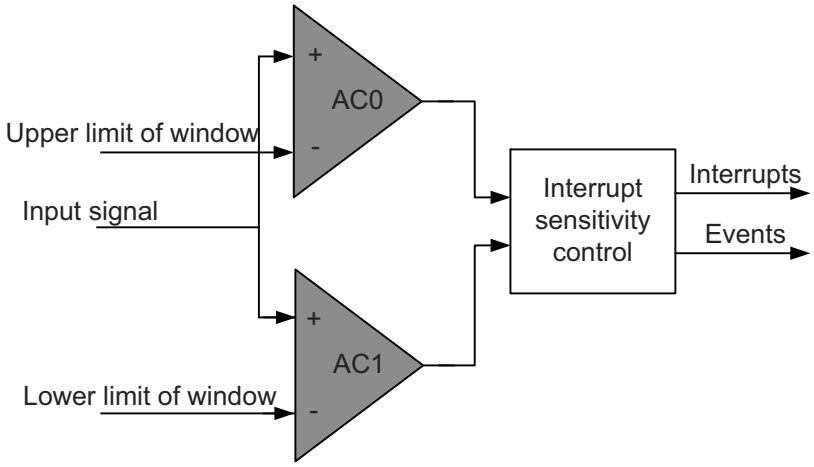
PORTA and PORTB each has one ADC. Notation of these peripherals are ADCA and ADCB, respectively.

Figure 28-1. Analog comparator overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 28-2.

Figure 28-2. Analog comparator window function



30. Pinout and Pin Functions

The pinout of XMEGA A1 is shown in “Pinout/Block Diagram” on page 3. In addition to general I/O functionality, each pin may have several functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at time.

30.1 Alternate Pin Function Description

The tables below shows the notation for all pin functions available and describes its function.

30.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

30.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

30.1.3 Analog functions

ACn	Analog Comparator input pin n
AC0OUT	Analog Comparator 0 Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

30.1.4 EBI functions

An	Address line n	
Dn	Data line n	
$\overline{CSn}$	Chip Select n	
ALEn	Address Latch Enable pin n	(SRAM)
$\overline{RE}$	Read Enable	(SRAM)
$\overline{WE}$	External Data Memory Write	(SRAM /SDRAM)
BAn	Bank Address	(SDRAM)
$\overline{CAS}$	Column Access Strobe	(SDRAM)
CKE	SDRAM Clock Enable	(SDRAM)

PORT C	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPIC	TWIC	CLOCKOUT	EVENTOUT
PC3	18	SYNC	OC0D	OC0BHS		TXD0					
PC4	19	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PC5	20	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	21	SYNC		OC0DLS			RXD1	MISO			
PC7	22	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT

Table 30-4. Port D - Alternate functions.

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPID	TWID	CLOCKOUT	EVENTOUT
GND	23									
VCC	24									
PD0	25	SYNC	OC0A					SDA		
PD1	26	SYNC	OC0B		XCK0			SCL		
PD2	27	SYNC/ASYNC	OC0C		RXD0					
PD3	28	SYNC	OC0D		TXD0					
PD4	29	SYNC		OC1A			$\overline{SS}$			
PD5	30	SYNC		OC1B		XCK1	MOSI			
PD6	31	SYNC				RXD1	MISO			
PD7	32	SYNC				TXD1	SCK		CLKOUT	EVOUT

Table 30-5. Port E - Alternate functions.

PORT E	PIN #	INTERRUPT	TCE0	AWEXE	TCE1	USARTE0	USARTE1	SPIE	TWIE	CLOCKOUT	EVENTOUT
GND	33										
VCC	34										
PE0	35	SYNC	OC0A	OC0ALS					SDA		
PE1	36	SYNC	OC0B	OC0AHS		XCK0			SCL		
PE2	37	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PE3	38	SYNC	OC0D	OC0BHS		TXD0					
PE4	39	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PE5	40	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PE6	41	SYNC		OC0DLS			RXD1	MISO			
PE7	42	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT

Table 30-6. Port F - Alternate functions.

PORT F	PIN #	INTERRUPT	TCF0	TCF1	USARTF0	USARTF1	SPIF	TWIF
GND	43							
VCC	44							
PF0	45	SYNC	OC0A					SDA

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Conversion rate	V_{CC}≥2.0V			2000	ksps
		V_{CC}<2.0V			500	
	Conversion time (propagation delay)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0 or 1	5	7	8	ADC_{clk} cycles
	Sampling Time	1/2 ADC_{clk} cycle	0.25			µS
	Conversion range		0		VREF	V
AVCC	Analog Supply Voltage		V_{cc}-0.3		V_{cc}+0.3	V
VREF	Reference voltage		1.0		V_{cc}-0.6	V
	Input bandwidth	V_{CC}≥2.0V			2000	kHz
		V_{CC}<2.0V			500	
INT1V	Internal 1.00V reference			1.00		V
INTVCC	Internal V_{CC}/1.6			V_{CC}/1.6		V
SCALEDVCC	Scaled internal V_{CC}/10 input			V_{CC}/10		V
R_{AREF}	Reference input resistance			>10		MΩ
	Start-up time			12	24	ADC_{clk} cycles
	Internal input sampling speed	Temp. sensor, V_{CC}/10, Bandgap			100	ksps

Table 34-6. ADC gain stage characteristics.

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Gain error	1 to 64 gain			< ±1		%
	Offset error				< ±1		mV
Vrms	Noise level at input	64x gain	VREF = Int. 1V		0.12		mV
			VREF = Ext. 2V		0.06		
	Clock rate	Same as ADC				1000	kHz

Figure 35-11.I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} - I/O Pin Read as "0"

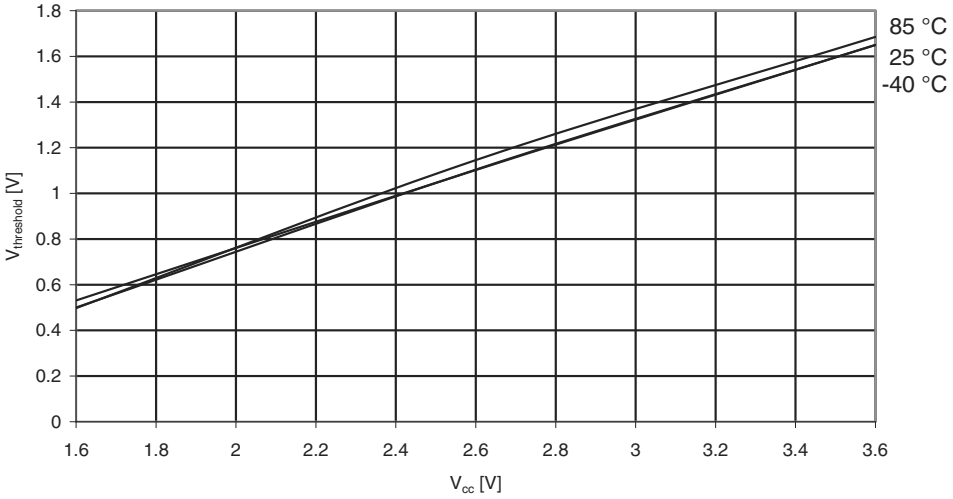


Figure 35-12.I/O Pin Input Hysteresis vs. V_{CC}.

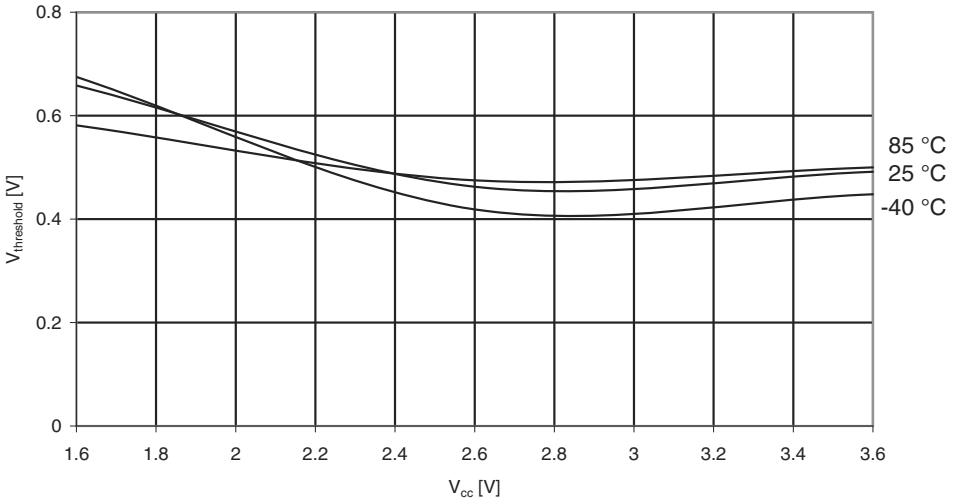


Figure 35-19.Analog Comparator Hysteresis vs. V_{CC}, High-speed

Large hysteresis

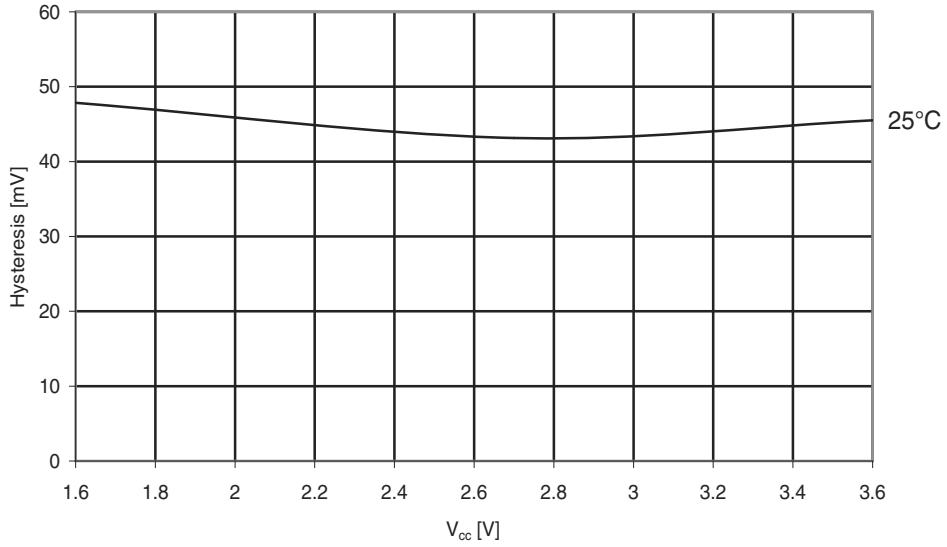
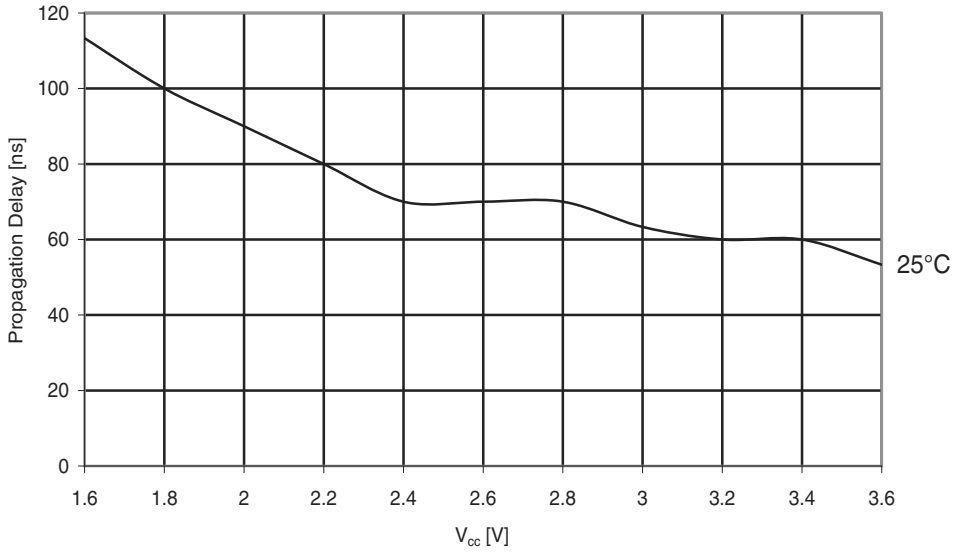


Figure 35-20.Analog Comparator Propagation Delay vs. V_{CC}

High-speed



36. Errata

36.1 ATxmega64A1and ATxmega128A1 rev. H

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- VCC voltage scaler for AC is non-linear
- The ADC has up to ±2 LSB inaccuracy
- ADC gain stage output range is limited to 2.4 V
- Sampling speed limited to 500 ksps for supply voltage below 2.0V
- ADC Event on compare match non-functional
- Bandgap measurement with the ADC is non-functional when VCC is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- The input difference between two succeeding ADC samples is limited by VREF
- Increased noise when using internal 1.0V reference at low temperature
- Configuration of PGM and CWCM not as described in XMEGA A Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- BODACT fuse location is not correct
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- DAC has up to ±10 LSB noise in Sampled Mode
- DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V
- DAC refresh may be blocked in S/H mode
- Conversion lost on DAC channel B in event triggered mode
- Both DFLLs and both oscillators have to be enabled for one to work
- Access error when multiple bus masters are accessing SDRAM
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- Low level interrupt triggered when pin input is disabled
- JTAG enable does not override Analog Comparator B output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Flash Power Reduction Mode can not be enabled when entering sleep
- Some NVM Commands are non-functional
- Crystal start-up time required after power-save even if crystal is source for RTC
- Setting PRHIRES bit makes PWM output unavailable
- Accessing EBI address space with PREBI set will lock Bus Master
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI, the minimum I2C SCL low time could be violated in Master Read mode
- TWI address-mask feature is non-functional
- TWI, a general address call will match independent of the R/W-bit value
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus

18. DAC has up to ±10 LSB noise in Sampled Mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

19. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto trigged conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion internal never is shorter than 1.5 µs.

20. Both DFLLs and both oscillators have to be enabled for one to work

In order to use the automatic runtime calibration for the 2 MHz or the 32 MHz internal oscillators, the DFLL for both oscillators and both oscillators have to be enabled for one to work.

Problem fix/Workaround

Enable both DFLLs and both oscillators when using automatic runtime calibration for either of the internal oscillators.

21. Access error when multiple bus masters are accessing SDRAM

If one bus master (CPU and DMA channels) is using the EBI to access an SDRAM in burst mode and another bus master is accessing the same row number in a different BANK of the SDRAM in the cycle directly after the burst access is complete, the access for the second bus master will fail.

Problem fix/Workaround

Do not put stack pointer in SDRAM and use DMA Controller in 1 byte burst mode if CPU and DMA Controller are required to access SDRAM at the same time.

22. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

23. Pending full asynchronous pin change interrupts will not wake the device

32. Accessing EBI address space with PREBI set will lock Bus Master

If EBI Power Reduction Bit is set while EBI is enabled, accessing external memory could result in bus hang-up, blocking all further access to all data memory.

Problem fix/Workaround

Ensure that EBI is disabled before setting EBI Power Reduction bit.

33. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

34. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

35. TWI, the minimum I^2C SCL low time could be violated in Master Read mode

If the TWI is in Master Read mode and issues a Repeated Start on the bus, this will immediately release the SCL line even if one complete SCL low period has not passed. This means that the minimum SCL low time in the I2C specification could be violated.

Problem fix/Workaround

If this is a problem in the application, ensure in software that the Repeated Start is never issued before one SCL low time has passed.

36. TWI address-mask feature is non-functional

The address-mask feature is non-functional, so the TWI can not perform hardware address match on more than one address.

Problem fix/Workaround

If the TWI must respond to multiple addresses, enable Promiscuous Mode for the TWI to respond to all address and implement the address-mask function in software.

17. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workarund

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

18. Inverted I/O enable does not affect Analog Comparator Output

The inverted I/O pin function does not affect the Analog Comparator output function.

Problem fix/Workarund

Configure the analog comparator setup to give a inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and externel inverter to change polarity of Analog Comparator Output.

19. Both DFLLs and both oscillators has to be enabled for one to work

In order to use the automatic runtime calibration for the 2 MHz or the 32 MHz internal oscilla-tors, the DFLL for both oscillators and both oscillators has to be enabled for one to work.

Problem fix/Workarund

Enabled both DFLLs and oscillators when using automatic runtime calibration for one of the internal oscillators.

6.	Updated “DAC Characteristics” on page 78. Removed DC output impedance.
7.	Fixed typo in “Packaging information” section.
8.	Fixed typo in “Errata” section.

37.5 8067K – 02/2010

1.	Added “PDI Speed vs. VCC” on page 95.

37.6 8067J – 02/2010

1.	Removed JTAG Reset from the datasheet.
2.	Updated “Timer/Counter and AWEX functions” on page 56.
3.	Updated “Alternate Pin Functions” on page 58.
3.	Updated all “Electrical Characteristics” on page 73.
4.	Updated “PAD Characteristics” on page 79.
5.	Changed Internal Oscillator Speed to “Oscillators and Wake-up Time” on page 92.
6.	Updated “Errata” on page 96

37.7 8067I – 04/2009

1.	Updated “Ordering Information” on page 2.
2.	Updated “PAD Characteristics” on page 79.

37.8 8067H – 04/2009

1.	Editorial updates.
2.	Updated “Overview” on page 54.
3.	Updated Table 29-9 on page 54.
4.	Updated “Peripheral Module Address Map” on page 62. IRCOM has address map: 0x08F8.
5.	Updated “Electrical Characteristics” on page 73.
6.	Updated “PAD Characteristics” on page 79.
7.	Updated “Typical Characteristics” on page 82.

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