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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a1-au

1. Ordering Information

Ordering Code	Flash (B)	E^2	SRAM	Speed (MHz)	Power Supply	Package[1][2][3]	Temp
ATxmega128A1-AU	128K + 8K	2 KB	8 KB	32	1.6 - 3.6V	100A	-40°C - 85°C
ATxmega128A1-AUR							
ATxmega64A1-AU	64K + 4K	2 KB	4 KB				
ATxmega64A1-AUR							
ATxmega128A1-CU	128K + 8K	2 KB	8 KB			100C1	
ATxmega128A1CUR							
ATxmega64A1-CU	64K + 4K	2 KB	4 KB				
ATxmega64A1-CUR							
ATxmega128A1-C7U	128K + 8K	2 KB	8 KB			100C2	
ATxmega128A1-C7UR							
ATxmega64A1-C7U	64K + 4K	2 KB	4 KB				
ATxmega64A1-C7UR							

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see “Packaging information” on page 70.

Package Type	
100A	100-lead, 14 x 14 x 1.0mm, 0.5mm lead pitch, thin profile plastic quad flat package (TQFP)
100C1	100-ball, 9 x 9 x 1.2mm body, ball pitch 0.88mm, chip ball grid array (CBGA)
100C2	100-ball, 7 x 7 x 1.0mm body, ball pitch 0.65mm, very thin fine-pitch ball grid array (VFBGA)

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	Sensor control	HVAC
Board control	Optical	Utility metering
White goods	Medical applications	

4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended reading

- XMEGA A Manual
- XMEGA A Application Notes

This device data sheet only contains part specific information and a short description of each peripheral and module. The XMEGA A Manual describes the modules and peripherals in depth. The XMEGA A application notes contain example code and show applied use of the modules and peripherals.

The XMEGA A Manual and Application Notes are available from http://www.atmel.com/avr.

5. Capacitive touch sensing

The Atmel QTouch library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the QTouch library user guide - also available for download from the Atmel website.

6. Disclaimer

For devices that are not available yet, typical values contained in this datasheet are based on simulations and characterization of other AVR XMEGA microcontrollers manufactured on the same process technology. Min. and Max values will be available after the device is characterized.

10. Event System

10.1 Features

- Inter-peripheral communication and signalling with minimum latency
- CPU and DMA independent operation
- 8 Event Channels allows for up to 8 signals to be routed at the same time
- Events can be generated by
  - Timer/Counters (TCxn)
  - Real Time Counter (RTC)
  - Analog to Digital Converters (ADCx)
  - Analog Comparators (ACx)
  - Ports (PORTx)
  - System Clock (Clk_{SYS})
  - Software (CPU)
- Events can be used by
  - Timer/Counters (TCxn)
  - Analog to Digital Converters (ADCx)
  - Digital to Analog Converters (DACx)
  - Ports (PORTx)
  - DMA Controller (DMAC)
  - IR Communication Module (IRCOM)
- The same event can be used by multiple peripherals for synchronized timing
- Advanced Features
  - Manual Event Generation from software (CPU)
  - Quadrature Decoding
  - Digital Filtering
- Functions in Active and Idle mode

10.2 Overview

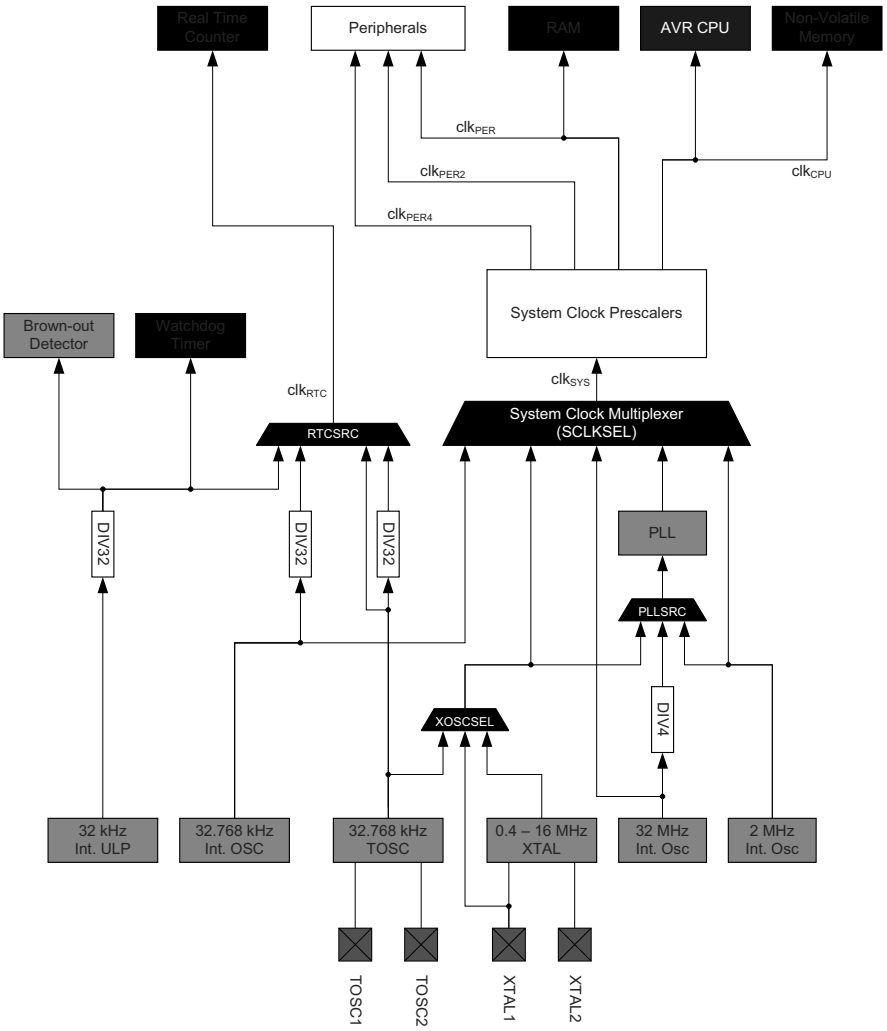
The Event System is a set of features for inter-peripheral communication. It enables the possibility for a change of state in one peripheral to automatically trigger actions in one or more peripherals. These changes in a peripheral that will trigger actions in other peripherals are configurable by software. It is a simple, but powerful system as it allows for autonomous control of peripherals without any use of interrupts, CPU or DMA resources.

The indication of a change in a peripheral is referred to as an event, and is usually the same as the interrupt conditions for that peripheral. Events are passed between peripherals using a dedicated routing network called the Event Routing Network. Figure 10-1 on page 20 shows a basic block diagram of the Event System with the Event Routing Network and the peripherals to which it is connected. This highly flexible system can be used for simple routing of signals, pin functions or for sequencing of events.

The maximum latency is two CPU clock cycles from when an event is generated in one peripheral, until the actions are triggered in one or more other peripherals.

The Event System is functional in both Active and Idle modes.

Figure 11-1. The clock system, clock sources and clock distribution



11.3 Clock Options

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources and PLL are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

11.3.1 32 kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

12. Power Management and Sleep Modes

12.1 Features

- Power management for adjusting power consumption and functions
- 5 sleep modes
  - Idle
  - Power-down
  - Power-save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

12.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

12.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

12.3.1 Idle Mode

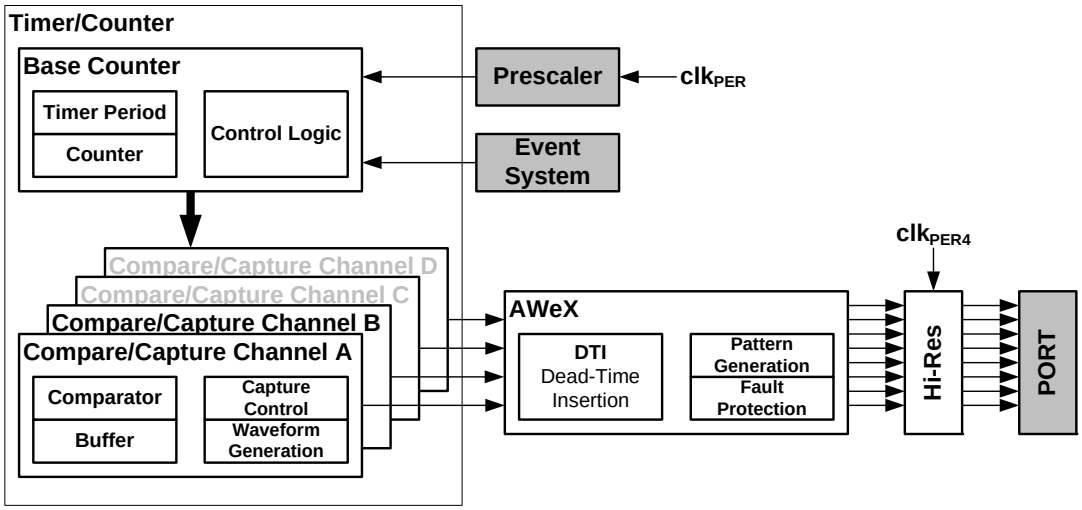
In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, event system and DMA controller are kept running. Any enabled interrupt will wake the device.

12.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt and asynchronous port interrupts, e.g pin change.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res - High Resolution Extension” on page 39 for more details.

Figure 16-1. Overview of a Timer/Counter and closely related peripherals



PORTC, PORTD, PORTE and PORTF each has one Timer/Counter 0 and one Timer/Counter1. Notation of these Timer/Counters are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1, TCE0, TCE1, TCF0, and TCF1, respectively.

It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different VCC voltage than used by the TWI bus.

PORTC, PORTD, PORTE, and PORTF each has one TWI. Notation of these peripherals are TWIC, TWID, TWIE, and TWIF.

30. Pinout and Pin Functions

The pinout of XMEGA A1 is shown in “Pinout/Block Diagram” on page 3. In addition to general I/O functionality, each pin may have several functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at time.

30.1 Alternate Pin Function Description

The tables below shows the notation for all pin functions available and describes its function.

30.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

30.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

30.1.3 Analog functions

ACn	Analog Comparator input pin n
AC0OUT	Analog Comparator 0 Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

30.1.4 EBI functions

An	Address line n	
Dn	Data line n	
$\overline{CSn}$	Chip Select n	
ALEn	Address Latch Enable pin n	(SRAM)
$\overline{RE}$	Read Enable	(SRAM)
$\overline{WE}$	External Data Memory Write	(SRAM /SDRAM)
BAn	Bank Address	(SDRAM)
$\overline{CAS}$	Column Access Strobe	(SDRAM)
CKE	SDRAM Clock Enable	(SDRAM)

Table 30-9. Port K - Alternate functions.

PORT K	PIN #	INTERRUPT	SDRAM 3P	SRAM ALE1 3P	SRAM ALE12 3P	LPC ALE1 3P	LPC ALE1 2P	LPC ALE12 2P
GND	73							
VCC	74							
PK0	75	SYNC	A0	A0/A8	A0/A8/A16	A8		
PK1	76	SYNC	A1	A1/A9	A1/A9/A17	A9		
PK2	77	SYNC/ASYNC	A2	A2/A10	A2/A10/A18	A10		
PK3	78	SYNC	A3	A3/A11	A3/A11/A19	A11		
PK4	79	SYNC	A4	A4/A12	A4/A12/A20	A12		
PK5	80	SYNC	A5	A5/A13	A5/A13/A21	A13		
PK6	81	SYNC	A6	A6/A14	A6/A14/A22	A14		
PK7	82	SYNC	A7	A7/A15	A7/A15/A23	A15		

Table 30-10. Port Q - Alternate functions.

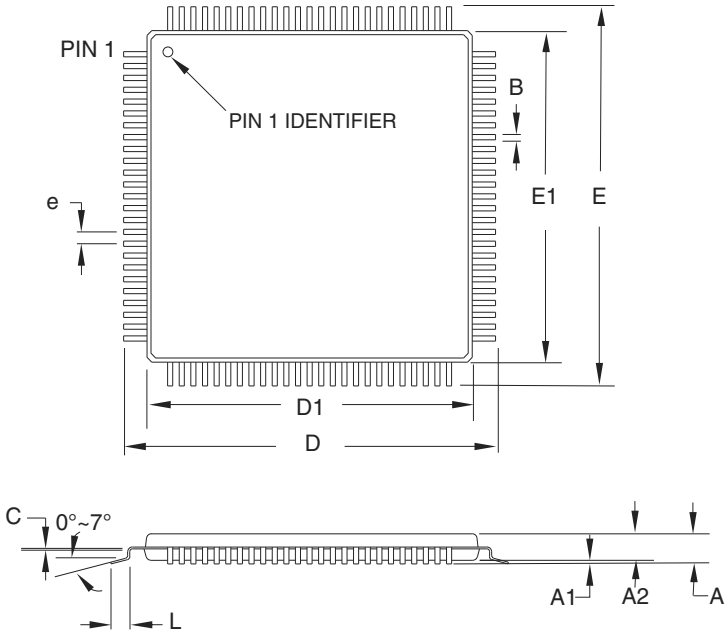
PORT Q	PIN #	INTERRUPT	
VCC	83		
GND	84		
PQ0	85	SYNC	TOSC1 (Input)
PQ1	86	SYNC	TOSC2 (Output)
PQ2	87	SYNC/ASYNC	
PQ3	88	SYNC	

Table 30-11. Port R - Alternate functions.

PORT R	PIN #	INTERRUPT	PDI	XTAL
PDI	89		PDI_DATA	
$\overline{\text{RESET}}$	90		PDI_CLOCK	
PRO	91	SYNC		XTAL2
PR1	92	SYNC		XTAL1

33. Packaging information

33.1 100A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	D

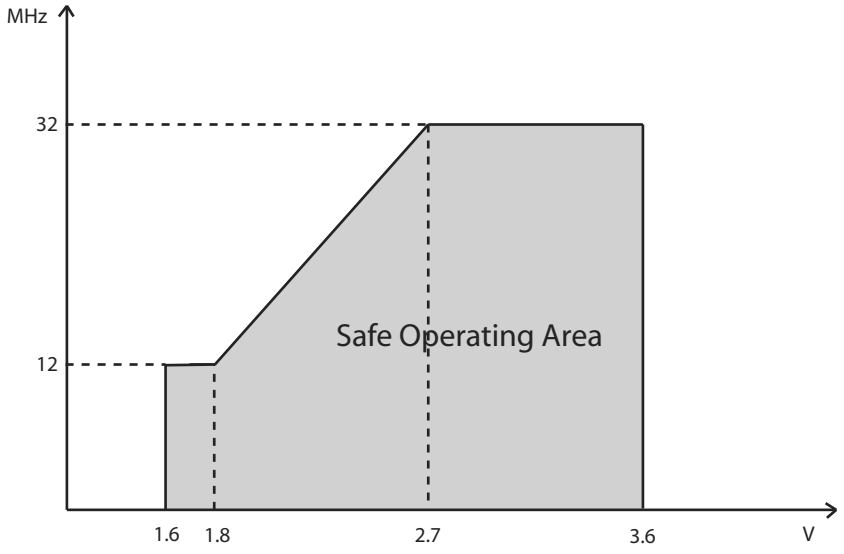
34.3 Speed

Table 34-2. Operating voltage and frequency.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency of the XMEGA A1 devices is depending on V_{CC}. As shown in Figure 34-1 on page 75 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 34-1. Maximum Frequency vs. Vcc



34.4 Flash and EEPROM Memory Characteristics

Table 34-3. Endurance and data retention.

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/Erase cycles	25°C	80K			Cycle
			85°C	30K			
		Data retention	25°C	100			Year
			55°C	25			

Table 34-4. Programming time.

Symbol	Parameter	Condition	Min	Typ[1]	Max	Units
	Chip Erase	Flash, EEPROM[2] and SRAM Erase		40		ms
	Flash	Page Erase		4		
		Page Write		6		
		Page WriteAutomatic Page Erase and Write		12		
	EEPROM	Page Erase		4		
		Page Write		6		
		Page Write Automatic Page Erase and Write		12		

Notes: 1. Programming is timed from the internal 2 MHz oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

34.5 ADC Characteristics

Table 34-5. ADC characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
RES	Resolution	Programmable: 8/12		8	12	12	Bits
INL	Integral Non-Linearity	500 kS/s		-5	<±1	5	LSB
DNL	Differential Non-Linearity	500 kS/s			< ±0.75		LSB
	Gain Error				±10		mV
	Offset Error				±2		mV
ADC_{clk}	ADC Clock frequency	Max is 1/4 of Peripheral Clock	$V_{CC} \geq 2.0V$			2000	kHz
			$V_{CC} < 2.0V$			500	

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Conversion rate	V_{CC}≥2.0V			2000	ksps
		V_{CC}<2.0V			500	
	Conversion time (propagation delay)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0 or 1	5	7	8	ADC_{clk} cycles
	Sampling Time	1/2 ADC_{clk} cycle	0.25			µS
	Conversion range		0		VREF	V
AVCC	Analog Supply Voltage		V_{cc}-0.3		V_{cc}+0.3	V
VREF	Reference voltage		1.0		V_{cc}-0.6	V
	Input bandwidth	V_{CC}≥2.0V			2000	kHz
		V_{CC}<2.0V			500	
INT1V	Internal 1.00V reference			1.00		V
INTVCC	Internal V_{CC}/1.6			V_{CC}/1.6		V
SCALEDVCC	Scaled internal V_{CC}/10 input			V_{CC}/10		V
R_{AREF}	Reference input resistance			>10		MΩ
	Start-up time			12	24	ADC_{clk} cycles
	Internal input sampling speed	Temp. sensor, V_{CC}/10, Bandgap			100	ksps

Table 34-6. ADC gain stage characteristics.

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Gain error	1 to 64 gain			< ±1		%
	Offset error				< ±1		mV
Vrms	Noise level at input	64x gain	VREF = Int. 1V		0.12		mV
			VREF = Ext. 2V		0.06		
	Clock rate	Same as ADC				1000	kHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage GPIO	I_{OH} = -8 mA, V_{CC} = 3.3V	2.6	3		V
		I_{OH} = -6 mA, V_{CC} = 3.0V	2.1	2.2		
		I_{OH} = -2 mA, V_{CC} = 1.8V	1.4	1.6		
I_{IL}	Input Leakage Current I/O pin			<0.001	1	µA
I_{IH}	Input Leakage Current I/O pin			<0.001	1	µA
R_P	I/O pin Pull/Buss keeper Resistor			20		kΩ
R_{RST}	Reset pin Pull-up Resistor			20		kΩ
	Input hysteresis			0.5		V

34.11 POR Characteristics

Table 34-12. Power-on Reset characteristics.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{POT-}	POR threshold voltage falling Vcc			1		V
V_{POT+}	POR threshold voltage rising Vcc			1.4		V

34.12 Reset Characteristics

Table 34-13. Reset characteristics.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Minimum reset pulse width			90		ns
	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.42*V_{CC}		

34.13 Oscillator Characteristics

Table 34-14. Internal 32.768kHz oscillator characteristics.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-0.5		0.5	%

35. Typical Characteristics

35.1 Active Supply Current

Figure 35-1. Active Supply Current vs. Frequency

f_{SYS} = 1 - 32 MHz, T = 25°C

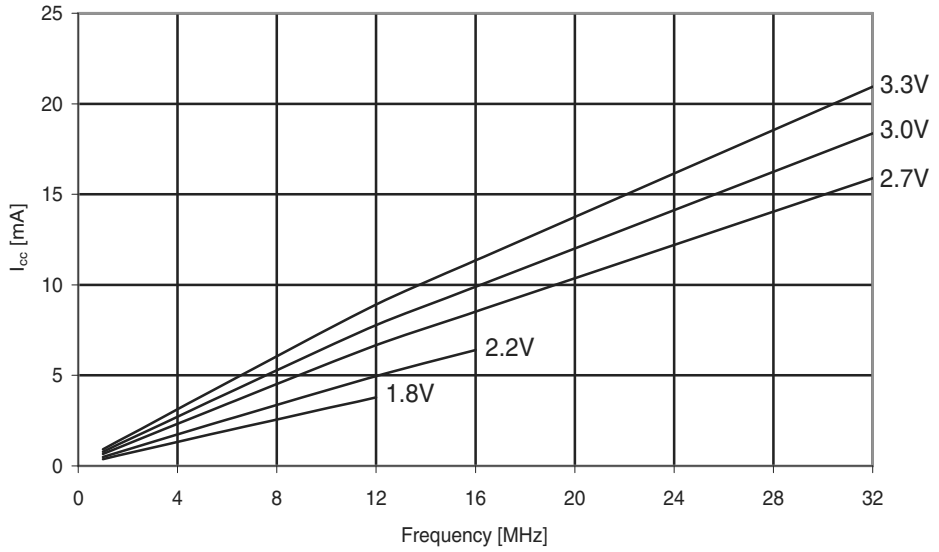


Figure 35-2. Active Supply Current vs. V_{CC}

f_{SYS} = 1.0 MHz

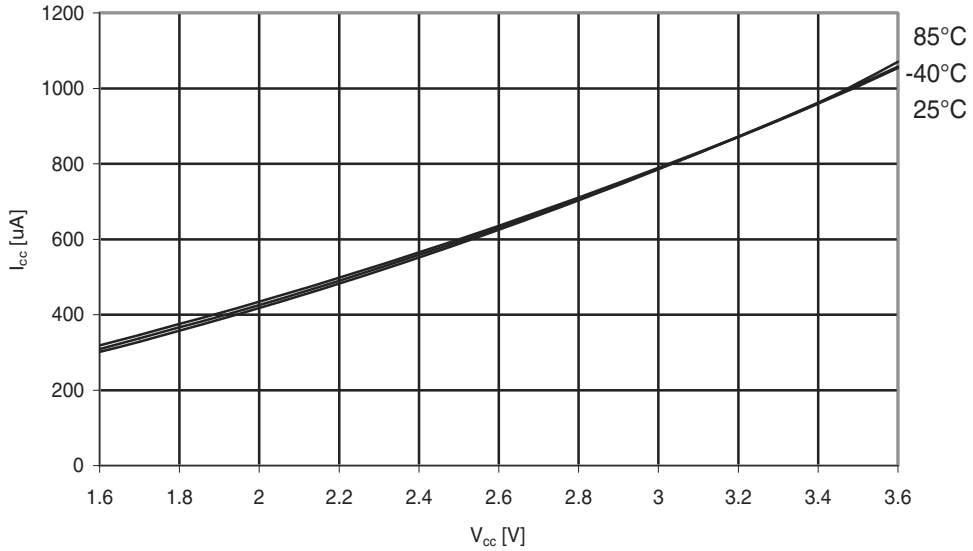
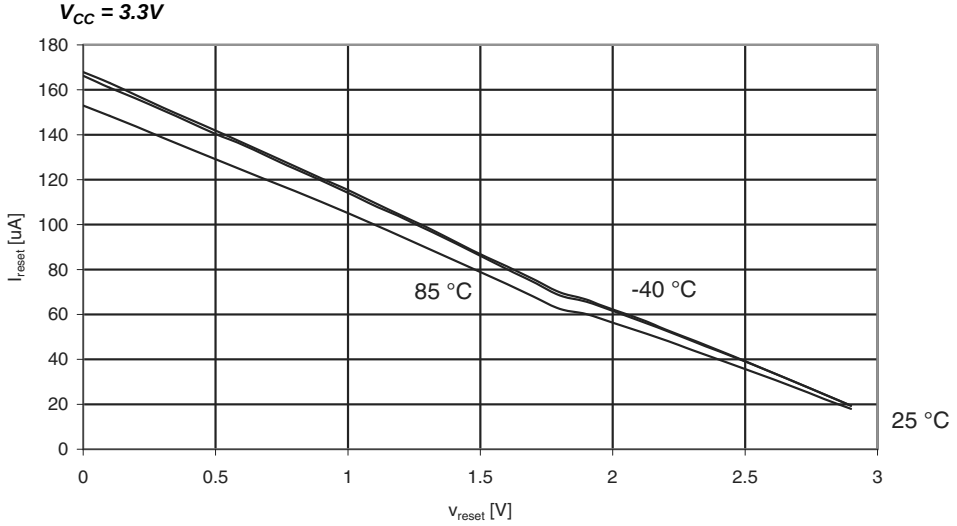
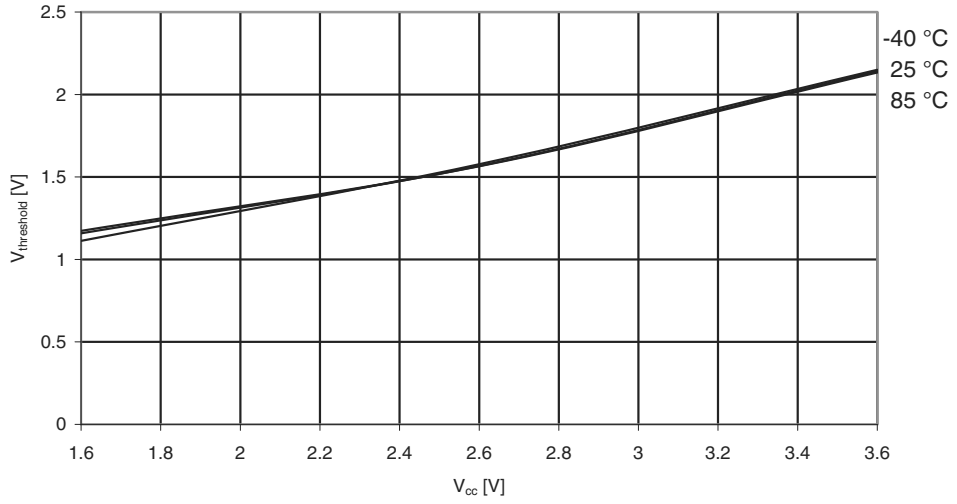


Figure 35-9. I/O Reset Pull-up Resistor Current vs. Reset Pin Voltage



35.6 Pin Thresholds and Hysteresis

Figure 35-10.I/O Pin Input Threshold Voltage vs. V_{CC}



- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag erroneously read as set
- WDR instruction inside closed window will not issue reset

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

Problem fix/Workaround

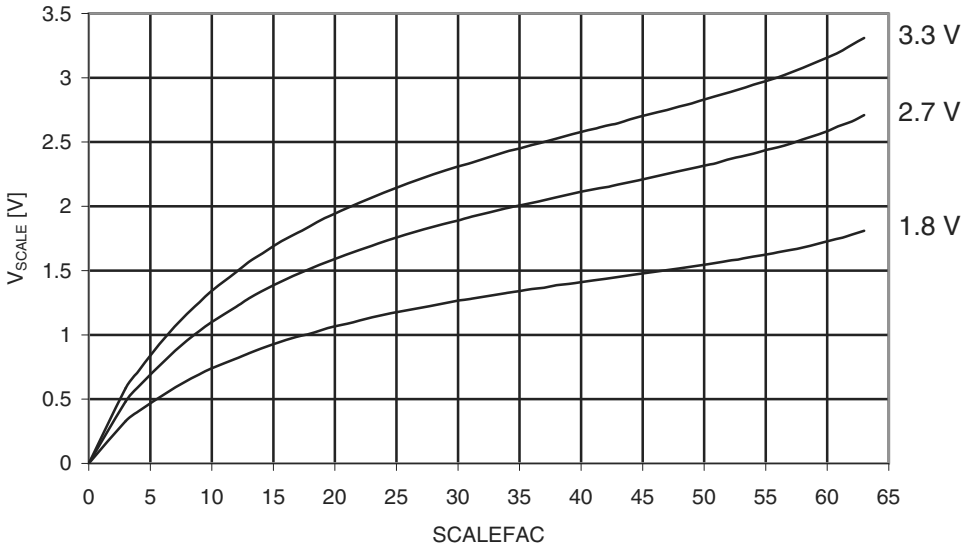
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Figure 36-1. Analog Comparator Voltage Scaler vs. Scalefac

T = 25°C



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. The ADC has up to ±2 LSB inaccuracy

The ADC will have up to ±2 LSB inaccuracy, visible as a saw-tooth pattern on the input voltage/ output value transfer function of the ADC. The inaccuracy increases with increasing voltage reference reaching ±2 LSB with 3V reference.

40. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

41. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

42. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

37.9 8067G – 11/2008

1. Updated “Block Diagram” on page 6.
2. Updated feature list in “Memories” on page 12.
3. Updated “Programming and Debugging” on page 54.
4. Updated “Peripheral Module Address Map” on page 62. IRCOM has address 0x8F0.
5. Added “Electrical Characteristics” on page 73.
6. Added “Typical Characteristics” on page 82.
7. Added “ATxmega64A1and ATxmega128A1 rev. H” on page 96.
8. Updated “ATxmega64A1 and ATxmega128A1 rev. G” on page 107.

37.10 8067F – 09/2008

1. Updated “Features” on page 1
2. Updated “Ordering Information” on page 2
3. Updated Figure 7-1 on page 11 and Figure 7-2 on page 11.
4. Updated Table 7-2 on page 15.
5. Updated “Features” on page 48 and “Overview” on page 48.
6. Removed “Interrupt Vector Summary” section from datasheet.

37.11 8067E – 08/2008

1. Changed Figure 2-1’s title to “Block diagram and pinout” on page 3.
2. Updated Figure 2-2 on page 4.
3. Updated Table 29-2 on page 51 and Table 29-3 on page 52.

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1. Updated “Ordering Information” on page 2.
2. Updated “Peripheral Module Address Map” on page 62.
3. Inserted “Interrupt Vector Summary” on page 56.