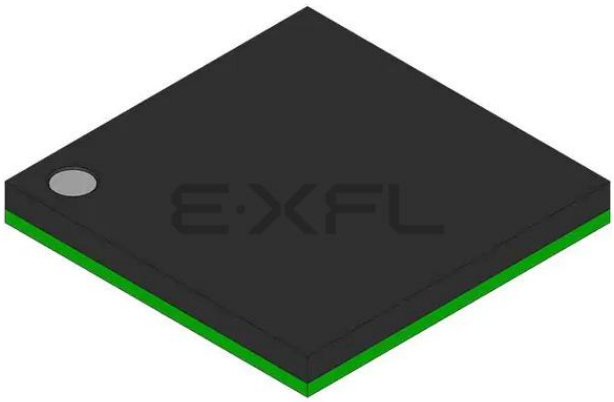

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atxmega64a1-c7u

4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended reading

- XMEGA A Manual
- XMEGA A Application Notes

This device data sheet only contains part specific information and a short description of each peripheral and module. The XMEGA A Manual describes the modules and peripherals in depth. The XMEGA A application notes contain example code and show applied use of the modules and peripherals.

The XMEGA A Manual and Application Notes are available from http://www.atmel.com/avr.

5. Capacitive touch sensing

The Atmel QTouch library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the QTouch library user guide - also available for download from the Atmel website.

6. Disclaimer

For devices that are not available yet, typical values contained in this datasheet are based on simulations and characterization of other AVR XMEGA microcontrollers manufactured on the same process technology. Min. and Max values will be available after the device is characterized.

8.10 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. For burst read (DMA), new data are available every cycle. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. External memory has multi-cycle read and write. The number of cycles depends on the type of memory and configuration of the external bus interface. Refer to the instruction summary for more details on instructions and instruction timing.

8.11 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

8.12 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

8.13 JTAG Disable

It is possible to disable the JTAG interface from the application software. This will prevent all external JTAG access to the device until the next device reset or until JTAG is enabled again from the application software. As long as JTAG is disabled, the I/O pins required for JTAG can be used as normal I/O pins.

8.14 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 8-2 shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) gives the page number and the least significant address bits (FWORD) gives the word in the page.

Table 8-2. Number of words and Pages in the Flash.

Device	PC size	Flash	Page Size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No of pages	Size	No of pages
ATxmega64A1	16	64K + 4K	128	Z[7:1]	Z[16:8]	64K	256	4K	16
ATxmega128A1	17	128K+ 8K	256	Z[8:1]	Z[17:9]	128K	256	8K	16

Table 8-3 shows EEPROM memory organization for the Atmel AVR XMEGA A1U devices. EEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM Address Register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Table 8-3. Number of Bytes and Pages in the EEPROM.

Device	EEPROM	Page Size	E2BYTE	E2PAGE	No of pages
	Size	bytes			
ATxmega64A1	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A1	2 KB	32	ADDR[4:0	ADDR[10:5]	64

8.14.1 I/O Memory

All peripherals and modules are addressable through I/O memory locations in the data memory space. All I/O memory locations can be accessed by the Load (LD/LDS/LDD) and Store (ST/STS/STD) instructions, transferring data between the 32 general purpose registers in the CPU and the I/O Memory.

The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions on these registers.

The I/O memory address for all peripherals and modules in XMEGA A1 is shown in the “Peripheral Module Address Map” on page 62.

11.3.2 32.768 kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

11.3.3 32.768 kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the 1 and 2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on 2 is available. This oscillator can be used as a clock source for the system clock and RTC.

11.3.4 0.4 - 16 MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

11.3.5 2 MHz Run-time Calibrated Internal Oscillator

The 2MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32kHz Calibrated Internal Oscillator or the 32kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

11.3.6 32 MHz Run-time Calibrated Internal Oscillator

The 32MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32kHz Calibrated Internal Oscillator or the 32kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

11.3.7 External Clock input

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 can be used as input for an external clock signal. The 1 and 2 pins is dedicated to driving a 32.768kHz crystal oscillator.

11.3.8 PLL with Multiplication factor 1 - 31x

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

Program Address (Base Address)	Source	Interrupt Description
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x038	USARTC1_INT_base	USART 1 on port C Interrupt base
0x03E	AES_INT_vect	AES Interrupt vector
0x040	NVM_INT_base	Non-Volatile Memory Interrupt base
0x044	PORTB_INT_base	Port B Interrupt base
0x048	ACB_INT_base	Analog Comparator on Port B Interrupt base
0x04E	ADCB_INT_base	Analog to Digital Converter on Port B Interrupt base
0x056	PORTE_INT_base	Port E Interrupt base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E Interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x06A	TCE1_INT_base	Timer/Counter 1 on port E Interrupt base
0x072	SPIE_INT_vect	SPI on port E Interrupt vector
0x074	USARTE0_INT_base	USART 0 on port E Interrupt base
0x07A	USARTE1_INT_base	USART 1 on port E Interrupt base
0x080	PORTD_INT_base	Port D Interrupt base
0x084	PORTA_INT_base	Port A Interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base
0x096	TWID_INT_base	Two-Wire Interface on Port D Interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0A6	TCD1_INT_base	Timer/Counter 1 on port D Interrupt base
0x0AE	SPID_INT_vector	SPI on port D Interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D Interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D Interrupt base
0x0BC	PORTQ_INT_base	Port Q INT base
0x0C0	PORTH_INT_base	Port H INT base
0x0C4	PORTJ_INT_base	Port J INT base
0x0C8	PORTK_INT_base	Port K INT base
0x0D0	PORTF_INT_base	Port F INT base
0x0D4	TWIF_INT_base	Two-Wire Interface on Port F INT base

Program Address (Base Address)	Source	Interrupt Description
0x0D8	TCF0_INT_base	Timer/Counter 0 on port F Interrupt base
0x0E4	TCF1_INT_base	Timer/Counter 1 on port F Interrupt base
0x0EC	SPIF_INT_vector	SPI ion port F Interrupt base
0x0EE	USARTF0_INT_base	USART 0 on port F Interrupt base
0x0F4	USARTF1_INT_base	USART 1 on port F Interrupt base

20. TWI - Two-Wire Interface

20.1 Features

- Four identical two-wire interface peripherals
- Bidirectional two-wire communication interface
  - Phillips I2C compatible
  - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
  - Slave operation
  - Single bus master operation
  - Bus master in multi-master bus environment
  - Multi-master arbitration
- Flexible slave address match functions
  - 7-bit and general call address recognition in hardware
  - 10-bit addressing supported
  - Address mask register for dual address match or address range masking
  - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes, including power-down
- 100kHz and 400kHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)

20.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is I2C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. The master initiates a data transaction by addressing a slave on the bus and telling whether it wants to transmit or receive data. One bus can have many slaves and one or several masters that can take control of the bus. An arbitration process handles priority if more than one master tries to transmit data at the same time. Mechanisms for resolving bus contention are inherent in the protocol.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead.

The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

26. ADC - 12-bit Analog to Digital Converter

26.1 Features

- Two ADCs with 12-bit resolution
- 2Msps sample rate for each ADC
- Signed and unsigned conversions
- 4 result registers with individual input channel control for each ADC
- 8 single ended inputs for each ADC
- 8x4 differential inputs for each ADC
- 4 internal inputs:
  - Integrated Temperature Sensor
  - DAC Output
  - VCC voltage divided by 10
  - Bandgap voltage
- Software selectable gain of 2, 4, 8, 16, 32 or 64
- Software selectable resolution of 8- or 12-bit.
- Internal or External Reference selection
- Event triggered conversion for accurate timing
- DMA transfer of conversion results
- Interrupt/Event on compare result

26.2 Overview

XMEGA A1 devices have two Analog to Digital Converters (ADC), see Figure 26-1 on page 49. The two ADC modules can be operated simultaneously, individually or synchronized.

The ADC converts analog voltages to digital values. The ADC has 12-bit resolution and is capable of converting up to 2 million samples per second. The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements an optional gain stage is available to increase the dynamic range. In addition several internal signal inputs are available. The ADC can provide both signed and unsigned results.

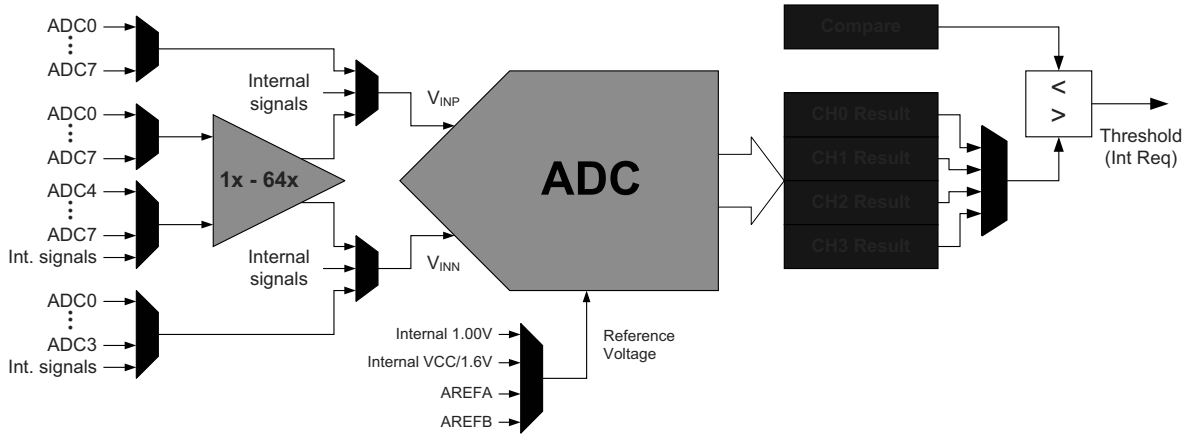
This is a pipeline ADC. A pipeline ADC consists of several consecutive stages, where each stage convert one part of the result. The pipeline design enables high sample rate at low clock speeds, and remove limitations on samples speed versus propagation delay. This also means that a new analog voltage can be sampled and a new ADC measurement started while other ADC measurements are ongoing.

ADC measurements can either be started by application software or an incoming event from another peripheral in the device. Four different result registers with individual input selection (MUX selection) are provided to make it easier for the application to keep track of the data. Each result register and MUX selection pair is referred to as an ADC Channel. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external analog reference voltages can be used. An accurate internal 1.0V reference is available.

An integrated temperature sensor is available and the output from this can be measured with the ADC. The output from the DAC, VCC/10 and the Bandgap voltage can also be measured by the ADC.

Figure 26-1. ADC overview



Each ADC has four MUX selection registers with a corresponding result register. This means that four channels can be sampled within 1.5 µs without any intervention by the application other than starting the conversion. The results will be available in the result registers.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5 µs for 12-bit to 2.5 µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each has one ADC. Notation of these peripherals are ADCA and ADCB, respectively.

Mnemonics	Operands	Description	Operation			Flags	#Clocks
LDI	Rd, K	Load Immediate	Rd	←	K	None	1
LDS	Rd, k	Load Direct from data space	Rd	←	(k)	None	2(1)(2)
LD	Rd, X	Load Indirect	Rd	←	(X)	None	1(1)(2)
LD	Rd, X+	Load Indirect and Post-Increment	Rd X	← ←	(X) X + 1	None	1(1)(2)
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, Rd ← (X)	← ←	X - 1 (X)	None	2(1)(2)
LD	Rd, Y	Load Indirect	Rd ← (Y)	←	(Y)	None	1(1)(2)
LD	Rd, Y+	Load Indirect and Post-Increment	Rd Y	← ←	(Y) Y + 1	None	1(1)(2)
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y Rd	← ←	Y - 1 (Y)	None	2(1)(2)
LDD	Rd, Y+q	Load Indirect with Displacement	Rd	←	(Y + q)	None	2(1)(2)
LD	Rd, Z	Load Indirect	Rd	←	(Z)	None	1(1)(2)
LD	Rd, Z+	Load Indirect and Post-Increment	Rd Z	← ←	(Z), Z+1	None	1(1)(2)
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z Rd	← ←	Z - 1, (Z)	None	2(1)(2)
LDD	Rd, Z+q	Load Indirect with Displacement	Rd	←	(Z + q)	None	2(1)(2)
STS	k, Rr	Store Direct to Data Space	(k)	←	Rd	None	2(1)
ST	X, Rr	Store Indirect	(X)	←	Rr	None	1(1)
ST	X+, Rr	Store Indirect and Post-Increment	(X) X	← ←	Rr, X + 1	None	1(1)
ST	-X, Rr	Store Indirect and Pre-Decrement	X (X)	← ←	X - 1, Rr	None	2(1)
ST	Y, Rr	Store Indirect	(Y)	←	Rr	None	1(1)
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) Y	← ←	Rr, Y + 1	None	1(1)
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y (Y)	← ←	Y - 1, Rr	None	2(1)
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q)	←	Rr	None	2(1)
ST	Z, Rr	Store Indirect	(Z)	←	Rr	None	1(1)
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) Z	← ←	Rr Z + 1	None	1(1)
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z	←	Z - 1	None	2(1)
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q)	←	Rr	None	2(1)
LPM		Load Program Memory	R0	←	(Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd	←	(Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd Z	← ←	(Z), Z + 1	None	3
ELPM		Extended Load Program Memory	R0	←	(RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd	←	(RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd Z	← ←	(RAMPZ:Z), Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z)	←	R1:R0	None	-

Mnemonics	Operands	Description	Operation	Flags	#Clocks
MCU Control Instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing Internal SRAM.

34. Electrical Characteristics

34.1 Absolute Maximum Ratings*

Operating Temperature . . . . . -55°C to +125°C

Storage Temperature . . . . . -65°C to +150°C

Voltage on any Pin with respect to Ground-0.5V to V_{CC}+0.5V

Maximum Operating Voltage 3.6V

DC Current per I/O Pin. . . . . 20.0 mA

DC Current V_{CC} and GND Pins. . . . . 200.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

34.2 DC Characteristics

Table 34-1. Current consumption.

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC}	Active mode(1)	1 MHz, Ext. Clk	V_{CC} = 1.8V		365		µA
			V_{CC} = 3.0V		790		
		2 MHz, Ext. Clk	V_{CC} = 1.8V		690	800	
			V_{CC} = 3.0V		1400	1600	
		32 MHz, Ext. Clk	V_{CC} = 3.0V		18.35	20	mA
	Idle mode(1)	1 MHz, Ext. Clk	V_{CC} = 1.8V		135		µA
			V_{CC} = 3.0V		255		
		2 MHz, Ext. Clk	V_{CC} = 1.8V		270	380	
			V_{CC} = 3.0V		510	650	
		32 MHz, Ext. Clk	V_{CC} = 3.0V		8.15	9.2	mA
	Power-down mode	All Functions Disabled	V_{CC} = 3.0V		0.1		µA
		All Functions Disabled, T = 85°C	V_{CC} = 3.0V		2	5	
		ULP, WDT, Sampled BOD	V_{CC} = 1.8V		0.5		
			V_{CC} = 3.0V		0.6		
		ULP, WDT, Sampled BOD, T=85°C	V_{CC} = 3.0V		3	10	
	Power-save mode	RTC 1 kHz from Low Power 32 kHz	V_{CC} = 1.8V		0.52		µA
			V_{CC} = 3.0V		0.55		
		RTC from Low Power 32 kHz	V_{CC} = 3.0V		1.16		

Symbol	Parameter	Condition	Min	Typ	Max	Units
	ADC/DAC ref	T= 85°C, After calibration	0.99		1.01	V
				1		
	Variation over voltage and temperature	V_{CC} = 1.6 - 3.6V, T = -40°C to 85°C		±5		%

34.9 Brownout Detection Characteristics

Table 34-10. Brownout Detection characteristics.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	BOD level 0 falling Vcc			1.6		V
	BOD level 1 falling Vcc			1.9		
	BOD level 2 falling Vcc			2.1		
	BOD level 3 falling Vcc			2.4		
	BOD level 4 falling Vcc			2.6		
	BOD level 5 falling Vcc			2.9		
	BOD level 6 falling Vcc			3.2		
	BOD level 7 falling Vcc			3.4		
	Hysteresis	BOD level 0-5		2		%

Note: 1. BOD is calibrated to BOD level 0 at 85°C, and BOD level 0 is the default level.

34.10 PAD Characteristics

Table 34-11. PAD characteristics.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	V_{CC} = 2.4 - 3.6V	0.7*V_{CC}		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V	0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Input Low Voltage	V_{CC} = 2.4 - 3.6V	-0.5		0.3*V_{CC}	V
		V_{CC} = 1.6 - 2.4V	-0.5		0.2*V_{CC}	
V_{OL}	Output Low Voltage GPIO	I_{OL} = 15 mA, V_{CC} = 3.3V		0.45	0.76	V
		I_{OL} = 10 mA, V_{CC} = 3.0V		0.3	0.64	
		I_{OL}= 5 mA, V_{CC} = 1.8V		0.2	0.46	

Figure 35-19.Analog Comparator Hysteresis vs. V_{CC}, High-speed

Large hysteresis

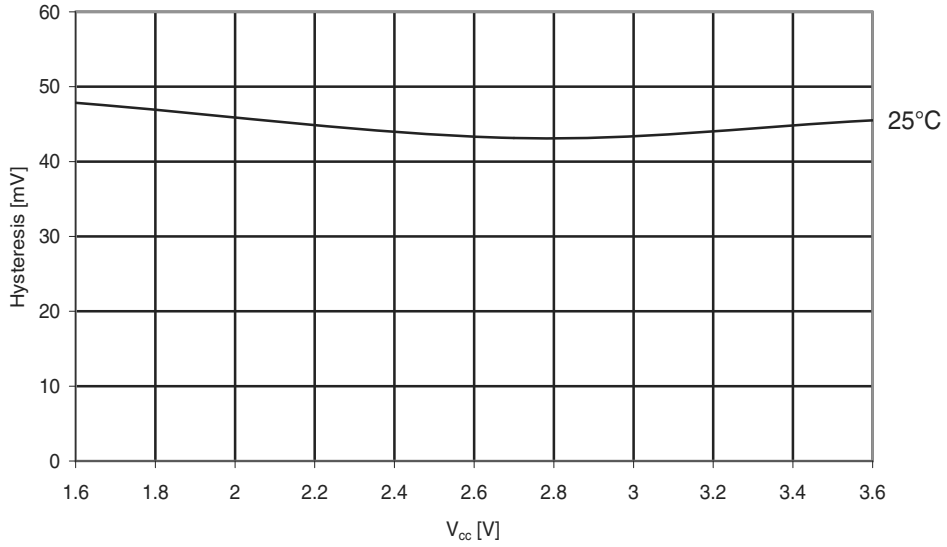
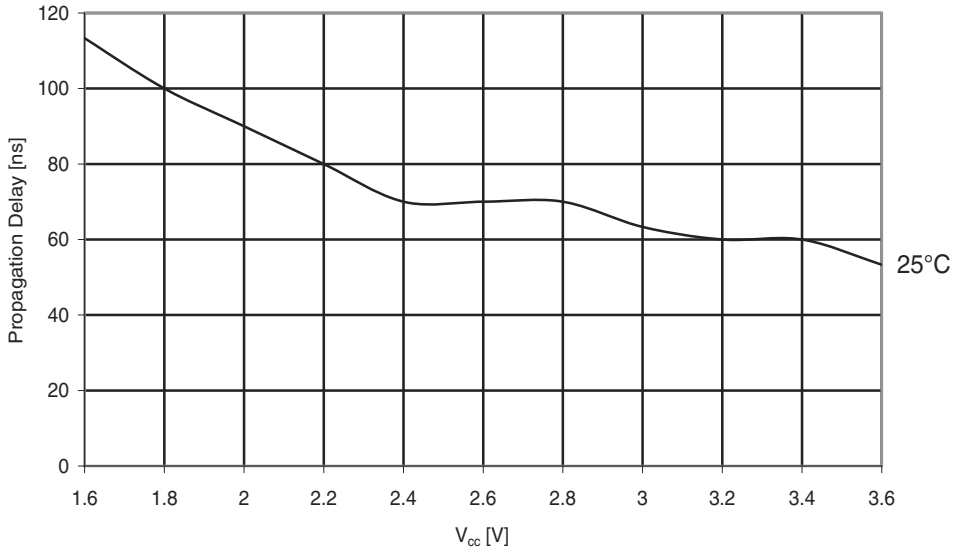


Figure 35-20.Analog Comparator Propagation Delay vs. V_{CC}

High-speed



18. DAC has up to ±10 LSB noise in Sampled Mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

19. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto trigged conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion internal never is shorter than 1.5 µs.

20. Both DFLLs and both oscillators have to be enabled for one to work

In order to use the automatic runtime calibration for the 2 MHz or the 32 MHz internal oscillators, the DFLL for both oscillators and both oscillators have to be enabled for one to work.

Problem fix/Workaround

Enable both DFLLs and both oscillators when using automatic runtime calibration for either of the internal oscillators.

21. Access error when multiple bus masters are accessing SDRAM

If one bus master (CPU and DMA channels) is using the EBI to access an SDRAM in burst mode and another bus master is accessing the same row number in a different BANK of the SDRAM in the cycle directly after the burst access is complete, the access for the second bus master will fail.

Problem fix/Workaround

Do not put stack pointer in SDRAM and use DMA Controller in 1 byte burst mode if CPU and DMA Controller are required to access SDRAM at the same time.

22. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

23. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

24. Pin configuration does not affect Analog Comparator Output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output function.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

25. Low level interrupt triggered when pin input is disabled

If a pin input is disabled, but pin is configured to trigger on low level, interrupt request will be sent.

Problem fix/Workaround

Ensure that Interrupt mask for the disabled pin is cleared.

26. JTAG enable does not override Analog Comparator B output

When JTAG is enabled this will not override the Analog Comparator B (ACB) output, AC0OUT on pin 7 if this is enabled.

Problem fix/Workaround

Use Analog Comparator output for ACA when JTAG is used, or use the PDI as debug interface.

27. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

28. Flash Power Reduction Mode can not be enabled when entering sleep

If Flash Power Reduction Mode is enabled when entering Power-save or Extended Standby sleep mode, the device will only wake up on every fourth wake-up request. If Flash Power Reduction Mode is enabled when entering Idle sleep mode, the wake-up time will vary with up to 16 CPU clock cycles.

37. TWI, a general address call will match independent of the R/W-bit value

When the TWI is in Slave mode and a general address call is issued on the bus, the TWI Slave will get an address match regardless of the received R/W bit.

Problem fix/Workaround

Use software to check the R/W-bit on general call address match.

38. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

39. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

37. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

37.1 8067O – 06/2013

1.	Not recommended for new designs - Use XMEGA A1U series.

37.2 8067N – 03/2013

1.	Removed all references to ATxmega192A1, ATxmega256A1 and ATxmega384A1.
2.	Updated module description. Based on the XMEGA A1U device datasheet.
3.	Updated analog comparator (AC) overview, Figure 28-1 on page 53.
4.	Updated “ADC Characteristics” on page 76.
5	Updated page erase time in “Flash and EEPROM Memory Characteristics” on page 76.
6	Updated Output low voltage conditions from I_{OH} to I_{OL} in “PAD Characteristics” on page 79.
7.	Removed TBDs from: “DC Characteristics” on page 73. “DAC Characteristics” on page 78. “Bandgap Characteristics” on page 78.
8.	Updated “Errata” on page 96 to be valid for both ATxmega64A1 and ATxmega128A1.
9.	Removed Boundary Scan Order table.

37.3 8067M – 09/2010

1.	Updated Errata “ATxmega64A1and ATxmega128A1 rev. H” on page 96

37.4 8067L – 08/2010

1.	Removed Footnote 3 of Figure 2-1 on page 3
2.	Updated “Features” on page 32. Event Channel 0 output on port pin 7
3.	Updated “DC Characteristics” on page 73, by adding I_{CC} for Flash/EEPROM Programming.
4.	Added AVCC in “ADC Characteristics” on page 76.
5.	Updated Start up time in “ADC Characteristics” on page 76.