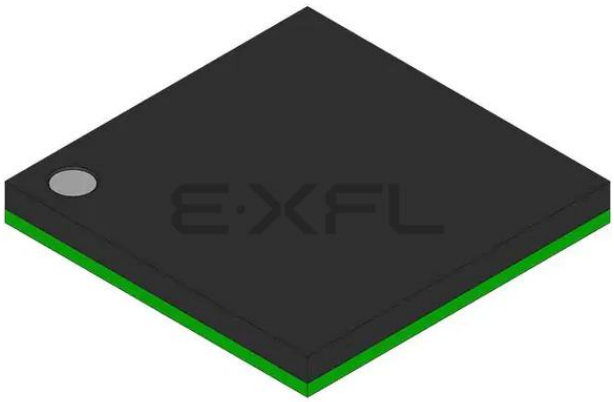

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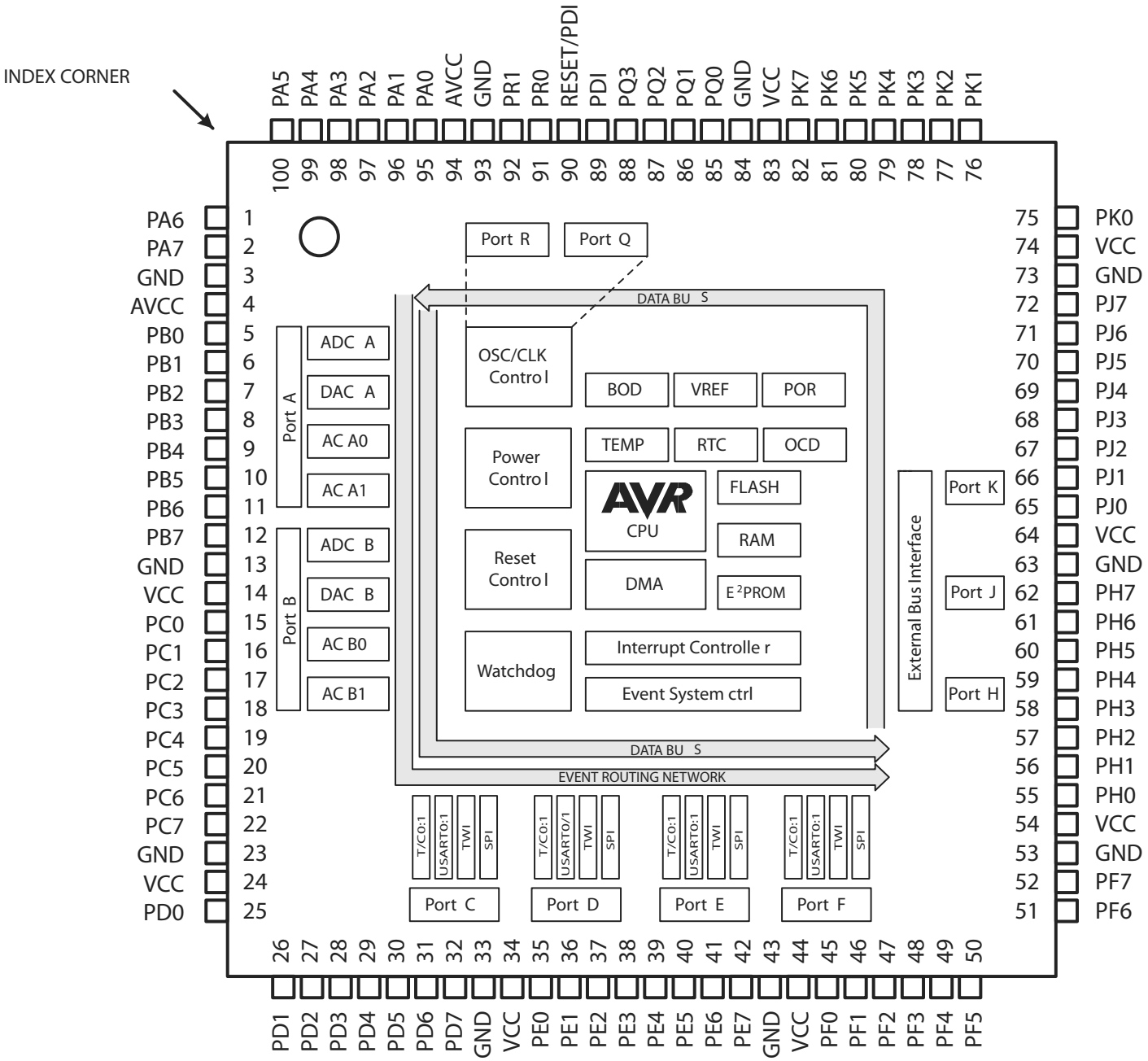
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atxmega64a1-cu

2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout



Notes: 1. For full details on pinout and pin functions refer to “Pinout and Pin Functions” on page 55.

2. VCC/GND on pin 83/84 are swapped compared to other VCC/GND to allow easier routing of GND to 32kHz crystal.

3.1 Block Diagram

Figure 3-1. XMEGA A1 Block Diagram

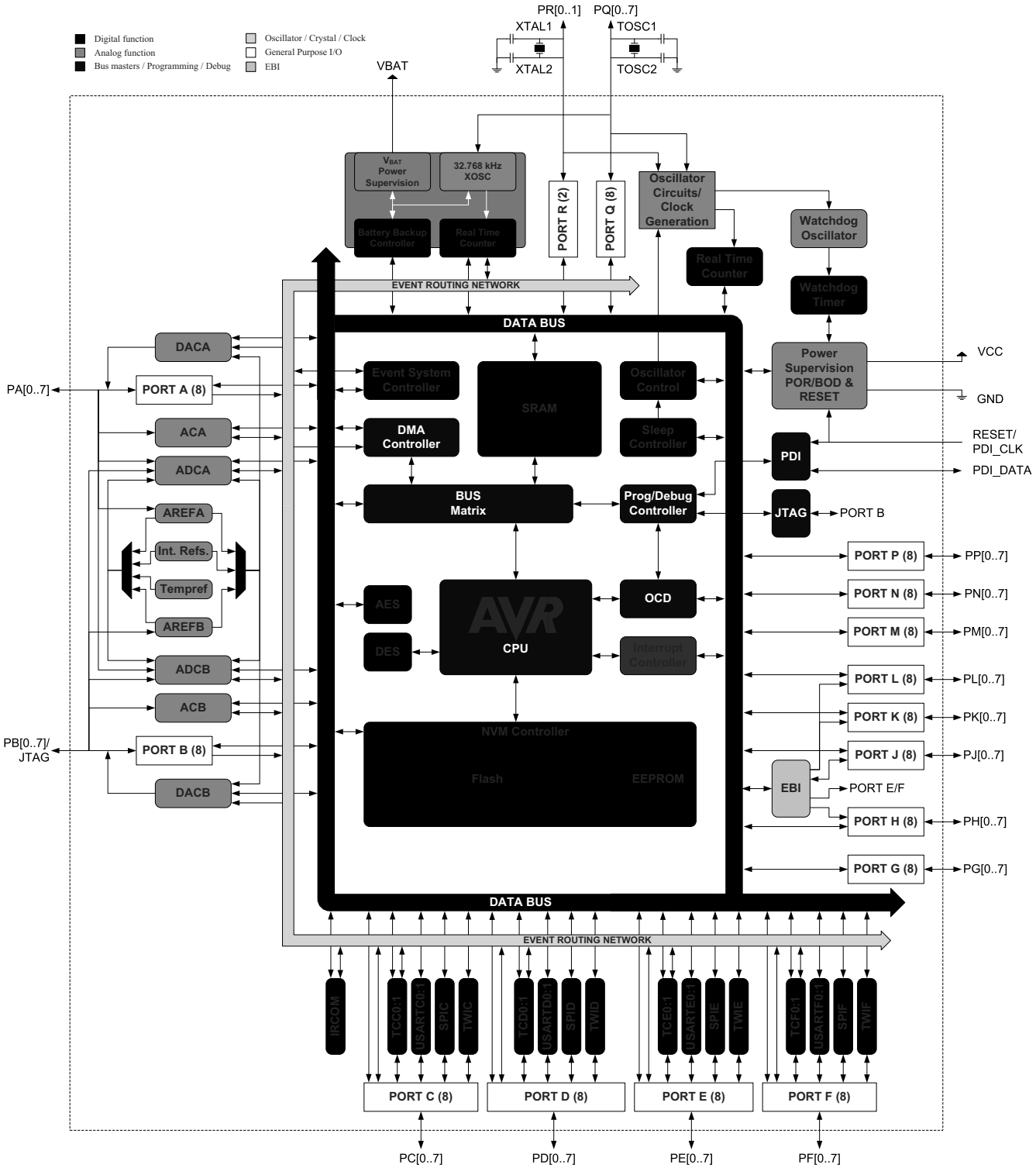
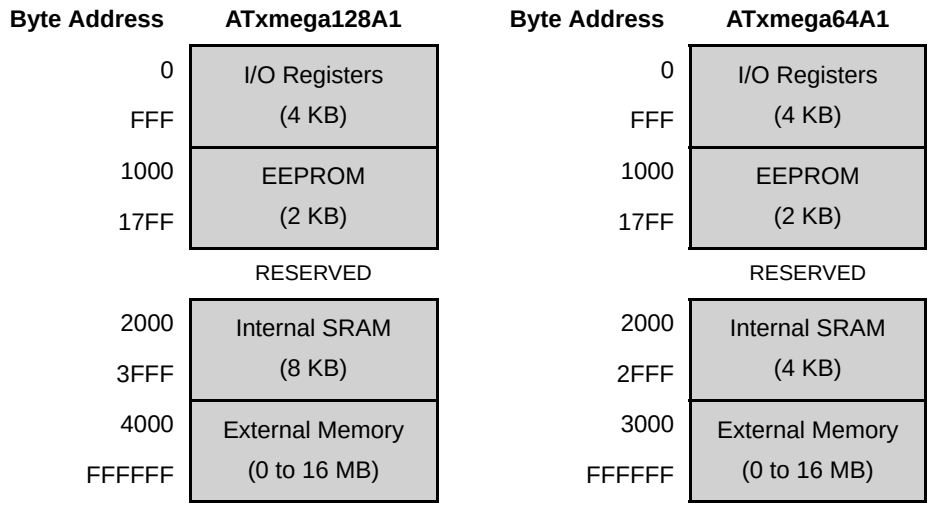


Figure 8-2. Data Memory Map (Hexadecimal address)



8.6 EEPROM

XMEGA AU devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

8.7 I/O Memory

The status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which is used to transfer data between the 32 registers in the register file and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly. In the address range 0x00 - 0x1F, single- cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules in XMEGA A1U is shown in the “Peripheral Module Address Map” on page 62.

8.7.1 General Purpose I/O Registers

The lowest 16 I/O memory addresses are reserved as general purpose I/O registers. These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

8.8 External Memory

Four ports can be used for external memory, supporting external SRAM, SDRAM, and memory mapped peripherals such as LCD displays. Refer to “EBI – External Bus Interface” on page 47. The external memory address space will always start at the end of internal SRAM.

8.9 Data Memory and Bus Arbitration

Since the data memory is organized as four separate sets of memories, the different bus masters (CPU, DMA controller read and DMA controller write, etc.) can access different memory sections at the same time.

Table 8-3. Number of Bytes and Pages in the EEPROM.

Device	EEPROM	Page Size	E2BYTE	E2PAGE	No of pages
	Size	bytes			
ATxmega64A1	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A1	2 KB	32	ADDR[4:0	ADDR[10:5]	64

8.14.1 I/O Memory

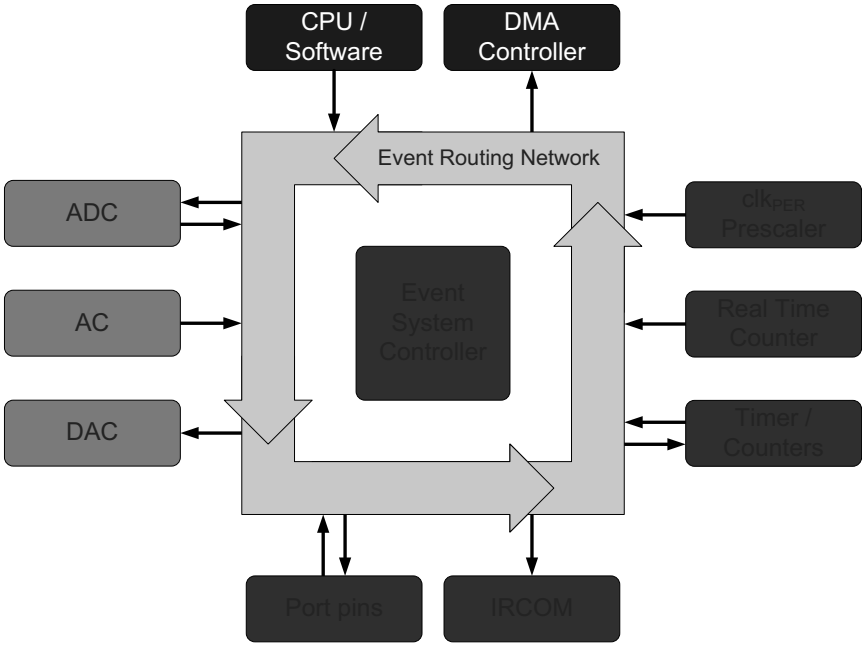
All peripherals and modules are addressable through I/O memory locations in the data memory space. All I/O memory locations can be accessed by the Load (LD/LDS/LDD) and Store (ST/STS/STD) instructions, transferring data between the 32 general purpose registers in the CPU and the I/O Memory.

The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions on these registers.

The I/O memory address for all peripherals and modules in XMEGA A1 is shown in the “Peripheral Module Address Map” on page 62.

Figure 10-1. Event system block diagram.



he event routing network consists of eight software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to eight parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

11. System Clock and Clock options

11.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal Oscillators:
  - 32 MHz run-time calibrated RC oscillator
  - 2 MHz run-time calibrated RC oscillator
  - 32.768 kHz calibrated RC oscillator
  - 32 kHz Ultra Low Power (ULP) oscillator with 1 kHz ouput
- External clock options
  - 0.4 - 16 MHz Crystal Oscillator
  - 32 kHz Crystal Oscillator
  - External clock
- PLL with internal and external clock options with 1 to 31x multiplication
- Clock Prescalers with 1x to 2048x division
- Fast peripheral clock running at two and four times the CPU clock speed
- Automatic Run-Time Calibration of internal oscillators
- Crystal Oscillator failure detection

11.2 Overview

Atmel AVR XMEGA devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 11-1 on page 22 presents the principal clock system in the XMEGA A1U family devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers as described in “Power Management and Sleep Modes” on page 24.

26. ADC - 12-bit Analog to Digital Converter

26.1 Features

- Two ADCs with 12-bit resolution
- 2Msps sample rate for each ADC
- Signed and unsigned conversions
- 4 result registers with individual input channel control for each ADC
- 8 single ended inputs for each ADC
- 8x4 differential inputs for each ADC
- 4 internal inputs:
  - Integrated Temperature Sensor
  - DAC Output
  - VCC voltage divided by 10
  - Bandgap voltage
- Software selectable gain of 2, 4, 8, 16, 32 or 64
- Software selectable resolution of 8- or 12-bit.
- Internal or External Reference selection
- Event triggered conversion for accurate timing
- DMA transfer of conversion results
- Interrupt/Event on compare result

26.2 Overview

XMEGA A1 devices have two Analog to Digital Converters (ADC), see Figure 26-1 on page 49. The two ADC modules can be operated simultaneously, individually or synchronized.

The ADC converts analog voltages to digital values. The ADC has 12-bit resolution and is capable of converting up to 2 million samples per second. The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements an optional gain stage is available to increase the dynamic range. In addition several internal signal inputs are available. The ADC can provide both signed and unsigned results.

This is a pipeline ADC. A pipeline ADC consists of several consecutive stages, where each stage convert one part of the result. The pipeline design enables high sample rate at low clock speeds, and remove limitations on samples speed versus propagation delay. This also means that a new analog voltage can be sampled and a new ADC measurement started while other ADC measurements are ongoing.

ADC measurements can either be started by application software or an incoming event from another peripheral in the device. Four different result registers with individual input selection (MUX selection) are provided to make it easier for the application to keep track of the data. Each result register and MUX selection pair is referred to as an ADC Channel. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external analog reference voltages can be used. An accurate internal 1.0V reference is available.

An integrated temperature sensor is available and the output from this can be measured with the ADC. The output from the DAC, VCC/10 and the Bandgap voltage can also be measured by the ADC.

CLK	SDRAM Clock	(SDRAM)
$\overline{DQM}$	Data Mask Signal/Output Enable	(SDRAM)
$\overline{RAS}$	Row Access Strobe	(SDRAM)
2P	2 Port Interface	
3P	3 Port Interface	

30.1.5 Timer/Counter and AWEX functions

OCnx	Output Compare Channel x for Timer/Counter n
$\overline{OCnx}$	Inverted Output Compare Channel x for Timer/Counter n
OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

30.1.6 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
$\overline{SS}$	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

30.1.7 Oscillators, Clock and Event

n	Timer Oscillator pin n
XTALn	Input/Output for inverting Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel 0 Output

30.1.8 Debug/System functions

$\overline{\text{RESET}}$	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin
TCK	JTAG Test Clock
TDI	JTAG Test Data In
TDO	JTAG Test Data Out
TMS	JTAG Test Mode Select

PORT C	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPIC	TWIC	CLOCKOUT	EVENTOUT
PC3	18	SYNC	OC0D	OC0BHS		TXD0					
PC4	19	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PC5	20	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	21	SYNC		OC0DLS			RXD1	MISO			
PC7	22	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT

Table 30-4. Port D - Alternate functions.

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPID	TWID	CLOCKOUT	EVENTOUT
GND	23									
VCC	24									
PD0	25	SYNC	OC0A					SDA		
PD1	26	SYNC	OC0B		XCK0			SCL		
PD2	27	SYNC/ASYNC	OC0C		RXD0					
PD3	28	SYNC	OC0D		TXD0					
PD4	29	SYNC		OC1A			$\overline{SS}$			
PD5	30	SYNC		OC1B		XCK1	MOSI			
PD6	31	SYNC				RXD1	MISO			
PD7	32	SYNC				TXD1	SCK		CLKOUT	EVOUT

Table 30-5. Port E - Alternate functions.

PORT E	PIN #	INTERRUPT	TCE0	AWEXE	TCE1	USARTE0	USARTE1	SPIE	TWIE	CLOCKOUT	EVENTOUT
GND	33										
VCC	34										
PE0	35	SYNC	OC0A	OC0ALS					SDA		
PE1	36	SYNC	OC0B	OC0AHS		XCK0			SCL		
PE2	37	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PE3	38	SYNC	OC0D	OC0BHS		TXD0					
PE4	39	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PE5	40	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PE6	41	SYNC		OC0DLS			RXD1	MISO			
PE7	42	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT

Table 30-6. Port F - Alternate functions.

PORT F	PIN #	INTERRUPT	TCF0	TCF1	USARTF0	USARTF1	SPIF	TWIF
GND	43							
VCC	44							
PF0	45	SYNC	OC0A					SDA

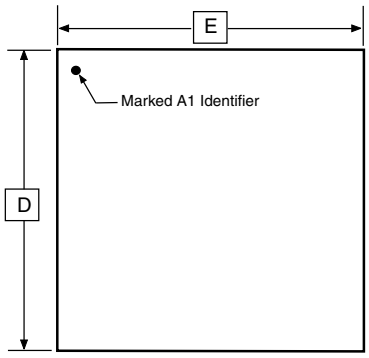
31. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in XMEGA A1. For complete register description and summary for each peripheral module, refer to the XMEGA A Manual.

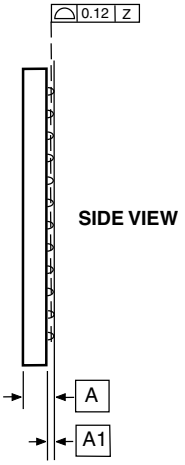
Table 31-1. Peripheral Module Address Map

Base Address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 3
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32 MHz Internal RC Oscillator
0x0068	DFLLRC2M	DFLL for the 2 MHz RC Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watch-Dog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable Multilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x00C0	AES	AES Module
0x0100	DMA	DMA Controller
0x0180	EVSYS	Event System
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0240	ADCB	Analog to Digital Converter on port B
0x0300	DACA	Digital to Analog Converter on port A
0x0320	DACB	Digital to Analog Converter on port B
0x0380	ACA	Analog Comparator pair on port A
0x0390	ACB	Analog Comparator pair on port B
0x0400	RTC	Real Time Counter
0x0440	EBI	External Bus Interface
0x0480	TWIC	Two Wire Interface on port C
0x0490	TWID	Two Wire Interface on port D

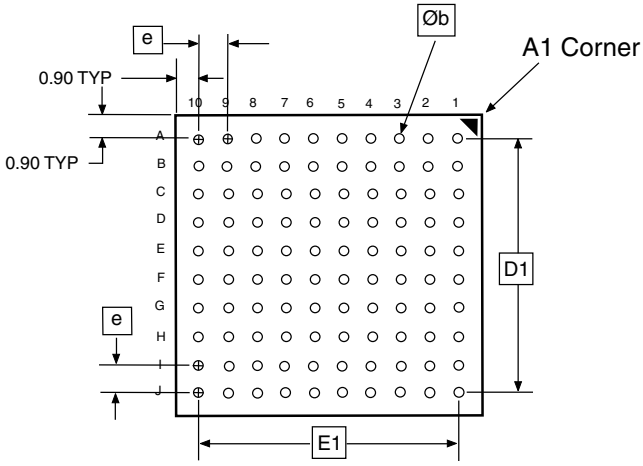
33.2 100C1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.10	–	1.20	
A1	0.30	0.35	0.40	
D	8.90	9.00	9.10	
E	8.90	9.00	9.10	
D1	7.10	7.20	7.30	
E1	7.10	7.20	7.30	
Øb	0.35	0.40	0.45	
e	0.80 TYP			

5/25/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100C1**, 100-ball, 9 x 9 x 1.2 mm Body, Ball Pitch 0.80 mm Chip Array BGA Package (CBGA)	100C1	A

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Conversion rate	V_{CC}≥2.0V			2000	ksps
		V_{CC}<2.0V			500	
	Conversion time (propagation delay)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0 or 1	5	7	8	ADC_{clk} cycles
	Sampling Time	1/2 ADC_{clk} cycle	0.25			µS
	Conversion range		0		VREF	V
AVCC	Analog Supply Voltage		V_{cc}-0.3		V_{cc}+0.3	V
VREF	Reference voltage		1.0		V_{cc}-0.6	V
	Input bandwidth	V_{CC}≥2.0V			2000	kHz
		V_{CC}<2.0V			500	
INT1V	Internal 1.00V reference			1.00		V
INTVCC	Internal V_{CC}/1.6			V_{CC}/1.6		V
SCALEDVCC	Scaled internal V_{CC}/10 input			V_{CC}/10		V
R_{AREF}	Reference input resistance			>10		MΩ
	Start-up time			12	24	ADC_{clk} cycles
	Internal input sampling speed	Temp. sensor, V_{CC}/10, Bandgap			100	ksps

Table 34-6. ADC gain stage characteristics.

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Gain error	1 to 64 gain			< ±1		%
	Offset error				< ±1		mV
Vrms	Noise level at input	64x gain	VREF = Int. 1V		0.12		mV
			VREF = Ext. 2V		0.06		
	Clock rate	Same as ADC				1000	kHz

35. Typical Characteristics

35.1 Active Supply Current

Figure 35-1. Active Supply Current vs. Frequency

f_{SYS} = 1 - 32 MHz, T = 25°C

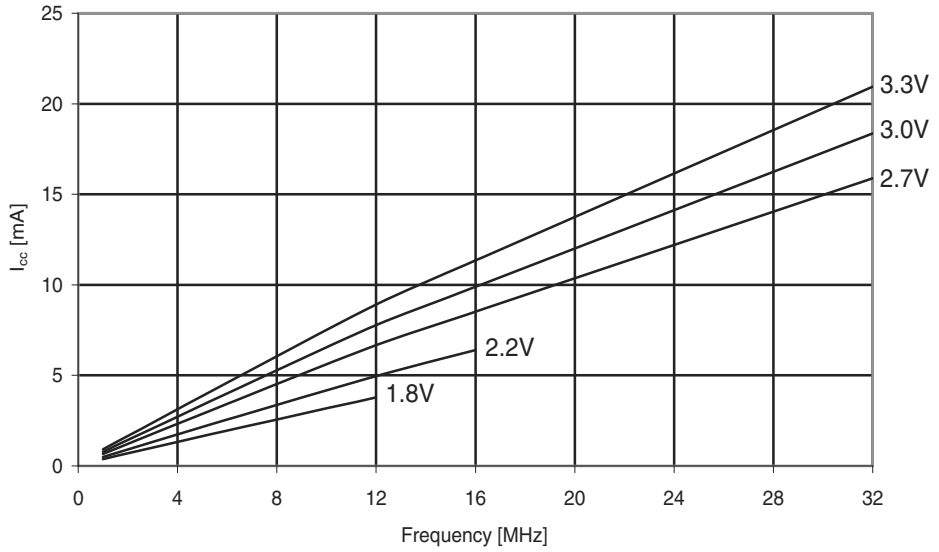
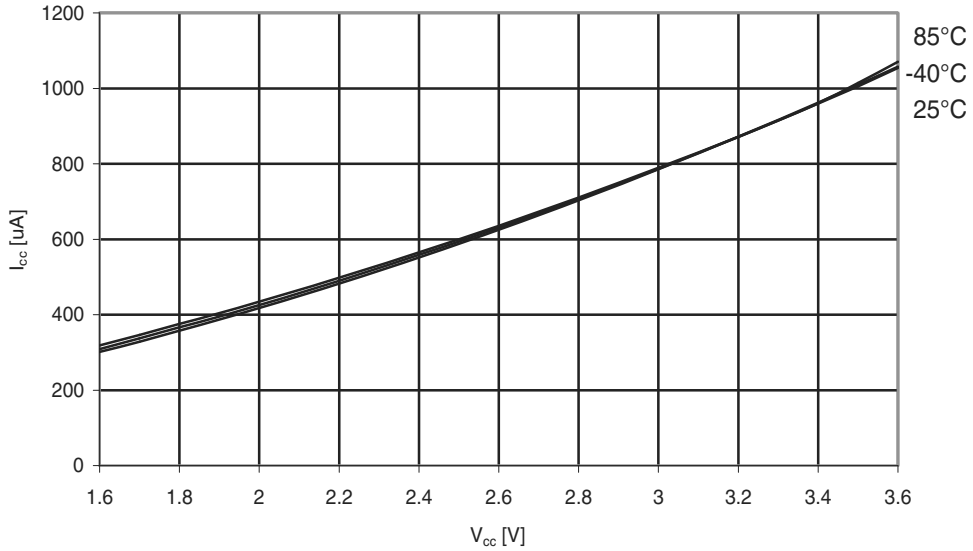


Figure 35-2. Active Supply Current vs. V_{CC}

f_{SYS} = 1.0 MHz



35.7 Bod Thresholds

Figure 35-15.BOD Thresholds vs. Temperature

BOD Level = 1.6V

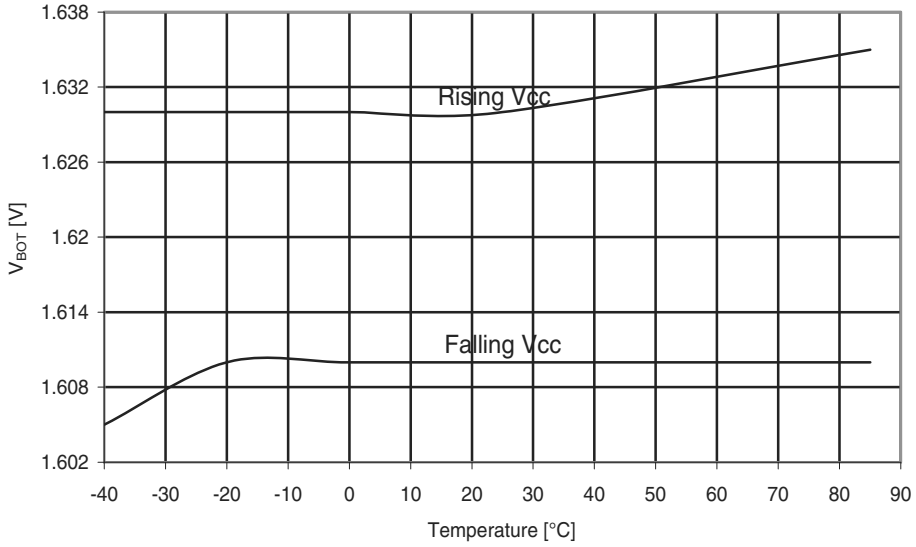
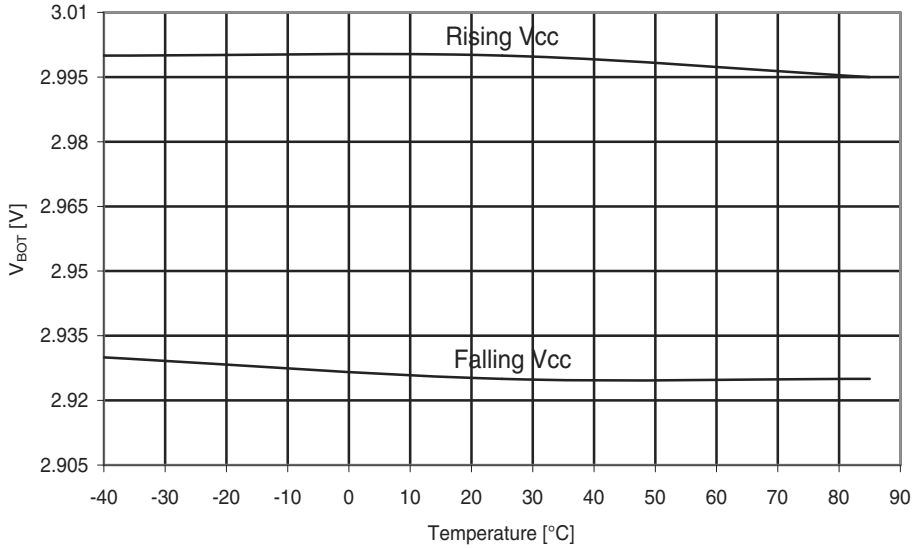


Figure 35-16.BOD Thresholds vs. Temperature

BOD Level = 2.9V



None.

8. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

9. The input difference between two succeeding ADC samples is limited by VREF

If the difference in input between two samples changes more than the size of the reference, the ADC will not be able to convert the data correctly. Two conversions will be required before the conversion is correct.

Problem fix/Workaround

Discard the first conversion if input is changed more than VREF, or ensure that the input never changes more then VREF.

10. Increased noise when using internal 1.0V reference at low temperature

When operating at below 0°C and using internal 1.0V reference the RMS noise will be up 4 LSB, Peak-to-peak noise up to 25 LSB.

Problem fix/Workaround

Use averaging to remove noise.

11. Configuration of PGM and CWCM not as described in XMEGA A Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

12 PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

- ±200 LSB for Sample and Hold mode

Problem fix/Workaround

None, avoid using a voltage reference above 2.4V.

4. ADC gain stage output range is limited to 2.4 V

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

–	1x	gain:	2.4	V
–	2x	gain:	1.2	V
–	4x	gain:	0.6	V
–	8x	gain:	300	mV
–	16x	gain:	150	mV
–	32x	gain:	75	mV
–	64x	gain:	38	mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4 V in order to get a correct result, or keep ADC voltage reference below 2.4 V.

5. The ADC has up to ±2 LSB inaccuracy

The ADC will have up to ±2 LSB inaccuracy, visible as a saw-tooth pattern on the input voltage/ output value transfer function of the ADC. The inaccuracy increases with increasing voltage reference reaching ±2 LSB with 3V reference.

Problem fix/Workaround

None, the actual ADC resolution will be reduced with up to ±2 LSB.

6. TWI, a general address call will match independent of the R/W-bit value

When the TWI is in Slave mode and a general address call is issued on the bus, the TWI Slave will get an address match regardless of the R/W-bit (ADDR[0] bit) value in the Slave Address Register.

Problem fix/Workaround

Use software to check the R/W-bit on general call address match.

17. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workarund

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

18. Inverted I/O enable does not affect Analog Comparator Output

The inverted I/O pin function does not affect the Analog Comparator output function.

Problem fix/Workarund

Configure the analog comparator setup to give a inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and externel inverter to change polarity of Analog Comparator Output.

19. Both DFLLs and both oscillators has to be enabled for one to work

In order to use the automatic runtime calibration for the 2 MHz or the 32 MHz internal oscilla-tors, the DFLL for both oscillators and both oscillators has to be enabled for one to work.

Problem fix/Workarund

Enabled both DFLLs and oscillators when using automatic runtime calibration for one of the internal oscillators.

37. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

37.1 8067O – 06/2013

1.	Not recommended for new designs - Use XMEGA A1U series.

37.2 8067N – 03/2013

1.	Removed all references to ATxmega192A1, ATxmega256A1 and ATxmega384A1.
2.	Updated module description. Based on the XMEGA A1U device datasheet.
3.	Updated analog comparator (AC) overview, Figure 28-1 on page 53.
4.	Updated “ADC Characteristics” on page 76.
5	Updated page erase time in “Flash and EEPROM Memory Characteristics” on page 76.
6	Updated Output low voltage conditions from I_{OH} to I_{OL} in “PAD Characteristics” on page 79.
7.	Removed TBDs from: “DC Characteristics” on page 73. “DAC Characteristics” on page 78. “Bandgap Characteristics” on page 78.
8.	Updated “Errata” on page 96 to be valid for both ATxmega64A1 and ATxmega128A1.
9.	Removed Boundary Scan Order table.

37.3 8067M – 09/2010

1.	Updated Errata “ATxmega64A1and ATxmega128A1 rev. H” on page 96

37.4 8067L – 08/2010

1.	Removed Footnote 3 of Figure 2-1 on page 3
2.	Updated “Features” on page 32. Event Channel 0 output on port pin 7
3.	Updated “DC Characteristics” on page 73, by adding I_{CC} for Flash/EEPROM Programming.
4.	Added AVCC in “ADC Characteristics” on page 76.
5.	Updated Start up time in “ADC Characteristics” on page 76.