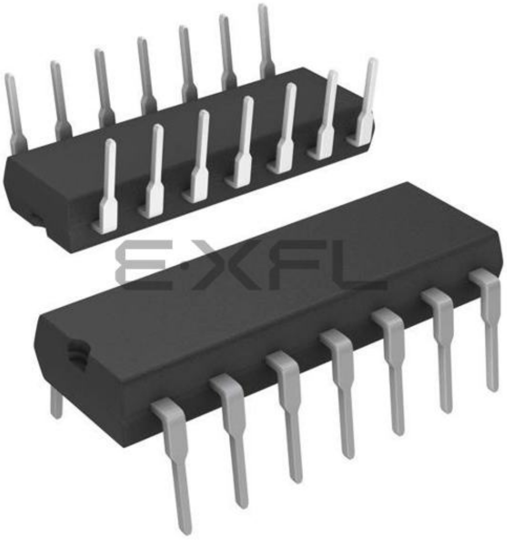

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c505-04e-p

1.0 GENERAL DESCRIPTION

The PIC16C505 from Microchip Technology is a low-cost, high-performance, 8-bit, fully static, EPROM/ ROM-based CMOS microcontroller. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (200 μs) except for program branches, which take two cycles. The PIC16C505 delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C505 product is equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are five oscillator configurations to choose from, including INTRC internal oscillator mode and the power-saving LP (Low Power) oscillator mode. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC16C505 is available in the cost-effective One-Time-Programmable (OTP) version, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C505 product is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16C505 fits in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The EPROM technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller perfect for applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16C505 very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic and PLD's in larger systems, and coprocessor applications).

4.0 MEMORY ORGANIZATION

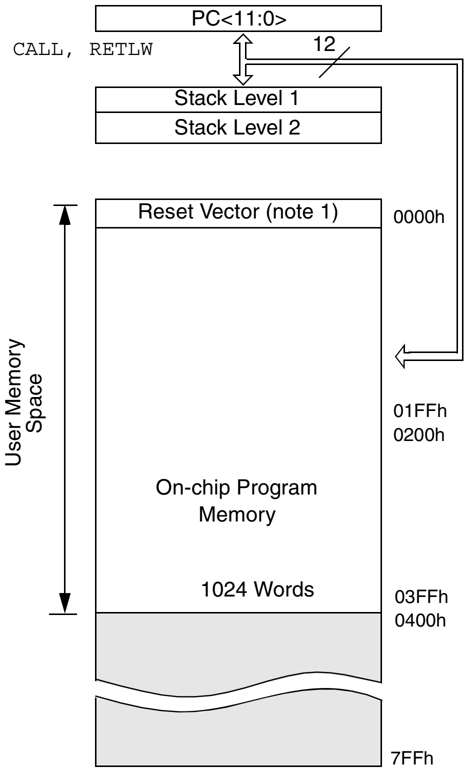
PIC16C505 memory is organized into program memory and data memory. For the PIC16C505, a paging scheme is used. Program memory pages are accessed using one STATUS register bit. Data memory banks are accessed using the File Select Register (FSR).

4.1 Program Memory Organization

The PIC16C505 devices have a 12-bit Program Counter (PC).

The 1K x 12 (0000h-03FFh) for the PIC16C505 are physically implemented. Refer to Figure 4-1. Accessing a location above this boundary will cause a wrap-around within the first 1K x 12 space. The effective reset vector is at 0000h, (see Figure 4-1). Location 03FFh contains the internal clock oscillator calibration value. This value should never be overwritten.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C505



Note 1: Address 0000h becomes the effective reset vector. Location 03FFh contains the `MOVLW XX` INTERNAL RC oscillator calibration value.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets(2)
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								`xxxx xxxx`	`uuuu uuuu`
01h	TMR0	8-bit real-time clock/counter								`xxxx xxxx`	`uuuu uuuu`
02h(1)	PCL	Low order 8 bits of PC								`1111 1111`	`1111 1111`
03h	STATUS	RBWUF	—	PAO	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	`0001 1xxx`	`q00q quuu`(1)
04h	FSR	Indirect data memory address pointer								`110x xxxx`	`11uu uuuu`
05h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	`1000 00--`	`uuuu uu--`
N/A	TRISB	—	—	I/O control registers						`--11 1111`	`--11 1111`
N/A	TRISC	—	—	I/O control registers						`--11 1111`	`--11 1111`
N/A	OPTION	$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	TOCS	TOSE	PSA	PS2	PS1	PS0	`1111 1111`	`1111 1111`
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	`--xx xxxx`	`--uu uuuu`
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	`--xx xxxx`	`--uu uuuu`

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If reset was due to wake-up on pin change, then bit 7 = 1. All other rests will cause bit 7 = 0.

Note 2: Other (non-power-up) resets include external reset through $\overline{\text{MCLR}}$, watchdog timer and wake-up on pin change reset.

4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register, which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<7:0> bits.

Note:	If TRIS bit is set to ‘0’, the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides OPTION control of $\overline{\text{RBPU}}$ and $\overline{\text{RBWU}}$).

REGISTER 4-2: OPTION REGISTER

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

bit 7: **$\overline{\text{RBWU}}$:** Enable wake-up on pin change (RB0, RB1, RB3, RB4)
`1` = Disabled
`0` = Enabled

bit 6: **$\overline{\text{RBPU}}$**: Enable weak pull-ups (RB0, RB1, RB3, RB4)
`1` = Disabled
`0` = Enabled

bit 5: **T0CS**: Timer0 clock source select bit
`1` = Transition on T0CKI pin (overrides TRIS <RC57>
`0` = Transition on internal instruction cycle clock, Fosc/4

bit 4: **T0SE**: Timer0 source edge select bit
`1` = Increment on high to low transition on the T0CKI pin
`0` = Increment on low to high transition on the T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
`1` = Prescaler assigned to the WDT
`0` = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>:** Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
`000`	1 : 2	1 : 1
`001`	1 : 4	1 : 2
`010`	1 : 8	1 : 4
`011`	1 : 16	1 : 8
`100`	1 : 32	1 : 16
`101`	1 : 64	1 : 32
`110`	1 : 128	1 : 64
`111`	1 : 256	1 : 128

4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the internal 4 MHz oscillator. It contains six bits for calibration

Note: Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part, so it can be reprogrammed correctly later.

After you move in the calibration constant, do not change the value. See Section 7.2.5

REGISTER 4-3: OSCCAL REGISTER (ADDRESS 05h) PIC16C505

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

bit 7-2: **CAL<5:0>:** Calibration

bit 1-0: Unimplemented read as ‘0’

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

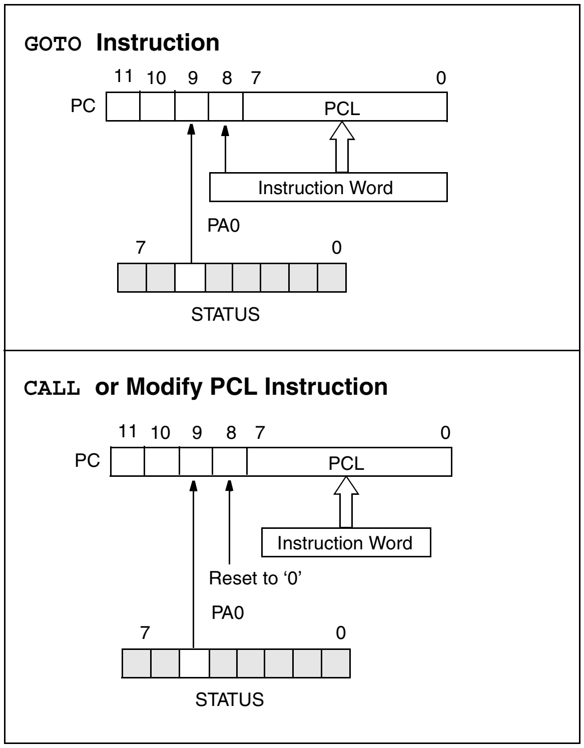
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-3).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-3).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC,5.

Note:	Because PC<8> is cleared in the CALL instruction or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-3: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C505



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the oscillator calibration instruction.) After executing MOVLW XX, the PC will roll over to location 00h and begin executing user code.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

PIC16C505 devices have a 12-bit wide hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Note 1:	There are no STATUS bits to indicate stack overflows or stack underflow conditions.
Note 2:	There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETLW, and instructions.

4.8 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

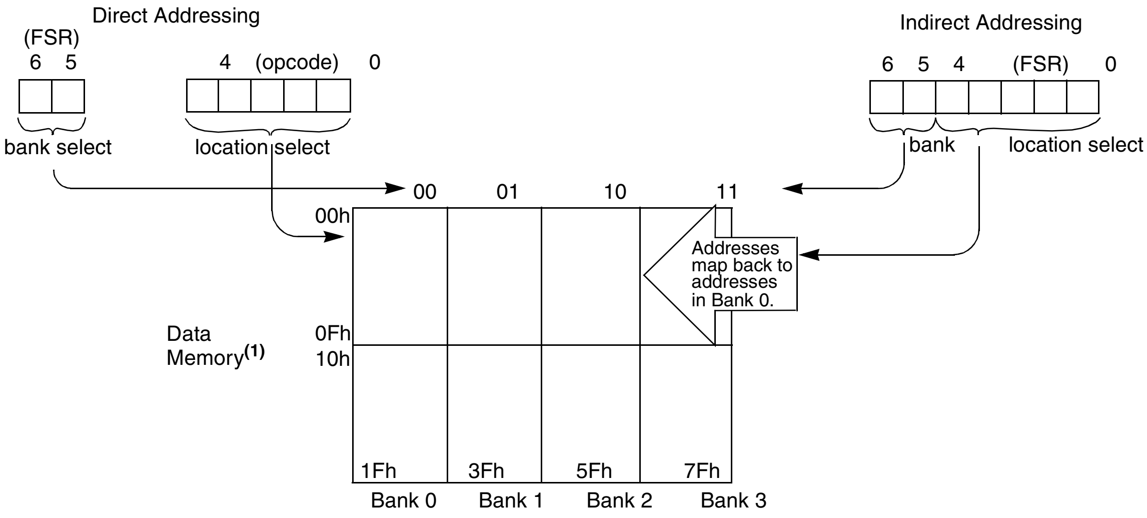
```
            movlw   0x10    ;initialize pointer
            movwf   FSR     ; to RAM
NEXT        clrf    INDF    ;clear INDF register
            incf    FSR,F   ;inc pointer
            btfsc   FSR,4   ;all done?
            goto    NEXT    ;NO, clear next
CONTINUE
            :               ;YES, continue
            :
```

The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

The device uses FSR<6:5> to select between banks 0:3.

FIGURE 4-4: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Section 4.2.

6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

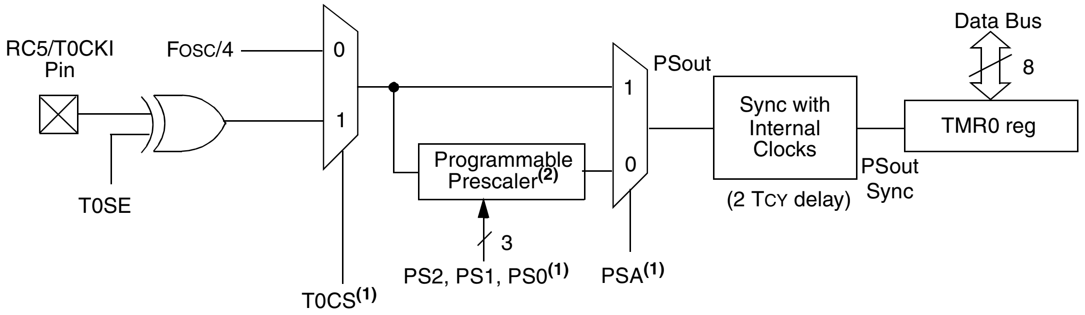
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

7.2.5 INTERNAL 4 MHz RC OSCILLATOR

The internal RC oscillator provides a fixed 4 MHz (nominal) system clock at V_{DD} = 5V and 25°C, see Electrical Specifications section for information on variation over voltage and temperature.

In addition, a calibration instruction is programmed into the last address of memory, which contains the calibration value for the internal RC oscillator. This location is always protected, regardless of the code protect settings. This value is programmed as a `MOVLW XX` instruction where XX is the calibration value, and is placed at the reset vector. This will load the W register with the calibration value upon reset and the PC will then roll over to the users program at address 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

OSCCAL, when written to with the calibration value, will "trim" the internal oscillator to remove process variation from the oscillator frequency.

> **Note:** Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part so it can be reprogrammed correctly later.

For the PIC16C505, only bits <7:2> of OSCCAL are implemented.

7.3 RESET

The device differentiates between various kinds of reset:

a) Power on reset (POR)

b) $\overline{\text{MCLR}}$ reset during normal operation

c) $\overline{\text{MCLR}}$ reset during SLEEP

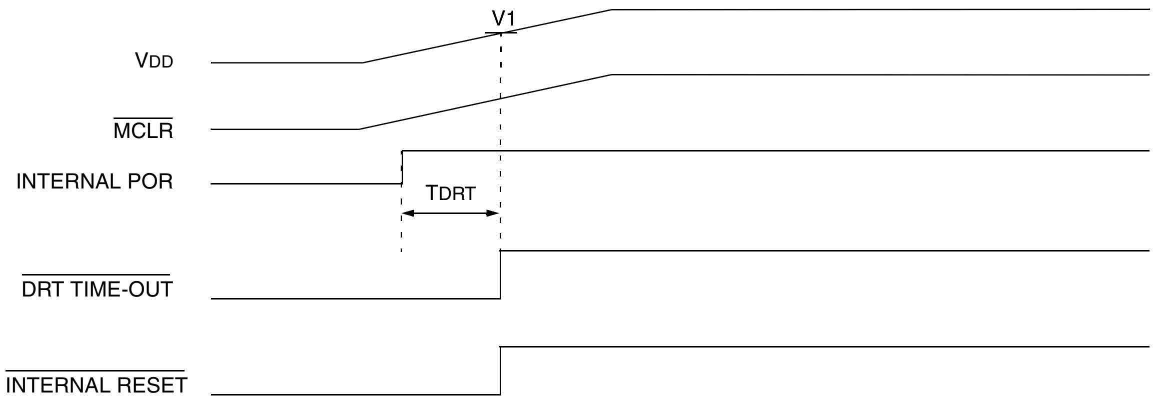
d) WDT time-out reset during normal operation

e) WDT time-out reset during SLEEP

f) Wake-up from SLEEP on pin change

Some registers are not reset in any way, they are unknown on POR and unchanged in any other reset. Most other registers are reset to "reset state" on power-on reset (POR), $\overline{\text{MCLR}}$, WDT or wake-up on pin change reset during normal operation. They are not affected by a WDT reset during SLEEP or $\overline{\text{MCLR}}$ reset during SLEEP, since these resets are viewed as resumption of normal operation. The exceptions to this are $\overline{\text{TO}}$, $\overline{\text{PD}}$ and RBWUF bits. They are set or cleared differently in different reset situations. These bits are used in software to determine the nature of reset. See Table 7-3 for a full description of reset states of all registers.

FIGURE 7-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD): SLOW VDD RISE TIME



Note: When VDD rises slowly, the TDRT time-out expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ VDD min.

7.5 Device Reset Timer (DRT)

In the PIC16C505, the DRT runs any time the device is powered up. DRT runs from RESET and varies based on oscillator selection and reset type (see Table 7-5).

The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min. and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after $\overline{\text{MCLR}}$ has reached a logic high ($V_{IH}\overline{\text{MCLR}}$) level. Thus, programming RB3/$\overline{\text{MCLR}}$/VPP as $\overline{\text{MCLR}}$ and using an external RC network connected to the $\overline{\text{MCLR}}$ input is not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the RB3/$\overline{\text{MCLR}}$/VPP pin as a general purpose input.

The Device Reset time delay will vary from chip to chip due to VDD, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake from SLEEP mode automatically.

Reset sources are POR, $\overline{\text{MCLR}}$, WDT time-out and Wake-up on pin change. (See Section 7.9.2, Notes 1, 2, and 3, page 37.)

7.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the external RC oscillator of the RB5/OSC1/CLKIN pin and the internal 4 MHz oscillator. That means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a `SLEEP` instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 7.1). Refer to the PIC16C505 Programming Specifications to determine how to access the configuration word.

TABLE 7-5: DRT (DEVICE RESET TIMER PERIOD)

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)	300 μs (typical)
HS, XT & LP	18 ms (typical)	18 ms (typical)

COMF Complement f

Syntax: [*label*] COMF f,d

Operands: $0 \leq f \leq 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow$ (dest)

Status Affected: Z

Encoding:

0010	01df	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:

```
COMF    REG1,0
```

Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
W = 0xEC

DECF Decrement f

Syntax: [*label*] DECF f,d

Operands: $0 \leq f \leq 31$
$d \in [0,1]$

Operation: (f) – 1 → (dest)

Status Affected: Z

Encoding:

0000	11df	ffff

Description: Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:

```
DECF    CNT,   1
```

Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ Decrement f, Skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: $0 \leq f \leq 31$
$d \in [0,1]$

Operation: (f) – 1 → d; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example:

```
HERE      DECFSZ   CNT, 1
          GOTO     LOOP
CONTINUE  •
          •
          •
```

Before Instruction
PC = address (HERE)

After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE+1)

GOTO Unconditional Branch

Syntax: [*label*] GOTO k

Operands: $0 \leq k \leq 511$

Operation: k → PC<8:0>;
STATUS<6:5> → PC<10:9>

Status Affected: None

Encoding:

101k	kkkk	kkkk

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Example:

```
GOTO THERE
```

After Instruction
PC = address (THERE)

9.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

9.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip’s next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

9.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

9.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user’s guide, lessons, tutorial, compiler and MPLAB IDE software.

10.2 DC CHARACTERISTICS: PIC16LC505-04 (Commercial, Industrial)

DC Characteristics Power Supply Pins							**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)
Parm. No.	**Characteristic**	**Sym**	**Min**	**Typ[(1)]**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	2.5	—	5.5	V	See Figure 10-1 through Figure 10-3
D002	RAM Data Retention Voltage[(2)]	VDR	—	1.5*	—	V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See section on Power-on Reset for details
D010	Supply Current[(3)]	IDD	— — —	0.8 0.4 15	1.4 0.8 23	mA mA µA	FOSC = 4MHz, VDD = 5.5V, WDT disabled (Note 4)* FOSC = 4MHz, VDD = 2.5V, WDT disabled (Note 4) FOSC = 32kHz, VDD = 2.5V, WDT disabled (Note 6)
D020	Power-Down Current [(5)]	IPD	— — —	0.25 0.25 3	3 4 8	µA µA µA	VDD = 2.5V (Note 6) VDD = 3.0V * (Note 6) VDD = 5.5V Industrial
D022	WDT Current[(5)]	ΔIWDT	—	2.0	4	µA	VDD = 2.5V (Note 6)
1A	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency	FOSC	0 0 0 0	— — — —	200 4 4 4	kHz MHz MHz MHz	All temperatures All temperatures All temperatures All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

6: Commercial temperature range only.

10.3 DC CHARACTERISTICS: PIC16C505-04 (Commercial, Industrial, Extended)
PIC16C505-20(Commercial, Industrial, Extended)
PIC16LC505-04 (Commercial, Industrial)

DC CHARACTERISTICS	**Standard Operating Conditions (unless otherwise specified)** Operating temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC spec Section 10.1 and Section 10.3.

Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	—	0.8V	V	For all 4.5 ≤ VDD ≤ 5.5V
D030A			VSS	—	0.15VDD	V	otherwise
D031	with Schmitt Trigger buffer		VSS	—	0.2VDD	V	
D032	MCLR, RC5/T0CKI (in EXTRC mode)		VSS	—	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	—	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		—			
D040	with TTL buffer		2.0	—	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8VDD	—	VDD	V	otherwise
D041	with Schmitt Trigger buffer		0.8VDD	—	VDD	V	For entire VDD range
D042	MCLR, RC5/T0CKI		0.8VDD	—	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	—	VDD	V	Note1
D043	OSC1 (in EXTRC mode)		0.9VDD	—	VDD	V	
D070	GPIO weak pull-up current (Note 4)	IPUR	50	250	400	μA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	—	—	±1	μA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	GP3/$\overline{\text{MCLR}}$I (Note 5)		—	—	±30	μA	Vss ≤ VPIN ≤ VDD
D061A	GP3/$\overline{\text{MCLR}}$I (Note 6)		—	—	±5	μA	Vss ≤ VPIN ≤ VDD
D063	OSC1		—	—	±5	μA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports/CLKOUT	VOL	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, –40°C to +85°C
D080A			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, –40°C to +125°C
D083	OSC2		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, –40°C to +85°C
D083A			—	—	0.6	V	IOL = 1.2 mA, VDD = 4.5V, –40°C to +125°C

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C505 be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Does not include GP3. For GP3 see parameters D061 and D061A.

5: This spec. applies to GP3/$\overline{\text{MCLR}}$ configured as external $\overline{\text{MCLR}}$ and GP3/$\overline{\text{MCLR}}$ configured as input with internal pull-up enabled.

6: This spec. applies when GP3/$\overline{\text{MCLR}}$ is configured as an input with pull-up disabled. The leakage current of the $\overline{\text{MCLR}}$ circuit is higher than the standard I/O logic.

TABLE 10-1: PULL-UP RESISTOR RANGES - PIC16C505

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
RB0/RB1/RB4					
2.5	–40	38K	42K	63K	W
	25	42K	48K	63K	W
	85	42K	49K	63K	W
	125	50K	55K	63K	W
5.5	–40	15K	17K	20K	W
	25	18K	20K	23K	W
	85	19K	22K	25K	W
	125	22K	24K	28K	W
RB3					
2.5	–40	285K	346K	417K	W
	25	343K	414K	532K	W
	85	368K	457K	532K	W
	125	431K	504K	593K	W
5.5	–40	247K	292K	360K	W
	25	288K	341K	437K	W
	85	306K	371K	448K	W
	125	351K	407K	500K	W

* These parameters are characterized but not tested.

10.4 Timing Parameter Symbology and Load Conditions - PIC16C505

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

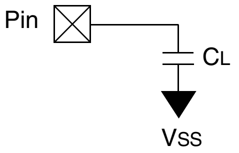
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 10-4: LOAD CONDITIONS - PIC16C505



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

TABLE 11-1: DYNAMIC IDD (TYPICAL) - WDT ENABLED, 25°C

Oscillator	Frequency	VDD = 3.0V[1]	VDD = 5.5V
External RC	4 MHz	240 µA[2]	800 µA[2]
Internal RC	4 MHz	320 µA	800 µA
XT	4 MHz	300 µA	800 µA
LP	32 kHz	19 µA	50 µA
HS	20 MHz	N/A	4.5 mA

Note 1: LP oscillator based on VDD = 2.5V

2: Does not include current through external R&C.

FIGURE 11-3: WDT TIMER TIME-OUT PERIOD vs. VDD

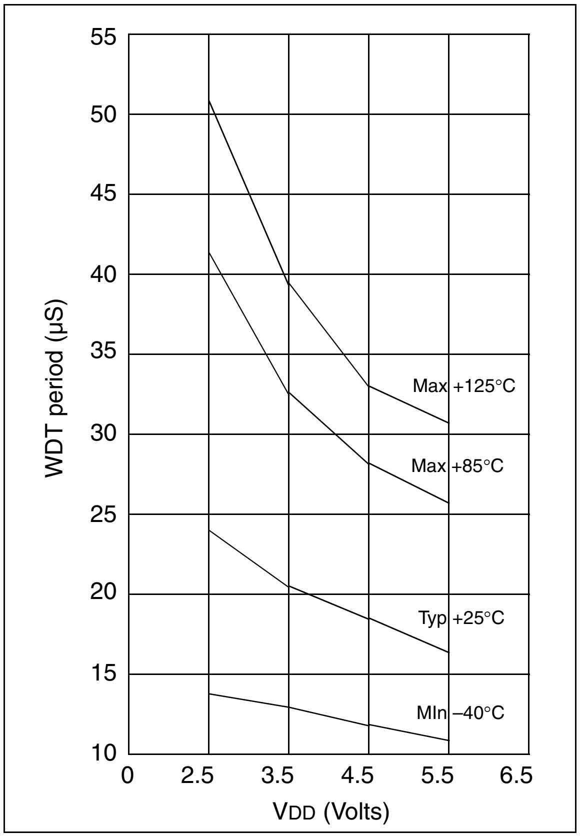
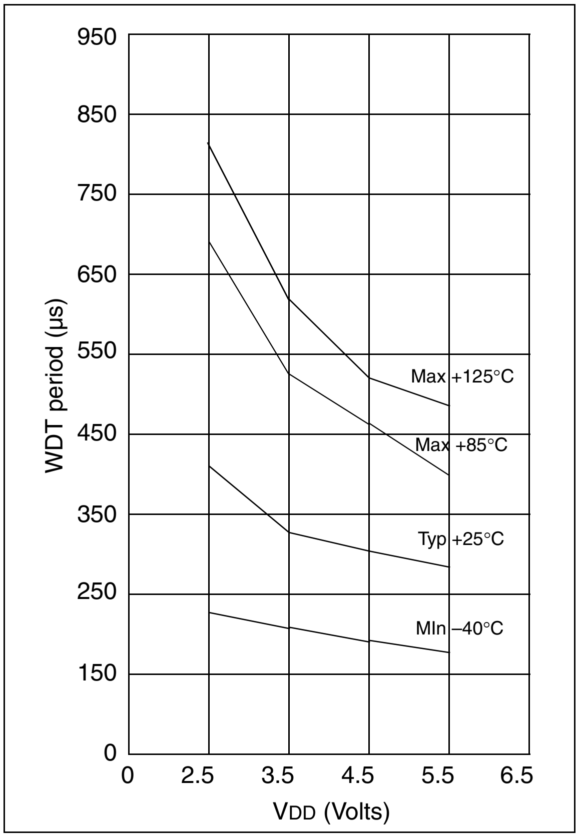


FIGURE 11-4: SHORT DRT PERIOD VS. VDD



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