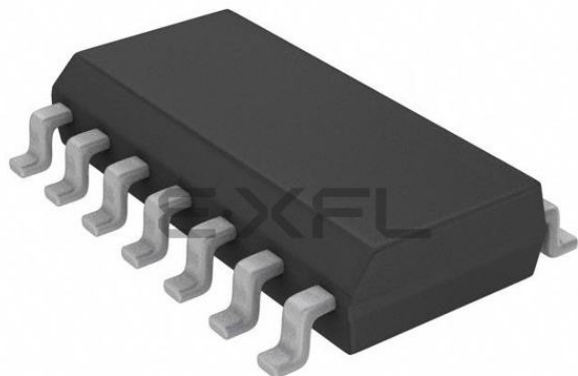




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c505t-04i-sl

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets ⁽²⁾
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	RBWUF	—	PAO	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	q00q quuu ⁽¹⁾
04h	FSR	Indirect data memory address pointer								110x xxxx	11uu uuuu
05h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--	uuuu uu--
N/A	TRISB	—	—	I/O control registers						--11 1111	--11 1111
N/A	TRISC	—	—	I/O control registers						--11 1111	--11 1111
N/A	OPTION	$\overline{RBWU}$	$\overline{RBPu}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If reset was due to wake-up on pin change, then bit 7 = 1. All other resets will cause bit 7 = 0.

Note 2: Other (non-power-up) resets include external reset through MCLR, watchdog timer and wake-up on pin change reset.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRISB	—	—	I/O control registers						--11 1111	--11 1111
N/A	TRISC	—	—	I/O control registers						--11 1111	--11 1111
N/A	OPTION	RBWU	RBPU	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS	RBWUF	—	PAO	TO	PD	Z	DC	C	0001 1xxx	q00q quuu ⁽¹⁾
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If reset was due to wake-up on pin change, then bit 7 = 1. All other resets will cause bit 7 = 0.

5.5 I/O Programming Considerations

5.5.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORTB Settings
; PORTB<5:3> Inputs
; PORTB<2:0> Outputs
;
;                                PORTB latch  PORTB pins
;                                -----
BCF  PORTB, 5  ;--01 -ppp  --11 pppp
BCF  PORTB, 4  ;--10 -ppp  --11 pppp
MOVLW 007h    ;
TRIS  PORTB    ;--10 -ppp  --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;RB5 to be latched as the pin value (High).
```

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

7.2 Oscillator Configurations

7.2.1 OSCILLATOR TYPES

The PIC16C505 can be operated in four different oscillator modes. The user can program three configuration bits (FOSC<2:0>) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- HS: High Speed Crystal/Resonator
- INTRC: Internal 4 MHz Oscillator
- EXTRC: External Resistor/Capacitor

7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In HS, XT or LP modes, a crystal or ceramic resonator is connected to the RB5/OSC1/CLKIN and RB4/OSC2/CLKOUT pins to establish oscillation (Figure 7-1). The PIC16C505 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in HS, XT or LP modes, the device can have an external clock source drive the RB5/OSC1/CLKIN pin (Figure 7-2).

FIGURE 7-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)

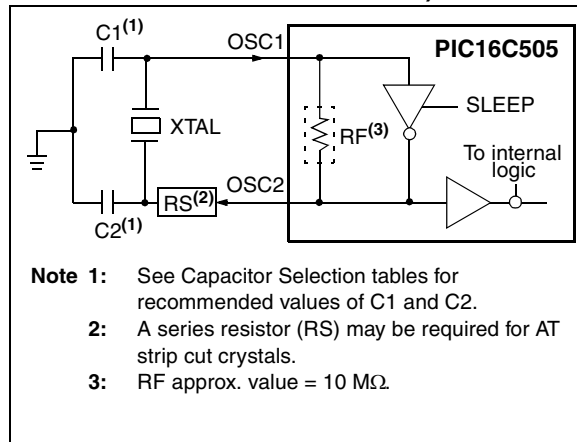


FIGURE 7-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

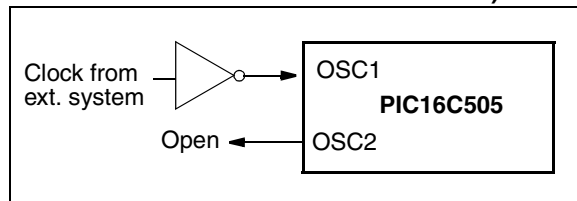


TABLE 7-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16C505

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	4.0 MHz	30 pF	30 pF
HS	16 MHz	10-47 pF	10-47 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C505

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	20 MHz	15-47 pF	15-47 pF

Note 1: For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

7.2.5 INTERNAL 4 MHz RC OSCILLATOR

The internal RC oscillator provides a fixed 4 MHz (nominal) system clock at $V_{DD} = 5V$ and $25^{\circ}C$, see Electrical Specifications section for information on variation over voltage and temperature.

In addition, a calibration instruction is programmed into the last address of memory, which contains the calibration value for the internal RC oscillator. This location is always protected, regardless of the code protect settings. This value is programmed as a `MOVLW XX` instruction where XX is the calibration value, and is placed at the reset vector. This will load the W register with the calibration value upon reset and the PC will then roll over to the users program at address 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

OSCCAL, when written to with the calibration value, will “trim” the internal oscillator to remove process variation from the oscillator frequency.

Note: Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part so it can be reprogrammed correctly later.
--

For the PIC16C505, only bits <7:2> of OSCCAL are implemented.

7.3 RESET

The device differentiates between various kinds of reset:

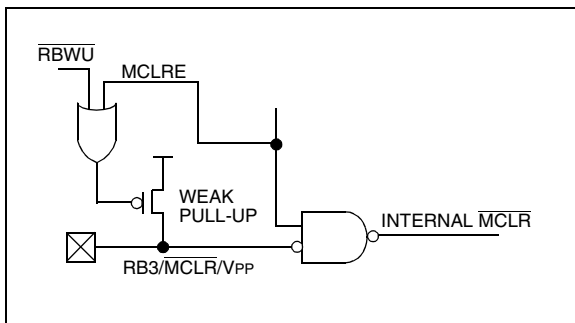
- a) Power on reset (POR)
- b) $\overline{MCLR}$ reset during normal operation
- c) $\overline{MCLR}$ reset during SLEEP
- d) WDT time-out reset during normal operation
- e) WDT time-out reset during SLEEP
- f) Wake-up from SLEEP on pin change

Some registers are not reset in any way, they are unknown on POR and unchanged in any other reset. Most other registers are reset to “reset state” on power-on reset (POR), $\overline{MCLR}$, WDT or wake-up on pin change reset during normal operation. They are not affected by a WDT reset during SLEEP or $\overline{MCLR}$ reset during SLEEP, since these resets are viewed as resumption of normal operation. The exceptions to this are TO, PD and RBWUF bits. They are set or cleared differently in different reset situations. These bits are used in software to determine the nature of reset. See Table 7-3 for a full description of reset states of all registers.

7.3.1 $\overline{\text{MCLR}}$ ENABLE

This configuration bit when unprogrammed (left in the '1' state) enables the external $\overline{\text{MCLR}}$ function. When programmed, the $\overline{\text{MCLR}}$ function is tied to the internal VDD, and the pin is assigned to be a I/O. See Figure 7-6.

FIGURE 7-6: $\overline{\text{MCLR}}$ SELECT



7.4 Power-On Reset (POR)

The PIC16C505 family incorporates on-chip Power-On Reset (POR) circuitry, which provides an internal chip reset for most power-up situations.

The on chip POR circuit holds the chip in reset until VDD has reached a high enough level for proper operation. To take advantage of the internal POR, program the RB3/ $\overline{\text{MCLR}}$ /VPP pin as $\overline{\text{MCLR}}$ and tie through a resistor to VDD or program the pin as RB3. An internal weak pull-up resistor is implemented using a transistor. Refer to Table 10-1 for the pull-up resistor ranges. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 7-7.

The Power-On Reset circuit and the Device Reset Timer (Section 7.5) circuit are closely related. On power-up, the reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms, it will reset the reset latch and thus end the on-chip reset signal.

A power-up example where $\overline{\text{MCLR}}$ is held low is shown in Figure 7-8. VDD is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of reset TDRT msec after $\overline{\text{MCLR}}$ goes high.

In Figure 7-9, the on-chip Power-On Reset feature is being used ($\overline{\text{MCLR}}$ and VDD are tied together or the pin is programmed to be RB3.). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. However, Figure 7-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that $\overline{\text{MCLR}}$ is high and when $\overline{\text{MCLR}}$ and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 7-9).

Note: When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information refer to Application Notes "Power-Up Considerations" - AN522 and "Power-up Trouble Shooting" - AN607.

8.0 INSTRUCTION SET SUMMARY

Each PIC16C505 instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC16C505 instruction set summary in Table 8-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 8-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 8-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-Out bit
$\overline{PD}$	Power-Down bit
dest	Destination, either the W register or the specified register file location
[]	Options
()	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s.

Figure 8-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 8-1: GENERAL FORMAT FOR INSTRUCTIONS

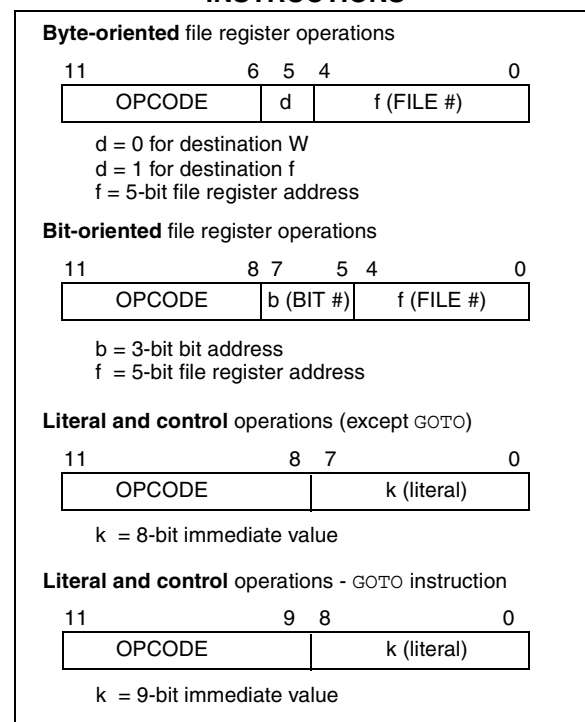


TABLE 8-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands	Description	Cycles	12-Bit Opcode			Status Affected	Notes
			MSb	LSb			
ADDWF f,d	Add W and f	1	0001	11df	ffff	C,DC,Z	1,2,4
ANDWF f,d	AND W with f	1	0001	01df	ffff	Z	2,4
CLRF f	Clear f	1	0000	011f	ffff	Z	4
CLRW —	Clear W	1	0000	0100	0000	Z	
COMF f,d	Complement f	1	0010	01df	ffff	Z	
DECF f,d	Decrement f	1	0000	11df	ffff	Z	2,4
DECFSZ f,d	Decrement f, Skip if 0	1(2)	0010	11df	ffff	None	2,4
INCF f,d	Increment f	1	0010	10df	ffff	Z	2,4
INCFSZ f,d	Increment f, Skip if 0	1(2)	0011	11df	ffff	None	2,4
IORWF f,d	Inclusive OR W with f	1	0001	00df	ffff	Z	2,4
MOVF f,d	Move f	1	0010	00df	ffff	Z	2,4
MOVWF f	Move W to f	1	0000	001f	ffff	None	1,4
NOP —	No Operation	1	0000	0000	0000	None	
RLF f,d	Rotate left f through Carry	1	0011	01df	ffff	C	2,4
RRF f,d	Rotate right f through Carry	1	0011	00df	ffff	C	2,4
SUBWF f,d	Subtract W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
SWAPF f,d	Swap f	1	0011	10df	ffff	None	2,4
XORWF f,d	Exclusive OR W with f	1	0001	10df	ffff	Z	2,4
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF f,b	Bit Clear f	1	0100	bbbf	ffff	None	2,4
BSF f,b	Bit Set f	1	0101	bbbf	ffff	None	2,4
BTFSC f,b	Bit Test f, Skip if Clear	1 (2)	0110	bbbf	ffff	None	
BTFSS f,b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS							
ANDLW k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL k	Call subroutine	2	1001	kkkk	kkkk	None	1
CLRWDT k	Clear Watchdog Timer	1	0000	0000	0100	$\overline{TO}$, $\overline{PD}$	
GOTO k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION —	Load OPTION register	1	0000	0000	0010	None	
RETLW k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP —	Go into standby mode	1	0000	0000	0011	$\overline{TO}$, $\overline{PD}$	
TRIS f	Load TRIS register	1	0000	0000	0fff	None	3
XORLW k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for **GOTO**. (Section 4.6)

- When an I/O register is modified as a function of itself (e.g. **MOVF** $\text{PORTB}, 1$), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- The instruction **TRIS** f, where f = 6 causes the contents of the W register to be written to the tristate latches of **PORTB**. A '1' forces the pin to a hi-impedance state and disables the output buffers.
- If this instruction is executed on the **TMR0** register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to **TMR0**).

ADDWF Add W and f

Syntax: [*label*] ADDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) + (f) \rightarrow (\text{dest})$

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff
------	------	------

Description: Add the contents of the W register and register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ADDWF FSR, 0

Before Instruction

W = 0x17
 FSR = 0xC2

After Instruction

W = 0xD9
 FSR = 0xC2

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .\text{AND.} (f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0001	01df	ffff
------	------	------

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ANDWF FSR, 1

Before Instruction

W = 0x17
 FSR = 0xC2

After Instruction

W = 0x17
 FSR = 0x02

ANDLW And literal with W

Syntax: [*label*] ANDLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) .\text{AND.} (k) \rightarrow (W)$

Status Affected: Z

Encoding:

1110	kkkk	kkkk
------	------	------

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: ANDLW 0x5F

Before Instruction

W = 0xA3

After Instruction

W = 0x03

BCF Bit Clear f

Syntax: [*label*] BCF f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: $0 \rightarrow (f)$

Status Affected: None

Encoding:

0100	bbbf	ffff
------	------	------

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example: BCF FLAG_REG, 7

Before Instruction

FLAG_REG = 0xC7

After Instruction

FLAG_REG = 0x47

IORLW Inclusive OR literal with W

Syntax: [*label*] IORLW *k*

Operands: $0 \leq k \leq 255$

Operation: (W) .OR. (k) $\rightarrow$ (W)

Status Affected: Z

Encoding:

1101	kkkk	kkkk
------	------	------

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: IORLW 0x35

Before Instruction

W = 0x9A

After Instruction

W = 0xBF

Z = 0

IORWF Inclusive OR W with f

Syntax: [*label*] IORWF *f*,*d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (W).OR. (f) $\rightarrow$ (dest)

Status Affected: Z

Encoding:

0001	00df	ffff
------	------	------

Description: Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: IORWF RESULT, 0

Before Instruction

RESULT = 0x13

W = 0x91

After Instruction

RESULT = 0x13

W = 0x93

Z = 0

MOVF Move f

Syntax: [*label*] MOVF *f*,*d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (f) $\rightarrow$ (dest)

Status Affected: Z

Encoding:

0010	00df	ffff
------	------	------

Description: The contents of register 'f' are moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' = 1 is useful as a test of a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example: MOVF FSR, 0

After Instruction

W = value in FSR register

MOVLW Move Literal to W

Syntax: [*label*] MOVLW *k*

Operands: $0 \leq k \leq 255$

Operation: *k* $\rightarrow$ (W)

Status Affected: None

Encoding:

1100	kkkk	kkkk
------	------	------

Description: The eight bit literal 'k' is loaded into the W register. The don't cares will assembled as 0s.

Words: 1

Cycles: 1

Example: MOVLW 0x5A

After Instruction

W = 0x5A

9.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C® for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICKit™ 3 Debug Express
- Device Programmers
 - PICKit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

9.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

10.2 DC CHARACTERISTICS: PIC16LC505-04 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature				
			0°C ≤ TA ≤ +70°C (commercial)				
			–40°C ≤ TA ≤ +85°C (industrial)				
Parm. No.	Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
D001	Supply Voltage	VDD	2.5	—	5.5	V	See Figure 10-1 through Figure 10-3
D002	RAM Data Retention Voltage ⁽²⁾	VDR	—	1.5*	—	V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See section on Power-on Reset for details
D010	Supply Current ⁽³⁾	IDD	—	0.8	1.4	mA	FOSC = 4MHz, VDD = 5.5V, WDT disabled (Note 4)*
			—	0.4	0.8	mA	FOSC = 4MHz, VDD = 2.5V, WDT disabled (Note 4)
			—	15	23	μA	FOSC = 32kHz, VDD = 2.5V, WDT disabled (Note 6)
D020	Power-Down Current ⁽⁵⁾	IPD	—	0.25	3	μA	VDD = 2.5V (Note 6)
			—	0.25	4	μA	VDD = 3.0V * (Note 6)
			—	3	8	μA	VDD = 5.5V Industrial
D022	WDT Current ⁽⁵⁾	ΔIWDI	—	2.0	4	μA	VDD = 2.5V (Note 6)
1A	LP Oscillator Operating Frequency	FOSC	0	—	200	kHz	All temperatures
	RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
	XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
	HS Oscillator Operating Frequency		0	—	4	MHz	All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula:

IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

6: Commercial temperature range only.

PIC16C505

FIGURE 10-6: I/O TIMING - PIC16C505

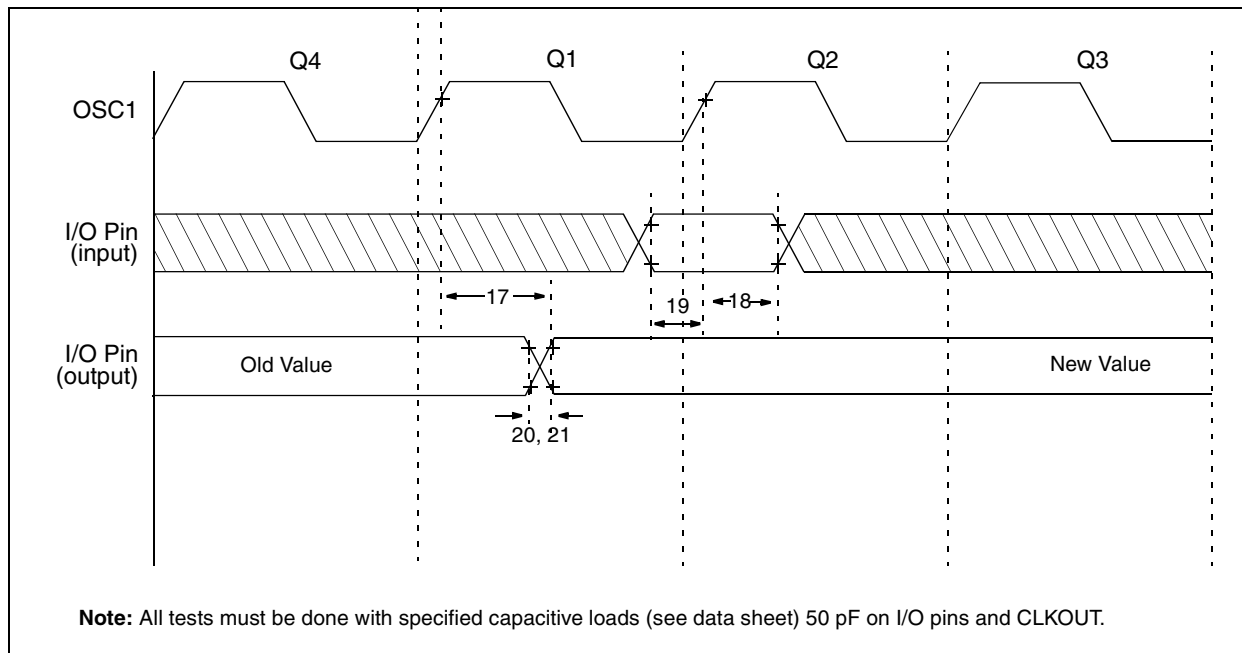


TABLE 10-4: TIMING REQUIREMENTS - PIC16C505

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature				
		0°C ≤ TA ≤ +70°C (commercial)				
		-40°C ≤ TA ≤ +85°C (industrial)				
		-40°C ≤ TA ≤ +125°C (extended)				
		Operating Voltage VDD range is described in Section 10.1				
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ^(2,3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) ⁽²⁾	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽³⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽³⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 10-4 for loading conditions.

11.0 DC AND AC CHARACTERISTICS - PIC16C505

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3 σ) and (mean - 3 σ) respectively, where σ is standard deviation.

FIGURE 11-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 5.0V) (INTERNAL RC IS CALIBRATED TO 25°C, 5.0V)

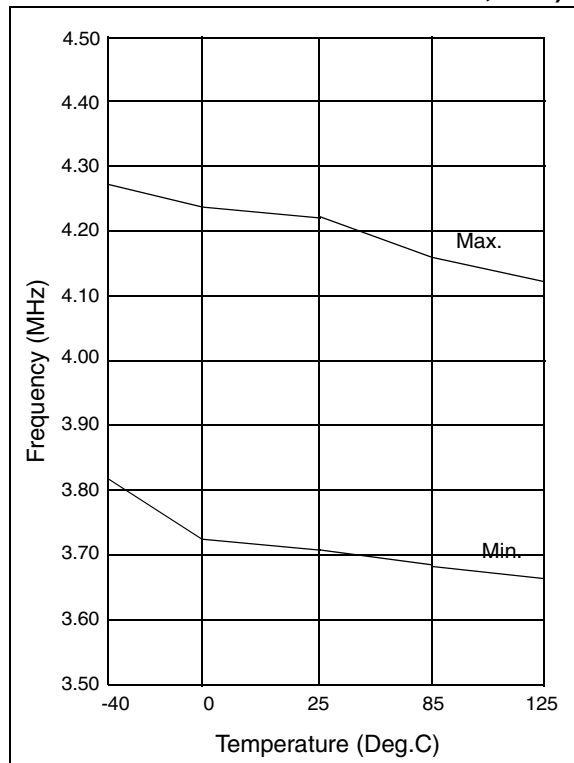
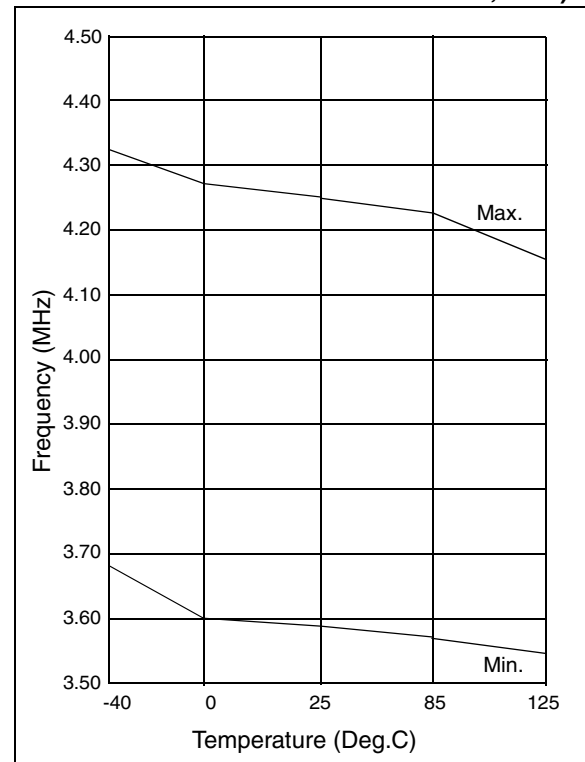


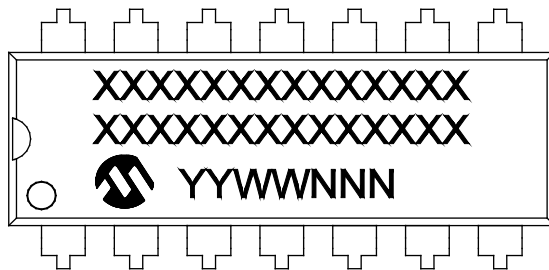
FIGURE 11-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 2.5V) (INTERNAL RC IS CALIBRATED TO 25°C, 5.0V)



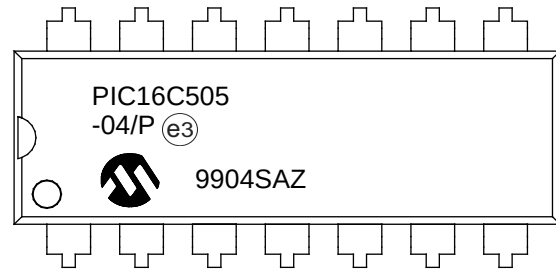
12.0 PACKAGING INFORMATION

12.1 Package Marking Information

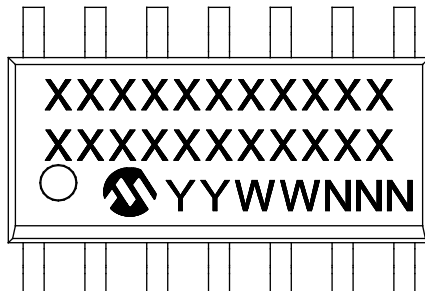
14-Lead PDIP (300 mil)



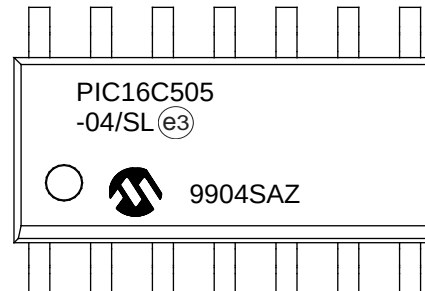
Example



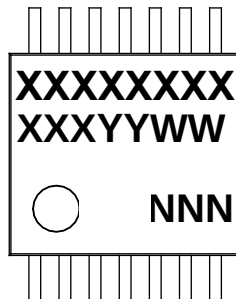
14-Lead SOIC (3.90 mm)



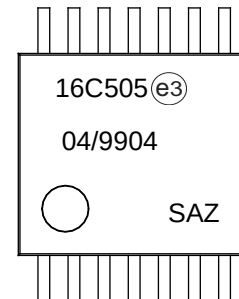
Example



14-Lead TSSOP (4.4 mm)



Example

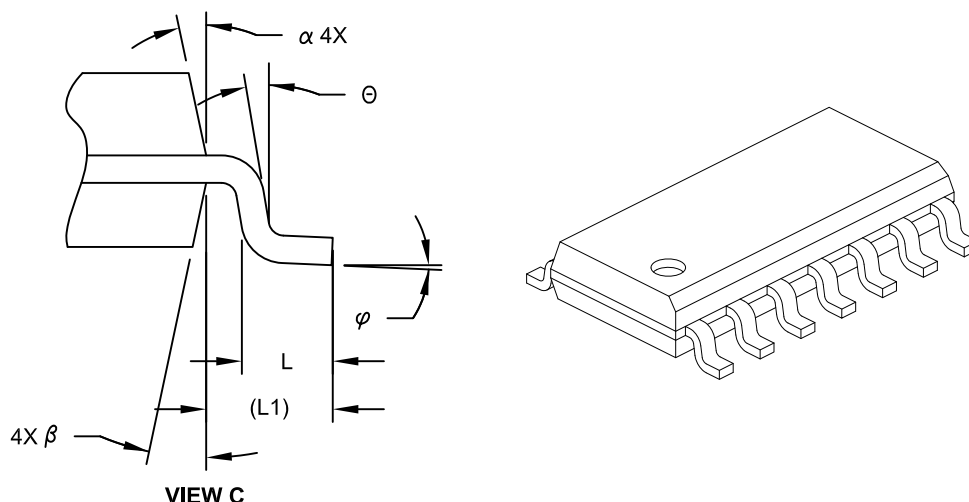


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

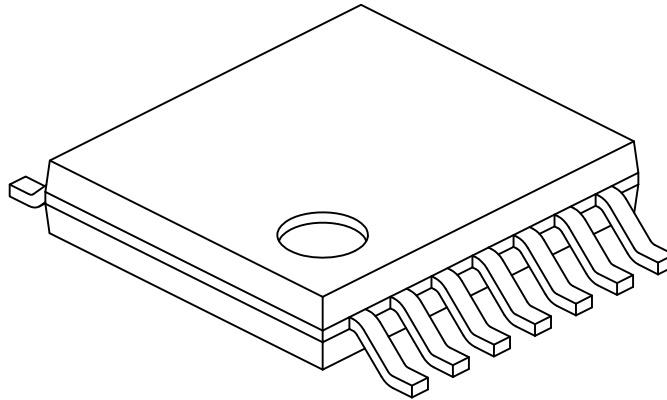
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)	1.00 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

PIC18F66K80 FAMILY

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PIC16C505

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