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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc505-04i-sl

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

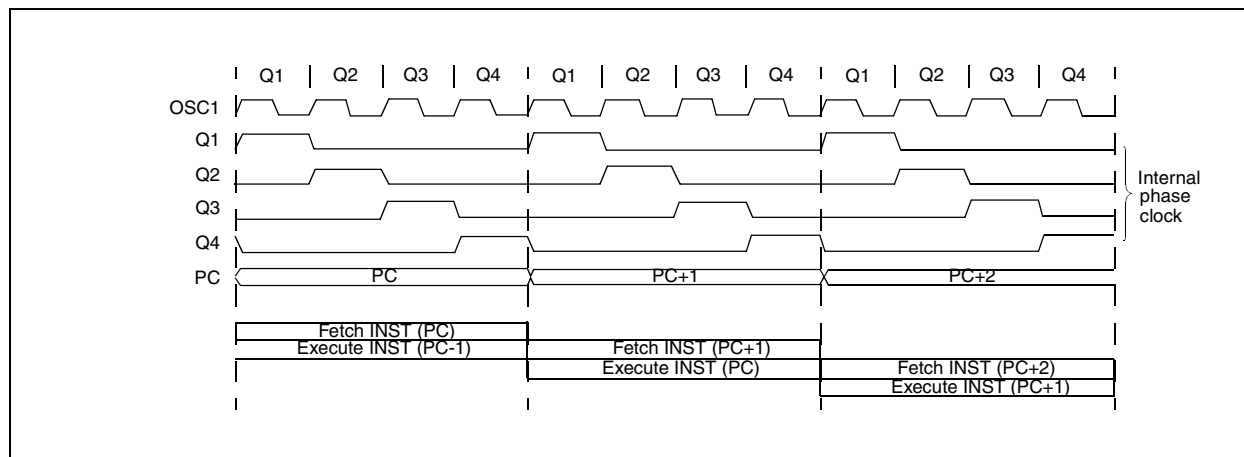
3.2 Instruction Flow/Pipelining

An Instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., `GOTO`) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

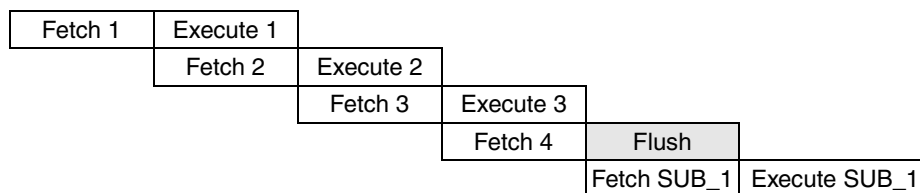
In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

```
1. MOVLW 03H
2. MOVWF PORTB
3. CALL SUB_1
4. BSF PORTB, BIT1
```



All instructions are single cycle, except for any program branches. These take two cycles, since the fetch instruction is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets ⁽²⁾
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	RBWUF	—	PAO	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	q00q quuu ⁽¹⁾
04h	FSR	Indirect data memory address pointer								110x xxxx	11uu uuuu
05h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--	uuuu uu--
N/A	TRISB	—	—	I/O control registers						--11 1111	--11 1111
N/A	TRISC	—	—	I/O control registers						--11 1111	--11 1111
N/A	OPTION	\overline{RBWU}	\overline{RBPu}	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If reset was due to wake-up on pin change, then bit 7 = 1. All other resets will cause bit 7 = 0.

Note 2: Other (non-power-up) resets include external reset through MCLR, watchdog timer and wake-up on pin change reset.

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register, because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Instruction Set Summary.

REGISTER 4-1: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
RBWUF	—	PA0	\overline{TO}	\overline{PD}	Z	DC	C
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **RBWUF**: I/O reset bit
1 = Reset due to wake-up from SLEEP on pin change
0 = After power up or other reset

bit 6: **Unimplemented**

bit 5: **PA0**: Program page preselect bits
1 = Page 1 (200h - 3FFh)
0 = Page 0 (000h - 1FFh)
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.

bit 4: **\overline{TO}** : Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **\overline{PD}** : Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/borrow bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/borrow bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)
ADDWF
1 = A carry occurred
0 = A carry did not occur
SUBWF
1 = A borrow did not occur
0 = A borrow occurred
RRF or RLF
Load bit with LSB or MSB, respectively

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRISB	—	—	I/O control registers						--11 1111	--11 1111
N/A	TRISC	—	—	I/O control registers						--11 1111	--11 1111
N/A	OPTION	RBWU	RBPU	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS	RBWUF	—	PAO	TO	PD	Z	DC	C	0001 1xxx	q00q quuu ⁽¹⁾
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If reset was due to wake-up on pin change, then bit 7 = 1. All other resets will cause bit 7 = 0.

5.5 I/O Programming Considerations

5.5.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```

;Initial PORTB Settings
; PORTB<5:3> Inputs
; PORTB<2:0> Outputs
;
;                                PORTB latch  PORTB pins
;                                -----
BCF  PORTB, 5  ;--01 -ppp  --11 pppp
BCF  PORTB, 4  ;--10 -ppp  --11 pppp
MOVLW 007h    ;
TRIS  PORTB    ;--10 -ppp  --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;RB5 to be latched as the pin value (High).

```

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
 - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
 - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

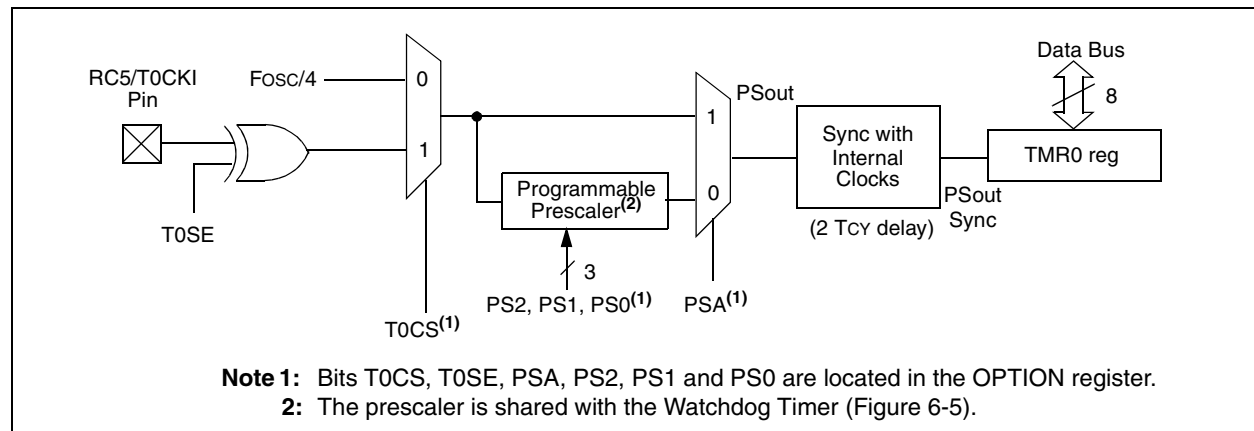
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



7.7 Time-Out Sequence, Power Down, and Wake-up from SLEEP Status Bits (TO/PD/RBWUF)

The TO, PD, and RBWUF bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a MCLR or Watchdog Timer (WDT) reset.

TABLE 7-7: TO/PD/RBWUF STATUS AFTER RESET

RBWUF	TO	PD	RESET caused by
0	0	0	WDT wake-up from SLEEP
0	0	u	WDT time-out (not from SLEEP)
0	1	0	MCLR wake-up from SLEEP
0	1	1	Power-up
0	u	u	MCLR not during SLEEP
1	1	0	Wake-up from SLEEP on pin change

Legend: u = unchanged
Note 1: The TO, PD, and RBWUF bits maintain their status (u) until a reset occurs. A low-pulse on the MCLR input does not change the TO, PD, and RBWUF status bits.

7.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.
To reset PIC16C505 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-12 and Figure 7-13.

FIGURE 7-12: BROWN-OUT PROTECTION CIRCUIT 1

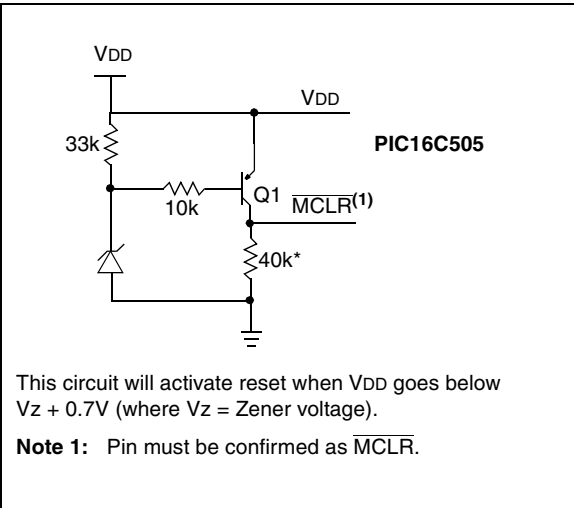


FIGURE 7-13: BROWN-OUT PROTECTION CIRCUIT 2

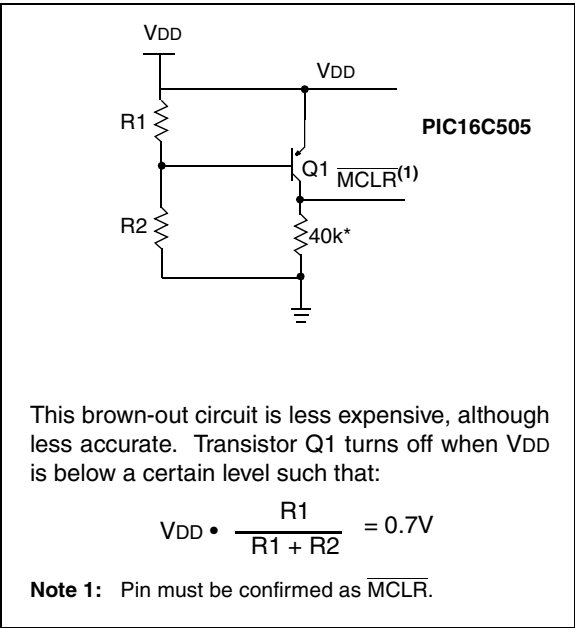
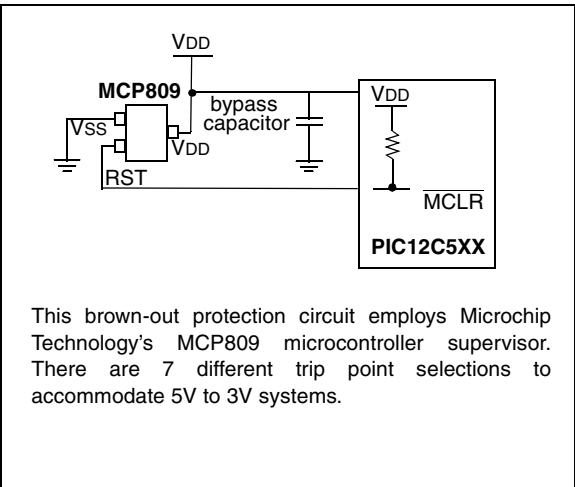


FIGURE 7-14: BROWN-OUT PROTECTION CIRCUIT 3



7.12 In-Circuit Serial Programming

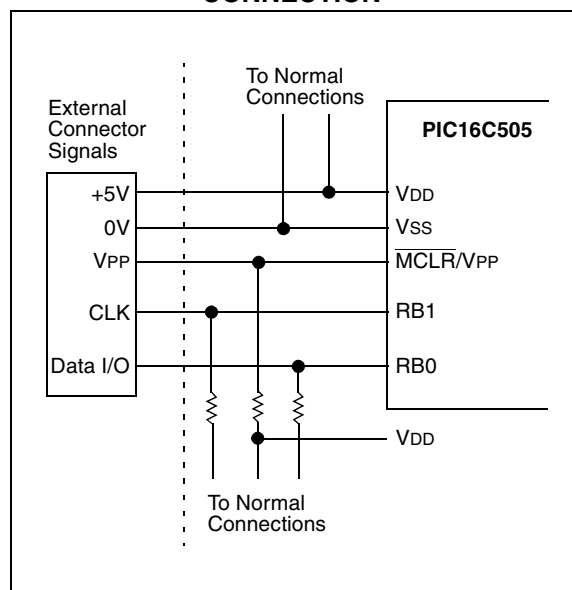
The PIC16C505 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB1 and RB0 pins low while raising the MCLR (VPP) pin from VIL to VIH (see programming specification). RB1 becomes the programming clock and RB0 becomes the programming data. Both RB1 and RB0 are Schmitt Trigger inputs in this mode.

After reset, a 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C505 Programming Specifications.

A typical in-circuit serial programming connection is shown in Figure 7-15.

FIGURE 7-15: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



ADDWF Add W and f

Syntax: [*label*] ADDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) + (f) \rightarrow (\text{dest})$

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff
------	------	------

Description: Add the contents of the W register and register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ADDWF FSR, 0

Before Instruction

W = 0x17
 FSR = 0xC2

After Instruction

W = 0xD9
 FSR = 0xC2

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .\text{AND}. (f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0001	01df	ffff
------	------	------

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ANDWF FSR, 1

Before Instruction

W = 0x17
 FSR = 0xC2

After Instruction

W = 0x17
 FSR = 0x02

ANDLW And literal with W

Syntax: [*label*] ANDLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) .\text{AND}. (k) \rightarrow (W)$

Status Affected: Z

Encoding:

1110	kkkk	kkkk
------	------	------

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: ANDLW 0x5F

Before Instruction

W = 0xA3

After Instruction

W = 0x03

BCF Bit Clear f

Syntax: [*label*] BCF f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: $0 \rightarrow (f)$

Status Affected: None

Encoding:

0100	bbbf	ffff
------	------	------

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example: BCF FLAG_REG, 7

Before Instruction

FLAG_REG = 0xC7

After Instruction

FLAG_REG = 0x47

CALL		Subroutine Call						
Syntax:	[<i>label</i>] CALL k							
Operands:	$0 \leq k \leq 255$							
Operation:	(PC) + 1 → Top of Stack; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>							
Status Affected:	None							
Encoding:	<table border="1"><tr><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>					1001	kkkk	kkkk
1001	kkkk	kkkk						
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.							
Words:	1							
Cycles:	2							
Example:	HERE CALL THERE							

Before Instruction
PC = address (HERE)

After Instruction
PC = address (THERE)
TOS = address (HERE + 1)

CLRF	Clear f			
Syntax:	[<i>label</i>] CLRF f			
Operands:	$0 \leq f \leq 31$			
Operation:	00h \rightarrow (f); 1 \rightarrow Z			
Status Affected:	Z			
Encoding:	<table border="1"><tr><td>0000</td><td>011f</td><td>ffff</td></tr></table>	0000	011f	ffff
0000	011f	ffff		
Description:	The contents of register 'f' are cleared and the Z bit is set.			
Words:	1			
Cycles:	1			
Example:	CLRF FLAG_REG			

Before Instruction
FLAG_REG = 0x5A

After Instruction
FLAG_REG = 0x00
Z = 1

CLRW	Clear W			
Syntax:	[<i>label</i>] CLRW			
Operands:	None			
Operation:	00h → (W); 1 → Z			
Status Affected:	Z			
Encoding:	<table border="1"><tr><td>0000</td><td>0100</td><td>0000</td></tr></table>	0000	0100	0000
0000	0100	0000		
Description:	The W register is cleared. Zero bit (Z) is set.			
Words:	1			
Cycles:	1			
Example:	CLRW			

Before Instruction
W = 0x5A

After Instruction
W = 0x00
Z = 1

CLRWD		Clear Watchdog Timer			
Syntax:	[<i>label</i>] CLRWD				
Operands:	None				
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → \overline{TO} ; 1 → \overline{PD}				
Status Affected:	\overline{TO} , \overline{PD}				
Encoding:	<table border="1"><tr><td>0000</td><td>0000</td><td>0100</td></tr></table>		0000	0000	0100
0000	0000	0100			
Description:	The CLRWD instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits \overline{TO} and \overline{PD} are set.				
Words:	1				
Cycles:	1				
Example:	CLRWD				

Before Instruction
WDT counter = ?

After Instruction
WDT counter = 0x00
WDT prescale = 0
 \overline{TO} = 1
 \overline{PD} = 1

SWAPF Swap Nibbles in f

Syntax: `[label] SWAPF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (dest<7:4>);$
 $(f<7:4>) \rightarrow (dest<3:0>)$

Status Affected: None

Encoding:

0011	10df	ffff
------	------	------

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.

Words: 1

Cycles: 1

Example `SWAPF REG1, 0`

Before Instruction
 REG1 = 0xA5

After Instruction
 REG1 = 0xA5
 W = 0x5A

TRIS Load TRIS Register

Syntax: `[label] TRIS f`

Operands: $f = 6$

Operation: $(W) \rightarrow \text{TRIS register } f$

Status Affected: None

Encoding:

0000	0000	0fff
------	------	------

Description: TRIS register 'f' ($f = 6$ or 7) is loaded with the contents of the W register

Words: 1

Cycles: 1

Example `TRIS PORTB`

Before Instruction
 W = 0xA5

After Instruction
 TRIS = 0xA5

XORLW Exclusive OR literal with W

Syntax: `[label] XORLW k`

Operands: $0 \leq k \leq 255$

Operation: $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Encoding:

1111	kkkk	kkkk
------	------	------

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `XORLW 0xAF`

Before Instruction
 W = 0xB5

After Instruction
 W = 0x1A

XORWF Exclusive OR W with f

Syntax: `[label] XORWF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .XOR. (f) \rightarrow (dest)$

Status Affected: Z

Encoding:

0001	10df	ffff
------	------	------

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example `XORWF REG,1`

Before Instruction
 REG = 0xAF
 W = 0xB5

After Instruction
 REG = 0x1A
 W = 0xB5

PIC16C505

10.1 DC CHARACTERISTICS: PIC16C505-04 (Commercial, Industrial, Extended) PIC16C505-20(Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)				
Parm. No.	Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
D001	Supply Voltage	VDD	3.0		5.5	V	See Figure 10-1 through Figure 10-3
D002	RAM Data Retention Voltage ⁽²⁾	VDR	—	1.5*	—	V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See section on Power-on Reset for details
D010	Supply Current ⁽³⁾	IDD	—	0.8 — — — — —	1.4 1.0 7 12 16 27	mA mA mA mA mA μA	FOSC = 4MHz, VDD = 5.5V, WDT disabled (Note 4)* FOSC = 4MHz, VDD = 3.0V, WDT disabled (Note 4) FOSC = 10MHz, VDD = 3.0V, WDT disabled (Note 6) FOSC = 20MHz, VDD = 4.5V, WDT disabled FOSC = 20MHz, VDD = 5.5V, WDT disabled* FOSC = 32kHz, VDD = 3.0V, WDT disabled (Note 6)
D020	Power-Down Current ⁽⁵⁾	IPD	—	0.25 — — — —	4 5.5 8 14	μA μA μA μA	VDD = 3.0V (Note 6) VDD = 4.5V* (Note 6) VDD = 5.5V, Industrial VDD = 5.5V, Extended Temp.
D022	WDT Current ⁽⁵⁾	ΔIWDT	—	2.2	5	μA	VDD = 3.0V (Note 6)
1A	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency	Fosc	0 0 0 0	— — — —	200 4 4 20	kHz MHz MHz MHz	All temperatures All temperatures All temperatures All temperatures

* These parameters are characterized but not tested.

- Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- 2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
- a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD;
WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4:** Does not include current through Rext. The current through the resistor can be estimated by the formula:
 $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.
- 5:** The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.
- 6:** Commercial temperature range only.

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TABLE 10-1: PULL-UP RESISTOR RANGES - PIC16C505

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
RB0/RB1/RB4					
2.5	–40	38K	42K	63K	W
	25	42K	48K	63K	W
	85	42K	49K	63K	W
	125	50K	55K	63K	W
5.5	–40	15K	17K	20K	W
	25	18K	20K	23K	W
	85	19K	22K	25K	W
	125	22K	24K	28K	W
RB3					
2.5	–40	285K	346K	417K	W
	25	343K	414K	532K	W
	85	368K	457K	532K	W
	125	431K	504K	593K	W
5.5	–40	247K	292K	360K	W
	25	288K	341K	437K	W
	85	306K	371K	448K	W
	125	351K	407K	500K	W

* These parameters are characterized but not tested.

PIC16C505

10.5 Timing Diagrams and Specifications

FIGURE 10-5: EXTERNAL CLOCK TIMING - PIC16C505

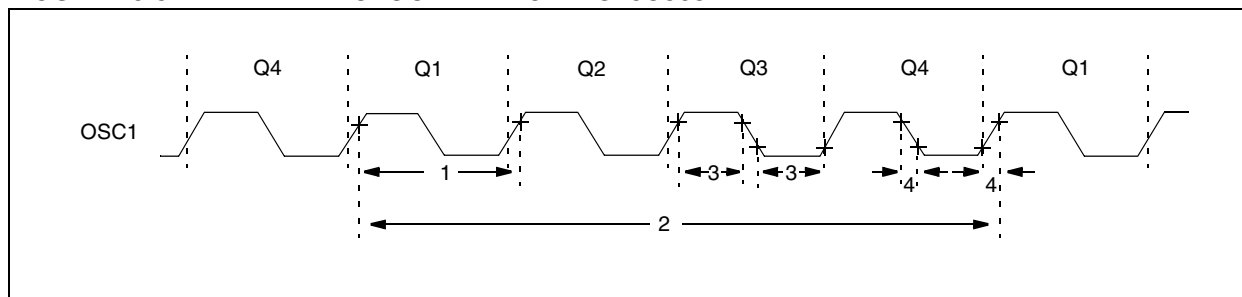


TABLE 10-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C505

AC Characteristics Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage V_{DD} range is described in Section 10.1							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
1A	Fosc	External CLKIN Frequency ⁽²⁾	DC	—	4	MHz	XT osc mode
			DC	—	4	MHz	HS osc mode (PIC16C505-04)
			DC	—	20	MHz	HS osc mode (PIC16C505-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency ⁽²⁾	DC	—	4	MHz	EXTRC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C505-04)
			DC	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period ⁽²⁾	250	—	—	ns	XT osc mode
			50	—	—	ns	HS osc mode (PIC16C505-20)
			—	—	—	μs	LP osc mode
		Oscillator Period ⁽²⁾	250	—	—	ns	EXTRC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS ocs mode (PIC16C505-04)
			50	—	250	ns	HS ocs mode (PIC16C505-20)
			5	—	—	μs	LP osc mode
2	Tcy	Instruction Cycle Time	—	4/Fosc	DC	ns	
			200	—	—	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

11.0 DC AND AC CHARACTERISTICS - PIC16C505

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3 σ) and (mean - 3 σ) respectively, where σ is standard deviation.

FIGURE 11-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 5.0V) (INTERNAL RC IS CALIBRATED TO 25°C, 5.0V)

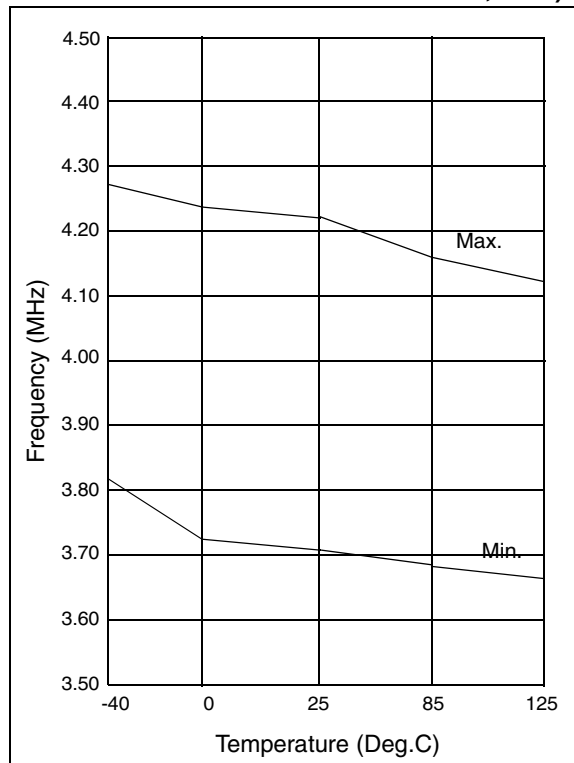
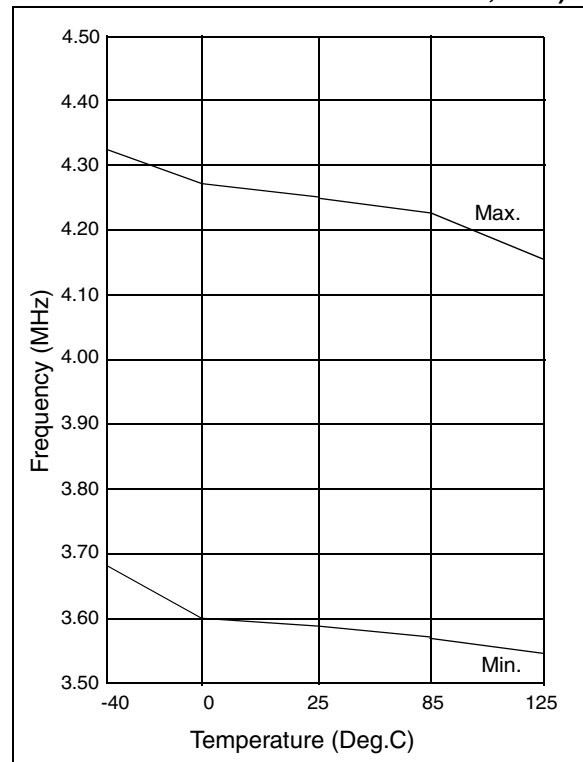


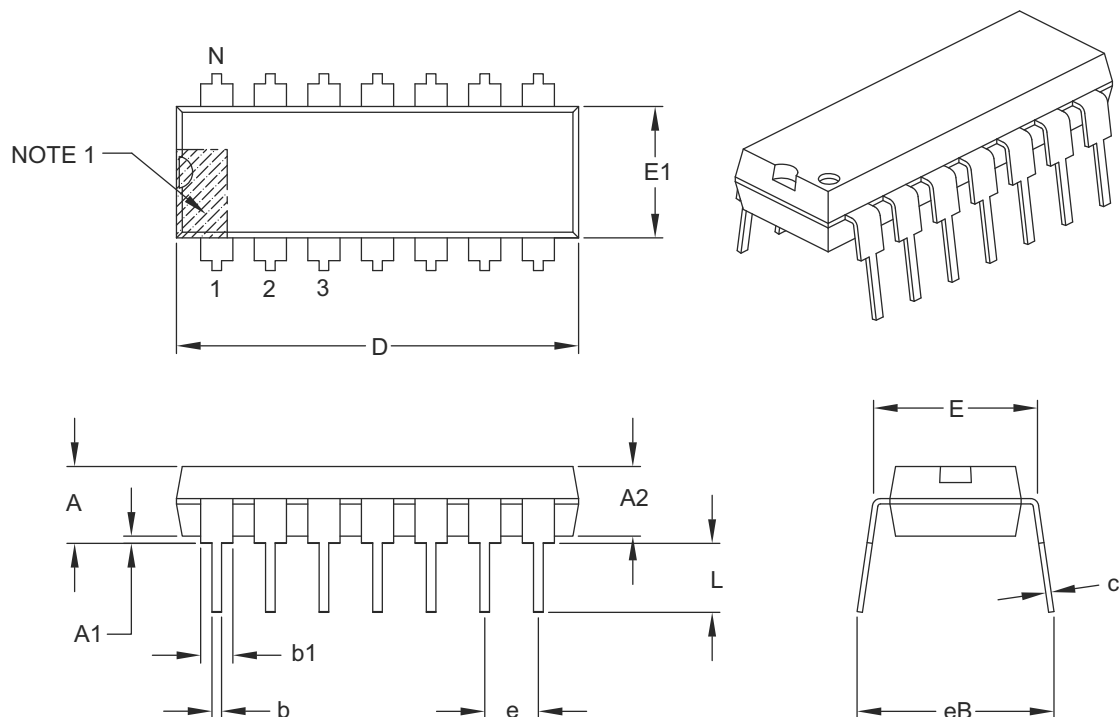
FIGURE 11-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 2.5V) (INTERNAL RC IS CALIBRATED TO 25°C, 5.0V)



PIC16C505

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	—	—	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	—	—
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	—	—	.430

Notes:

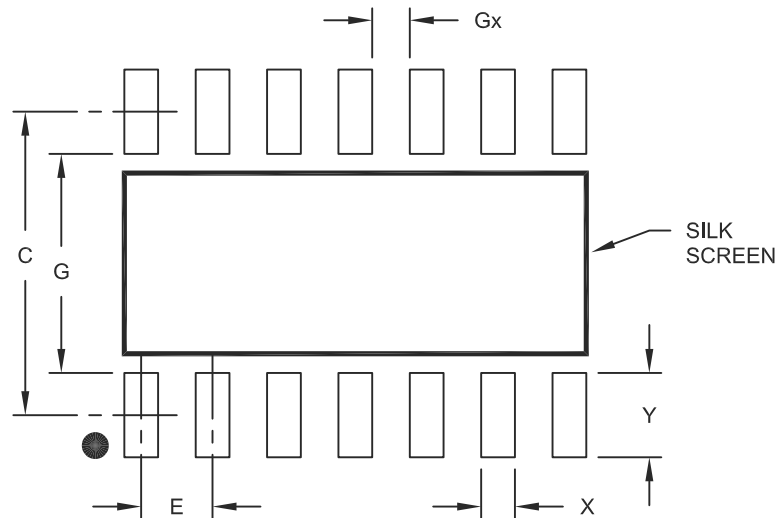
- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

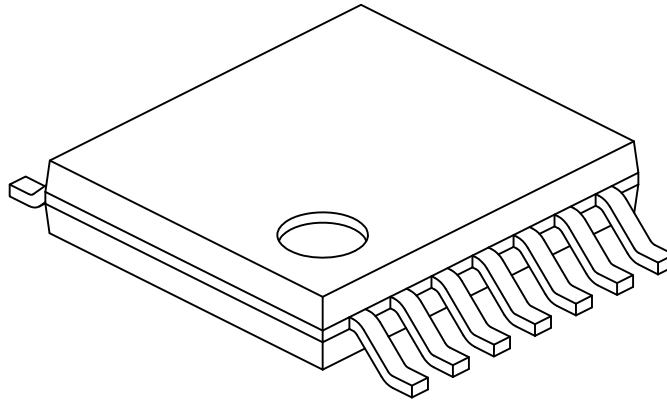
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)	1.00 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

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PIC16C505 Product Identification System

PART NO.	-XX	X	/XX	XXX			Examples
					Pattern:	Special Requirements	a) PIC16C505-04/P Commercial Temp., PDIP Package, 4 MHz, normal VDD limits
					Package:	SL = 150 mil SOIC P = 300 mil PDIP ST = 4.4 mm TSSOP	b) PIC16C505-04/SL Industrial Temp., SOIC package, 4 MHz, normal VDD limits
					Temperature Range:	- = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C	c) PIC16C505-04I/P Industrial Temp., PDIP package, 4 MHz, normal VDD limits
					Frequency Range:	04 = 4 MHz (XT, INTRC, EXTRC OSC) 20 = 20 MHz (HS OSC)	
					Device	PIC16C505 PIC16LC505 PIC16C505T (Tape & reel for SOIC only) PIC16LC505T (Tape & reel for SOIC only)	

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