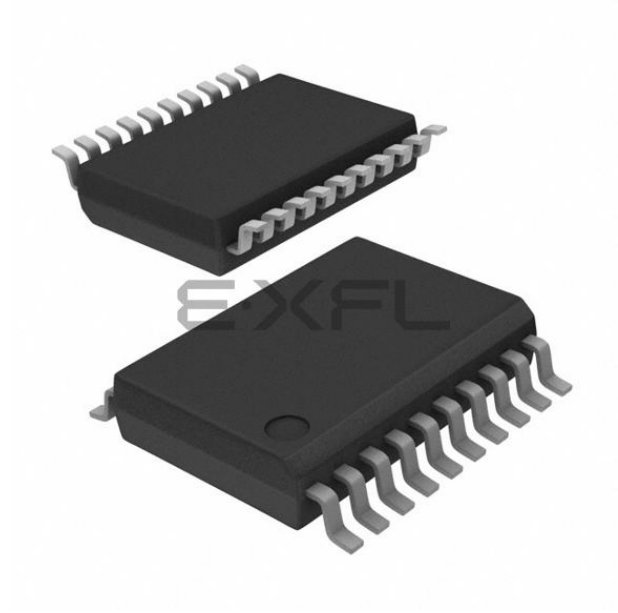
Analog Devices Inc./Maxim Integrated - ZLF645E0H2064G Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8 LXMC
Core Size	8-Bit
Speed	8MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.9V ~ 3.6V
Data Converters	-
Oscillator Type	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlf645e0h2064g

Table of Contents

Table 24. Stack Pointer Register Low Byte (SPL)

Bit	7	6	5	4	3	2	1	0
Field	Stack Pointer							
Reset	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank Independent: FFh; Linear: 0FFh							

Bit Position	Value	Description
[7:0]	00-FF	Stack Pointer

Table 25. Stack Pointer Register High Byte (SPH) or User Data Register (USER)

Bit	7	6	5	4	3	2	1	0
Field	Stack Pointer							
Reset	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank Independent: FEh; Linear: 0FEh							

Notes:

1. *For devices with 1K bytes of RAM and with 16-bit stack pointer mode enabled, the upper 6 bits of this register are unused for stack addressing. For devices with 512 bytes of RAM and with 16-bit stack pointer mode enabled, the upper 7 bits of this register are unused for stack addressing.*
2. *When ZLF645 MCU is not in 16-bit stack pointer mode, this register is available to store use user data and its functionality is identical to other Maxim® Crimzon products such as the ZLP12840 and ZLR64400 MCUs. When available for user data, this register must not be used as a counter for the DJNZ instruction.*

for the command will default to the maximum memory size. The on-chip Flash Controller must be written to and unlocked for the programming operation to occur. If the Flash Controller is not unlocked, the data is discarded. Also, data is discarded for writes to protected areas of the Flash's main or information Page 3 areas based upon the settings of the read/write protect option bits in User Option Byte 1 (OPT1) register.

```
ICP ← 0AH
ICP ← Flash Memory Address[15:8]
ICP ← Flash Memory Address[7:0]
ICP ← Size[15:8]
ICP ← Size[7:0]
ICP ← 1-memsize data bytes
```

- **Read Flash Memory (0BH)**—The Read Flash Memory command is used to read data from the Flash's main memory area or Information Area. This command is equivalent to the CPU reading the memory through the LDC and LDCI instructions. Data can be read 1 to 'memsize' bytes at a time where `memsize` represents the size (32 KB or 64 KB) of the Flash memory for the product option chosen (The `memsize` number of bytes can be written by setting the size to 0). Depending on the settings of the read/write protect option bits in User Option Byte 1 register, reads to protected areas of the Flash's main memory area will return `FFH` for the data.

  ```
  ICP ← 0BH
  ICP ← Flash Memory Address[15:8]
  ICP ← Flash Memory Address[7:0]
  ICP ← Size[15:8]
  ICP ← Size[7:0]
  ICP → 1-65536 data bytes
  ```

- **Read Flash Main Memory CRC (0EH)**—The Read Flash Main Memory CRC command computes and returns the Cyclic Redundancy Check (CRC) of the Flash's Main Memory using the 16-bit CRC-CCITT polynomial. If the device is not in ICP mode, this command returns `FFFFH` for the CRC value. Unlike most other ICP Read commands, there is a delay from issuing of the command until the ICP returns the data. The ICP reads the Main Memory, calculates the CRC value, and returns the result. The delay is a function of the Flash main memory size and is approximately equal to the system clock period multiplied by the number of bytes in the Flash main memory.

  ```
  ICP ← 0EH
  ICP → CRC[15:8]
  ICP → CRC[7:0]
  ```

- **Read ICP Autobaud Register (1BH)**— The Read ICP Autobaud register command reads the 12-bit ICP autobaud value set during autobaud detection.

  ```
  ICP ← 1BH
  ICP → (4'b0000, Autobaud[11:8])
  ```

TEST Mode Register

The TEST Mode register is used to enable various device test or Flash memory access modes. At present this register only provides configuration for a single mode where, once programmed, Flash memory accesses bypass the devices Flash Controller and are done through the devices I/O pins. A complete description of this mode is available in the Flash Byte Programming Interface section. This register can only be read or written using the ICP Read/Write Test Mode Register commands.

Table 31. TEST Mode Register (TESTMODE)

Bits	7	6	5	4	3	2	1	0
Field	Reserved F					lash Controller Bypass Mode	Reserved	
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R/W	R	R

Bit Position	Value	Description
[7:3]	—	**Reserved**— Must be written to 1. Reads return 0.
[2]		**Flash Controller Bypass Mode**
	0	The device is not in Flash Controller Bypass Mode.
	1	The device is in Flash Controller Bypass mode.
[1:0]	—	**Reserved**—Must be written to 1. Reads return 0.

Exiting ICP Mode

The ZLF645 MCU is taken out of ICP mode under any of the following conditions:

- Initiating a POR with P36 held High during the entire reset period.
- Lowering V_{DD} until the ZLF645 MCU reaches a Voltage Brownout reset state.

Table 40.Flash Byte Programming Functions Summary

Flash Memory Block	Program	Read	Page Erase	Mass Erase	Flash Protect Option Bits
Main Memory	Yes	Yes	Yes	Yes	FLRWP=1, FLPROT1=1
Main Memory	No	No	No	Yes	FLRWP=0, FLPROT1=X
Main Memory	Yes[1]	Yes[1]	Yes[1]	Yes	FLRWP=1, FLPROT1=0
Information Area	Yes[2]	Yes[2]	Yes[2]	Yes	FLRWP=1, FLPROT1=1
Information Area	No	Yes[2]	No	Yes	FLRWP=1, FLPROT1=0
Information Area	No	Yes[2]	No	Yes	FLRWP=0, FLPROT1=1

Notes

1. Program, Read, and Page Erase access is limited to the upper half address space of the main memory only.
2. Only Page 3 of the Information Area is accessible for Program, Read, and Page Erase operations.

9. Before disabling the transmitter, read the transmit completion status bit, UST[1]. If UST[1]=0, continue to monitor the bit until it changes to 1, which indicates that all data in the Transmit Data and Internal Shift registers has been transmitted.

Caution: *Data written while the transmit enable bit is clear (UCTL[7]=0) will not be transmitted. Data written while the transmit data status bit is clear (UST[2]=0) overwrites the previous value written, so the previous written value will not be transmitted. Disabling the UART transmitter while the transmit completion status bit is clear (UST[1]=0) can corrupt the byte being transmitted.*

Receiving Data Using the Polled Method

Follow the steps below to configure the UART for polled data reception:

1. Write to the BCNST register to set the appropriate baud rate.
2. Write to the UART Control register (UCTL) to:
   (a) Set the receive enable bit (UCTL[6]) to enable the UART for data reception
   (b) Enable parity (if appropriate) and select either even- or odd-parity
3. Check the receive status bit in the UART Status register, bit UST[7], to determine if the Receive Data register contains a valid data byte (indicated by a 1). If UST[7] is set to 1 to indicate available data, continue to Step 4. If the Receive Data register is empty (indicated by a 0), continue to monitor the UST[7] bit awaiting reception of the valid data.
4. Read data from the UART Receive Data register.
5. Return to Step 3 to receive additional data.

Receiving Data Using the Interrupt-Driven Method

The UART Receiver interrupt indicates the availability of new data (as well as error conditions).

Follow the steps below to configure the UART receiver for interrupt-driven operation:

1. Write to the UART BRG Constant registers to set the appropriate baud rate.
2. Execute DI instruction to disable interrupts.
3. Write to the Interrupt Control registers to enable the UART receiver interrupt and set the appropriate priority.
4. Clear the UART Receiver interrupt in the applicable Interrupt Request register.
5. Write to the UART Control register (UCTL) to:
   (a) Set the receive enable bit (UCTL[6]) to enable the UART for data reception
   (b) Enable parity, if appropriate, and select either even- or odd-parity
6. Execute an EI instruction to enable interrupts.

Bit Position	Value	Description
[6]		**Parity Error**—Set when a parity error occurs; cleared when URDATA is read.
	0	No parity error occurs.
	1	Parity error occurs.
[5]		**Overrun Error**—Set when an overrun error occurs; cleared when URDATA is read.
	0	No overrun error occurs.
	1	Overrun error occurs.
[4]		**Framing Error**—Set when a framing error occurs; cleared when URDATA is read.
	0	No framing error occurs.
	1	Framing error occurs.
[3]		**Break**—Set when a break is detected; cleared when URDATA is read.
	0	No break occurs.
	1	Break occurs.
[2]		**Transmit Data Status**—Set when the UART is ready to transmit; cleared when TRDATA is written.
	0	Do not write to the UART Transmit Data register.
	1	UART Transmit Data register ready to receive additional data.
[1]		**Transmit Completion Status**
	0	Data is currently transmitting.
	1	Transmission is complete.
[0]	Read	**Noise Filter**—Detects noise during data reception.
	0	No noise detected.
	1	Noise detected.
	Write	
	0	Turn off noise filter.
	1	Turn on noise filter.

UART Control Register

The UART Control register controls the UART. In addition to setting bit 5, you must also set appropriate bit in the Interrupt Mask register (see Table 65 on page 133).

Note: *This register is not reset after a Stop Mode Recovery.*

Table 45. UART Control Register (UCTL)

Bit	7	6	5	4	3	2	1	0
Field	Transmitter Enable	Receiver Enable	UART Interrupts Enable	Parity Enable	Parity Select	Send Break	Stop Bits	Baud Rate Generator
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank Independent: F3h; Linear: 0F3h							

Bit Position	Value	Description
[7]	0 1	Transmitter disabled. Transmitter enabled.
[6]	0 1	Receiver disabled. Receiver enabled.
[5]	0 1	UART Interrupts disabled. UART Interrupts enabled.
[4]	0 1	Parity disabled. Parity enabled.
[3]	0 1	Even parity selected. Odd parity selected.
[2]	0 1	No break is sent. Send Break (force Tx output to 0).
[1]	0 1	One stop bit. Two stop bits.
[0]	 0 1	**Baud Rate Generator**—When the transmitter and receiver are disabled, the BRG can be used as an additional timer. When setting this bit, clear bits [7:6] in this register. Also set bit [5] if an interrupt is required when the BRG is reloaded. BRG used as Baud Rate Generator for UART. BRG used as timer.

UART Baud Rate Generator Constant Register

The UART baud rate generator determines the frequency at which UART data is received and transmitted. This baud rate is determined by the following equation:

$$\text{UART Data Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{\text{16 x UART Baud Rate Divisor Value (BCNST)}}$$

T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 bits [5:4]) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 bits [5:4]) is detected during counting, the current value of T8 is complemented and put into one of the capture registers.

If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, bits [1:0]) is set, and an interrupt can be generated if enabled (CTR0, bit 2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, bit 5) is set, and an interrupt can be generated if enabled (CTR0, bit 1). T8 then continues counting from FFh(see Figure 32 on page 106).

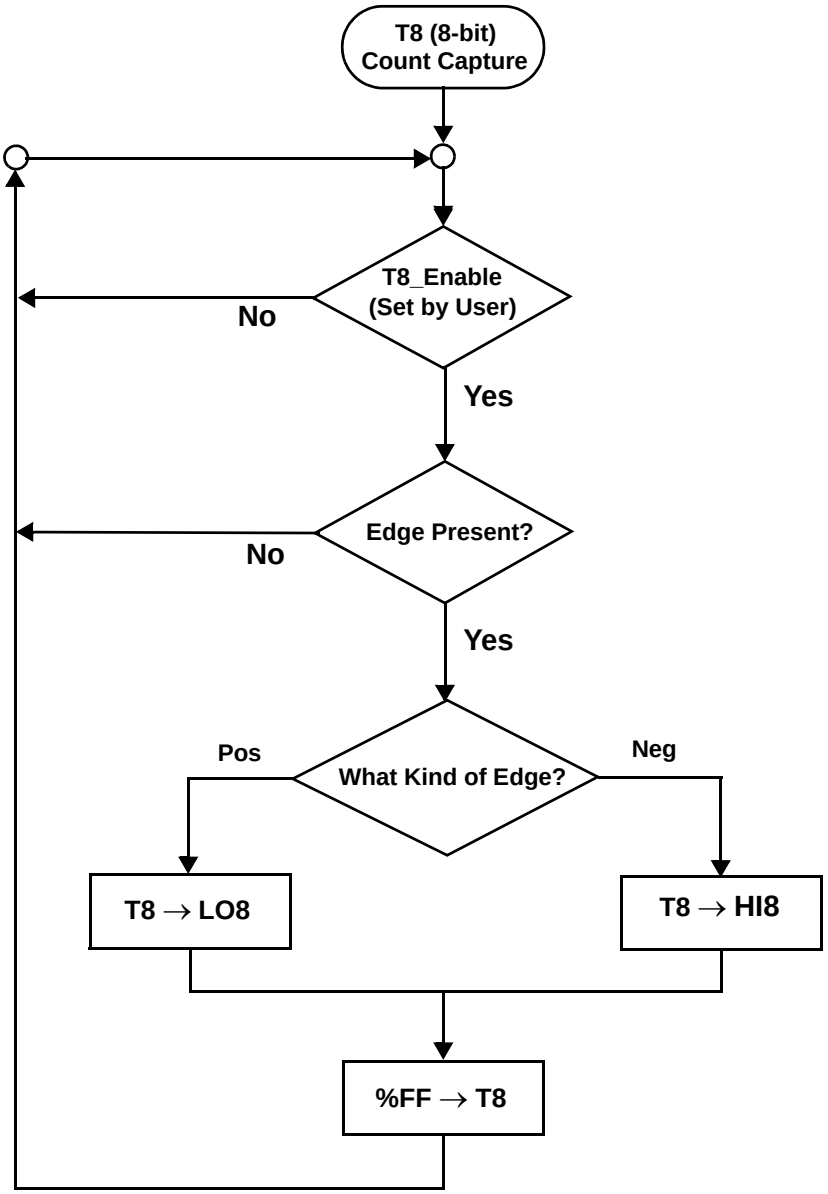


Figure 32. DEMODULATION Mode Count Capture Flowchart

When bit 4 of CTR3 is enabled, the flow of the demodulation sequence is altered. The third edge makes T8 active, and the fourth and fifth edges are captured. The capture interrupt is activated after the fifth event occurs. This mode is useful for capturing the carrier duty cycle as well as the frequency at which the first cycle is corrupted. See Figure 33 and Figure 34.

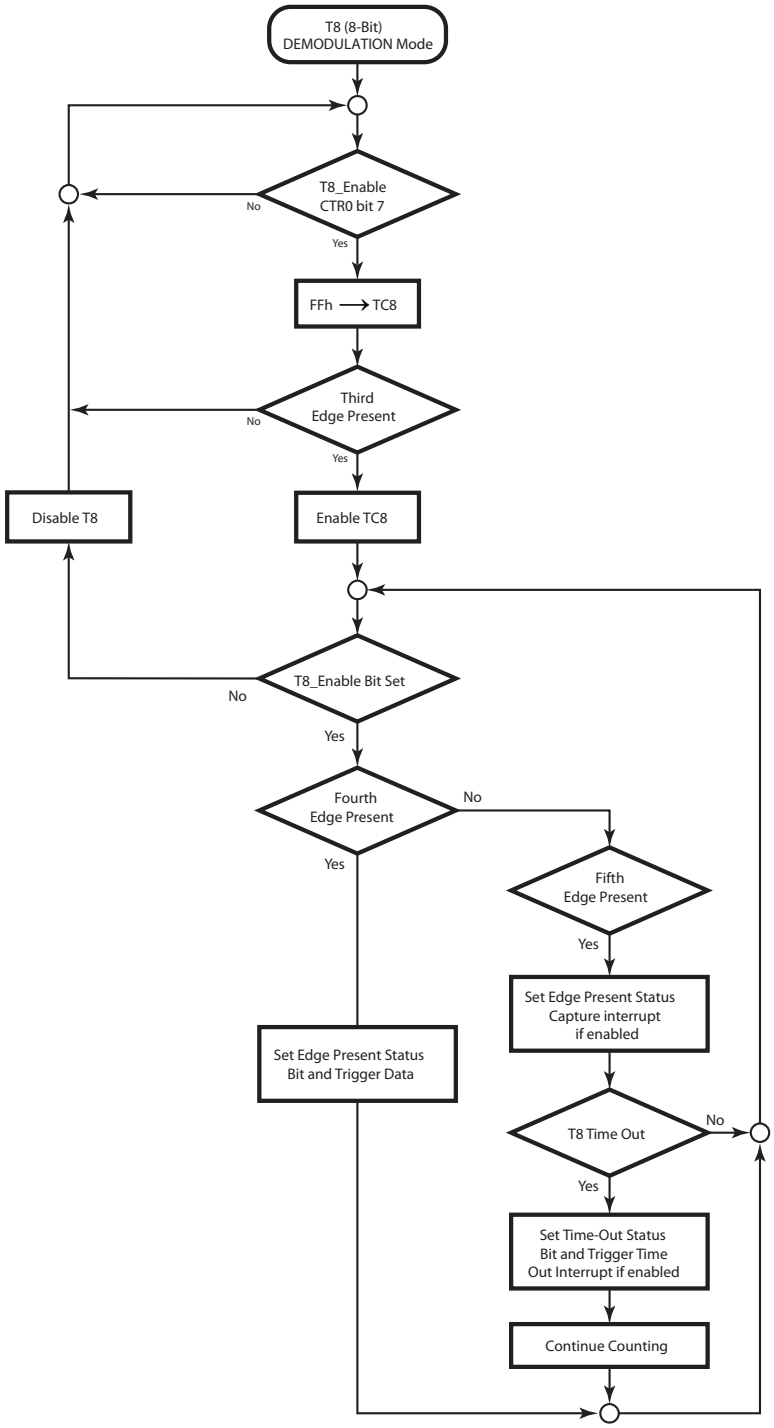


Figure 34. DEMODULATION Mode Flowchart with Bit 4 of CTR3 Set

Timer 16 Capture Low Register

The Timer 16 Capture Low register (see Table 51) holds the captured data from the output of the 16-bit Counter/Timer 16. This register contains the least significant byte (LSB) of the data.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 51. Timer 16 Capture Low Register (LO16)

Bit	7	6	5	4	3	2	1	0
Field	T16_Capture_LO							
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	Bank D: 08h; Linear: D08h							

Bit Position	Value	Description
[7:0]	0hh–FFh	**T16_Capture_LO**—Read returns captured data. Writes have no effect.

Counter/Timer 16 High Hold Register

The Counter/Timer 16 High Hold register (see Table 52) contains the high byte of the value loaded into the T16 timer.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 52. Counter/Timer 16 High Hold Register (TC16H)

Bit	7	6	5	4	3	2	1	0
Field	T16_Data_HI							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank D: 07h; Linear: D07h							

Bit Position	Value	Description
[7:0]	0hh–FFh	**T16_Data_HI**—Read/Write Data.

Voltage Brownout Standby

An on-chip voltage comparator circuit (VBO) checks that the V_{DD} is at the required level for correct operation of the device in terms of Flash memory reads. A second on-chip comparator circuit (subVBO) checks that the V_{DD} level is high enough for proper operation of the VBO circuit. If the V_{DD} level drops below the VBO trip point, the ZLF645 will be held in a reset state as long as V_{DD} remains below this trip point value, and the XTAL1 and XTAL2 oscillator circuitry will be disabled thereby stopping the clock input to the ZLF645 and saving power. If the V_{DD} level continues to drop below the subVBO trip point, the ZLF645 will remain in a reset state and the VBO comparator circuit will be disabled for further power savings. When the power level returns to a value above the VBO trip point, the device performs a power-on reset and functions normally.

STOP Mode

`STOP` instruction turns OFF the internal clock and external crystal oscillation, thus reducing the MCU supply current to a very low level. For STOP mode current specifications, see Table 80 on page 165.

To enter STOP mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP instruction (OpCode = `FFh`) immediately before the appropriate sleep instruction, as given below:

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP mode
```

STOP mode is terminated only by a reset, such as WDT time-out, POR, or one of the Stop Mode Recovery events as described in Stop Mode Recovery Event Sources on page 144. This condition causes the processor to restart the application program at address `000Ch`.

Unlike a normal POR or WDT reset, a Stop Mode Recovery reset does not reset the contents of some registers and bits. Register bits not reset by a Stop Mode Recovery are highlighted in grey in the register tables. Register bit SMR[7] is set to 1 by a Stop Mode Recovery.

HALT Mode

`HALT` instruction turns off the internal CPU clock, but not the XTAL oscillation.
The counter/timers, UART, and interrupts (IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5) remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after HALT mode.

Table 69. Stop Mode Recovery Register (SMR)

Bit	7	6	5	4	3	2	1	0
Field	Stop Flag	Stop Mode Recovery Level	Stop Delay	Stop Mode Recovery Source			Reset Time Reduction	SCLK/TCLK Divide-by-16
Reset	0	0	1	0	0	0	0	0
R/W	R	W	W	W	W	W	W	W
Address	Bank F: 0Bh; Linear: F0Bh							

Bit Position	Value	Description
[7]		**Stop Flag**—Indicates whether last startup was power-on reset or Stop Mode Recovery. A write to this bit has no effect.
	0	Power-on reset.
	1	Stop Mode Recovery.
[6]		**Stop Mode Recovery Level**—Selects whether an SMR[4:2]-selected SMR is initiated by a Low or High level at the XOR-gate input (see Figure 44 on page 145).
	0	Low.
	1	High.
[5]		**Stop Delay**—Controls the reset delay after recovery. Must be 1 if using a crystal or resonator clock source.
	0	Off.
	1	On.
[4:2]		**Stop Mode Recovery Source**—Specifies a Stop Mode Recovery wake-up source at the XOR gate input (see Figure 44 on page 145). This value is not changed by a Stop Mode Recovery. The following equations ignore any Port pin configured as output or selected in SMR1 or SMR3.
	000	No SMR register source selected.
	001	Reserved.
	010	P31.
	011	P32.
	100	P33.
	101	P27.
	110	Port 2 NOR 0–3.
	111	Port 2 NOR 0–7.

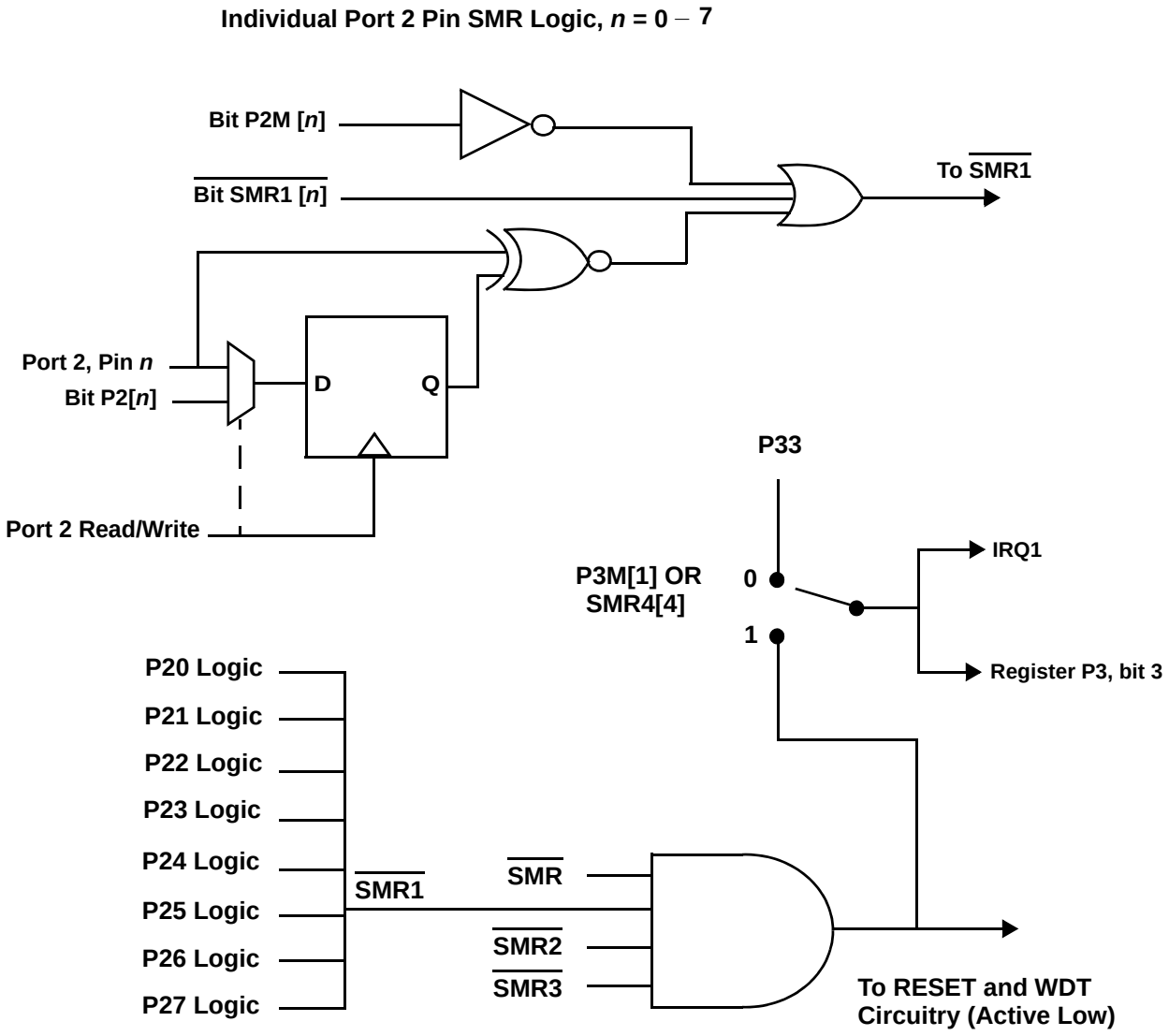


Figure 45. SMR1 Register-Controlled Event Sources

Table 81. Clock, Reset, Timers, and SMR Timing (Continued)

No	Symbol	Parameter	V_{CC}	T_A = 0 °C to +70 °C 8.0 MHz Min	T_A = 0 °C to +70 °C 8.0 MHz Max	Units	WDTMR (Bits 6, 5, 4, 1, 0)
13	T_{POR}	Power-on reset	1.9–3.6	2.5	10^5	ms	—
14	f_{iramp}	Frequency of input signal for IR amplifier	—	0	500	kHz	—

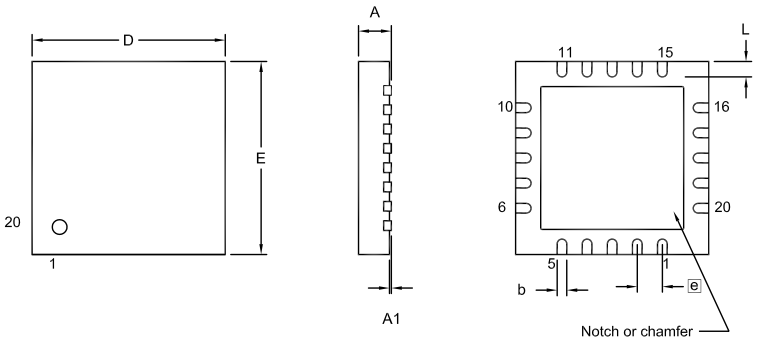
Notes
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33:P31).
3. SMR – bit 5 = 1.
4. SMR – bit 5 = 0.
5. If bit 1 of the SMR register is programmed to 1, this value is 2.5 ms as measured from the time the oscillator input to XTAL1 reaches a peak to peak voltage oscillation of at least 300 mV.

Table 82. Flash Memory Electrical Characteristics and Timing

No	Symbol	Parameter	T_A = 0 °C to +70 °C 8.0 MHz Min	T_A = 0 °C to +70 °C 8.0 MHz Max	Units	Condition
1	I_{FLP}	Flash Memory Programming Current	—	10	mA	—
2	I_{FLE}	Flash Memory Page/Mass Erase Current	—	6	mA	—
3	I_{RD}	Flash Dynamic Read Current	—	420	a	Assumes reads every clock cycle with a 1 MHz clock
4	V_{FLPE}	Flash Memory Program/ Erase Voltage	2.3	3.6	V	—
5	V_{FLR}	Flash Memory Read Voltage	1.8	3.6	V	—
6	T_{PROG}	Flash Programming Time	30	60	us	—
7	Tpe	Flash Page Erase Time	10	—	ms	—
8	Tme	Flash Mass Erase Time	10	—	ms	—
9	Tdr	Flash Data Retention Time	10	—	years	Temp=25 °C
10	Fen	Flash Program/Erase Endurance	20,000	—	cycles	—

Packaging

Figure 50 displays the 20-pin quad flat no-lead (QFN) package for the ZLF645 Series of Flash MCUs.

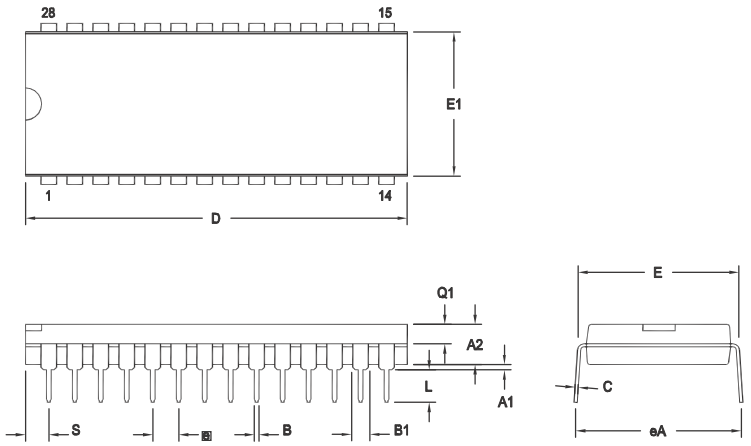


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	-	0.05	-	0.002
b	0.25	0.35	0.010	0.014
D	4.95	5.05	0.195	0.199
E	4.95	5.05	0.195	0.199
e	0.65 BSC		0.026 BSC	
L	0.35	0.45	0.014	0.018

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : 0.08 mm / 0.003"

Figure 50. 20-Pin QFN Package Diagram

Figure 56 displays the 28-pin plastic dual inline package (PDIP) for the ZLF645 Series of Flash MCUs.



SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: Zilog supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 56. 28-Pin PDIP Package Diagram

D

E

F

H

I

U

V

W

X

Z