Analog Devices Inc./Maxim Integrated - ZLF645E0H4864G Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8 LXMC
Core Size	8-Bit
Speed	8MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.9V ~ 3.6V
Data Converters	-
Oscillator Type	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlf645e0h4864g

Maxim Integrated Products
120 San Gabriel Drive
Sunnyvale, CA 94086
United States

408-737-7600
www.maxim-ic.com

19-4572; Rev 0; 4/09

Table 10. 48-Pin SSOP Functional Pin Identification (Continued)

Pin No	Symbol	Function	Signal Direction
45	P23	Port 2, bit 3	Input/Output
46	P24	Port 2, bit 4	Input/Output
2	P25	Port 2, bit 5	Input/Output
3	P26	Port 2, bit 6	Input/Output
4	P27	Port 2, bit 7	Input/Output
29	P30	Port 3, bit 0; connect to VDD if not used	Input
19	P31	Port 3, bit 1	Input
20	P32	Port 3, bit 2	Input
21	P33	Port 3, bit 3	Input
22	P34	Port 3, bit 4	Input/Output
26	P35	Port 3, bit 5	Output
28	P36	Port 3, bit 6	Output
27	P37	Port 3, bit 7	Output
1	P40	Port 4, bit 0	Input/Output
6	P41	Port 4, bit 1	Input/Output
14	P42	Port 4, bit 2	Input/Output
23	P43	Port 4, bit 3	Input/Output
30	P44	Port 4, bit 4	Input/Output
36	P45	Port 4, bit 5	Input/Output
47	P46	Port 4, bit 6	Input/Output
48	P47	Port 4, bit 7	Input/Output
12	V_{DD}	Power Supply	Input
13	V_{DD}	Power Supply	Input
24	V_{SS}	Ground	Input
37	V_{SS}	Ground	Input
38	V_{SS}	Ground	Input
18	XTAL1	Crystal oscillator	Input
17	XTAL2	Crystal oscillator	Output
25	/RESET	Bidirectional reset signal	Input/Output

Port 0

Port 0 is an 8-bit bidirectional CMOS-compatible port. Its eight I/O lines are configured under software control to create a nibble I/O port. The output drivers are push/pull or open-drain, controlled by bit 2 of the Port Configuration Register.

If one or both nibbles are required for I/O operation, they must be configured by writing to the Port 0/1 Mode Register. After a hardware reset or a Stop Mode Recovery, Port 0 is configured as an input port.

Port 0, bit 7 is used as the transmit output of the UART when UART Tx is enabled. The I/O function of Port 0, bit 7 is overridden by the UART serial output (TxD) when UART Tx is enabled (UCTL[7] = 1). The pin must be configured as an output for TxD data to reach the pin (P01M[6] = 0).

An optional pull-up transistor is available as an user-selectable flash programming option on all Port 0 bits with nibble select. Figure 6 displays the Port 0 configuration.

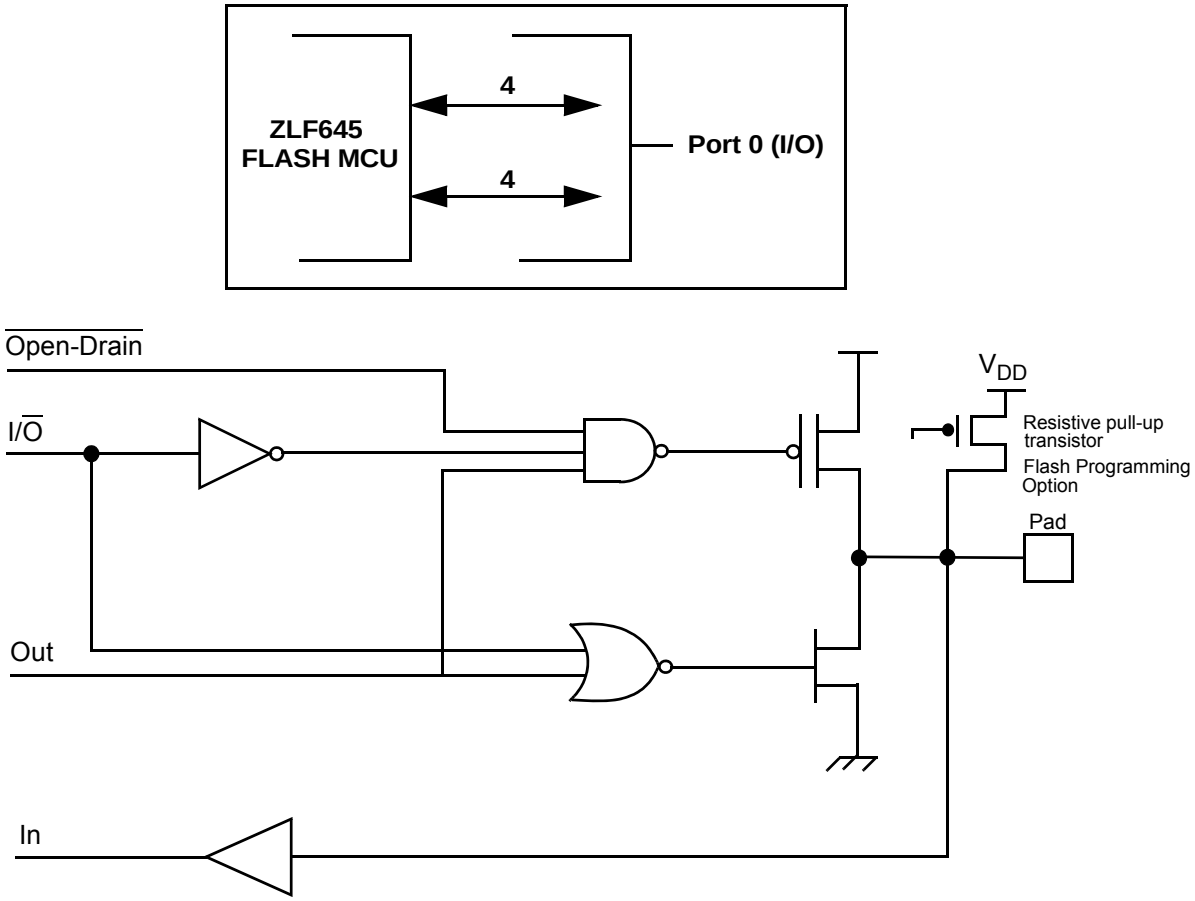


Figure 6. Port 0 Configuration

Port 2 Register

The Port 2 register (see Table 18) allows read and write access to the Port 2 pins.

Table 18. Port 2 Register (P2)

Bit	7	6	5	4	3	2	1	0
Field	P27	P26	P25	P24	P23	P22	P21	P20
Reset	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank 0–3: 02h; Linear: 002h							

Bit Position	Value	Description
[7:0]		**Port 2 Pins 7–0**—Each bit provides access to the corresponding Port 2 pin.
	Read	Pin configured as input or output in P2M register.
	0	Pin level is Low.
	1	Pin level is High.
	Write	Pin configured as output in P2M register.
	0	Assert pin Low.
	1	Assert pin High if configured as push-pull; make pin high-impedance if it is open-drain.

Port 3 Mode Register

The Port 3 Mode register (see Table 19) is used to configure the functionality of Port 3 inputs and the output mode of Port 2. When bit 2 is set, the IR Learning Amplifier is used instead of the COMP1 comparator, regardless of the value of bit 1.

Table 19. Port 3 Mode Register (P3M)

Bit	7	6	5	4	3	2	1	0
Field	Reserved					IR Learning Amplifier	DIGITAL/ ANALOG Mode	Port 2 Open-Drain
Reset	X	X	X	X	X	0	0	0
R/W	—	—	—	—	—	W	W	W
Address	Bank Independent: F7h; Linear: 0F7h							

Bit Position	R/W	Value	Description
[7:3]	—	—	**Reserved**—Must be written to 1. Reads return 11111b.
[2]	W	0 1	IR Learning Amplifier disabled. IR Learning Amplifier enabled with P31 configured as amplifier input.
[1]	W		**DIGITAL/ANALOG Mode**
		0	P30, P31, P32, P33 are digital inputs.
		1	P30, P32, and P33 are comparator inputs. If P3M[2]=0, P31 also function as a comparator input. If P3M[2]=1, P31 is the IR amplifier input.
[0]	W	0 1	Port 2 open-drain. Port 2 push/pull.

Note: *Port 3 Mode register is not reset after a Stop Mode Recovery.*

Port 4 Register

The Port 4 register (see Table 22) allows read and write access to the Port 4 pins.

Table 22. Port 4 Register (P4)

Bit	7	6	5	4	3	2	1	0
Field	P47	P46	P45	P44	P43	P42	P41	P40
Reset	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Banks 0-3: 04h; Linear: 004h							

Bit Position	Value	Description
[7:0]		**Port 4 Pins 7–0**—Each bit provides access to the corresponding Port 4 pin.
	Read	Pin configured as input or output in P4M register.
	0	Pin level is Low.
	1	Pin level is High.
	Write	Pin configured as output in P4M register.
	0	Assert pin Low.
	1	Assert pin High if configured as push-pull; make pin high-impedance if it is open-drain.

Table 36. Flash Sector Protect Register (FSEC)

Bits	7	6	5	4	3	2	1	0
Field	SPROT7	SPROT6	SPROT5	SPROT4	SPROT3	SPROT2	SPROT1	SPROT0
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank F, Register address 02H							

Bit Position	Value	Description
[7:0]		**SPROT7-SPROT0**—Sector Protection Each bit corresponds to an 16-page Flash sector. For the ZLF645xxxxx64, all bits are used. Only bits 3-0 are used in the ZLF645xxxxx32. For ICP initiated operations, no sector protection exists.

Flash Frequency High and Low Byte Registers

The Flash Frequency High and Low Byte registers (Table 37 and Table 38) combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash frequency value must contain the system clock frequency (in kHz) and is calculated using the following equation:

$$FFREQ[15:0] = \{FFREQH[7:0], FFREQL[7:0]\} = \frac{\text{System Clock Frequency (Hz)}}{1000}$$

Programming the Flash Frequency High and Low Byte Registers as per the formula provides a Flash programming time of approximately 30 µs and an erase time of approximately 10 ms.

Caution: *Flash programming and erasure is not supported for system clock frequencies below 1 MHz or above 8 MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure proper operation of the device.*

Architecture

The UARTs consist of three primary functional blocks: **transmitter**, **receiver**, and **Baud Rate Generator**. The UART transmitter and receiver function independently, but employ the same baud rate and data format. Figure 22 displays the UART architecture.

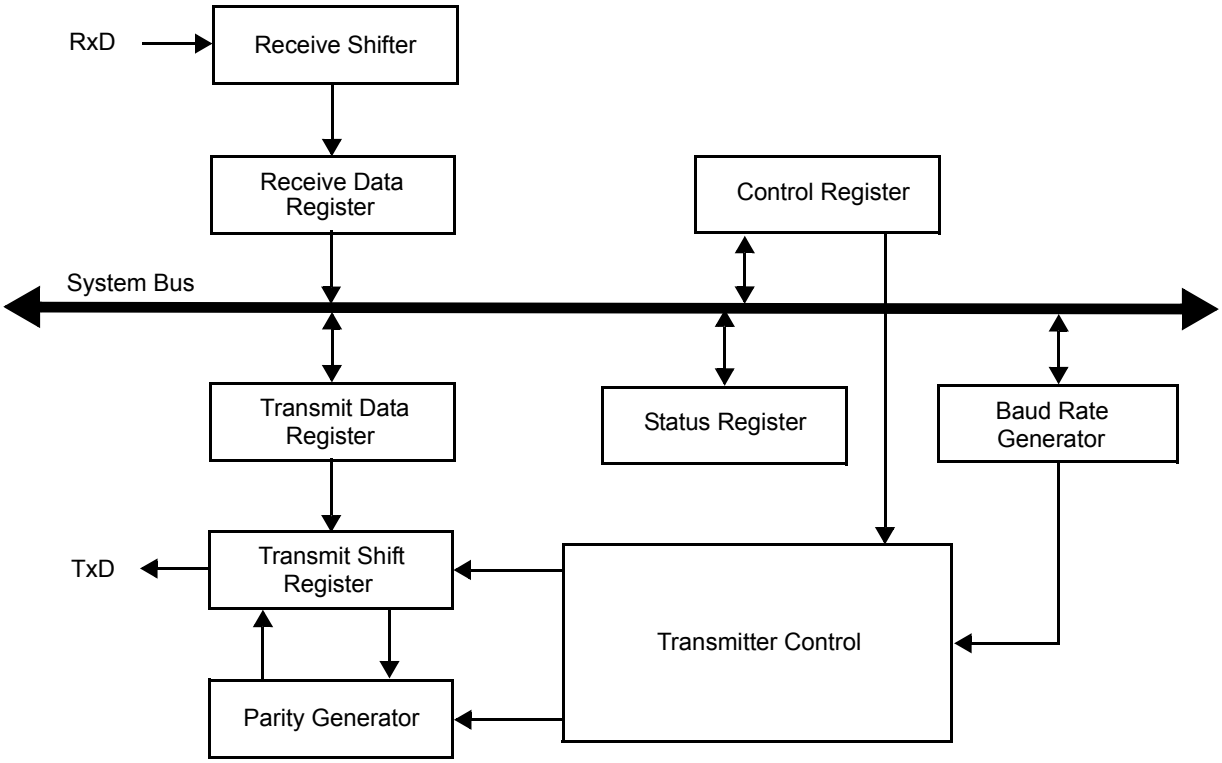


Figure 22. UART Block Diagram

Operation

The UART channel can be used to communicate with a master microprocessor or a slave microprocessor, both of which exhibit transmit and receive functionality. You can either operate the UART channel by polling the UART Status register or via interrupts. The UART remains active during HALT mode. If neither the transmitter nor the receiver is enabled, the UART baud rate generator can be used as an additional timer. The UART contains a noise filter for the receiver that can be enabled by the user.

4. Check the Transmit Status register bit, UST[2], to determine if the Transmit Data register is empty (indicated by 1). If empty, continue to Step 6. If the Transmit Data register is full (indicated by 0), continue to monitor the UST[2] bit until the Transmit Data register is available to receive new data.
5. Write the data byte to the UART Transmit Data register, `0F1h`. The transmitter automatically transfers the data to the internal transmit shift register and transmits the data.
6. To transmit additional bytes, return to Step 4.
7. Before disabling the transmitter, read the transmit completion status bit, UST[1]. If UST[1]=0, continue to monitor the bit until it changes to 1, which indicates that all data in the Transmit Data and internal shift registers has been transmitted.

Caution: *Data written while the transmit enable bit is clear (UCTL[7]=0) will not be transmitted. Data written while the transmit data status bit is clear (UST[2]=0) overwrites the previous value written, so the previous written value will not be transmitted. Disabling the UART transmitter while the transmit completion status bit is clear (UST[1]=0) can corrupt the byte being transmitted.*

Transmitting Data Using Interrupt-Driven Method

The UART transmitter interrupt indicates the availability of the Transmit Data register to accept new data for transmission.

Follow the steps below to configure the UART for interrupt-driven data transmission:

1. Write to the BCNST register to set the appropriate baud rate.
2. Write 0 to bit 6 of the P01M register.
3. Execute DI instruction to disable interrupts.
4. Write to the Interrupt Control registers to enable the UART Transmitter interrupt and set the appropriate priority.
5. Write to the UART Control register to:
   (a) Set the transmit enable bit (UCTL bit 7) to enable the UART for data transmission.
   (b) Enable parity, if appropriate, and select either even- or odd-parity.
6. Execute an EI instruction to enable interrupts as the transmit buffer is empty, an interrupt is immediately executed.
7. Write the data byte to the UART Transmit Data register. The transmitter automatically transfers the data to the Internal Transmit Shift register and transmits the data.
8. Execute the IRET instruction to return from the interrupt service routine (ISR) and wait for the Transmit Data register to again become empty.

Baud Rate Generator Interrupts

If the BRG interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This action allows the BRG to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate Constant register contains an 8-bit baud rate divisor value (BCNST[7:0]) that sets the data transmission rate (baud rate) of the UART. For programmed register values other than 00h, the UART data rate is calculated using the below equation:

$$\text{UART Data Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{\text{16 x UART Baud Rate Divisor Value (BCNST)}}$$

When the UART Baud Rate Low register is programmed to 00h, the UART data rate is calculated as follows:

$$\text{UART Data Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{4096}$$

When the UART Baud Rate Generator is used as a general-purpose counter, the counters time-out period can be computed as follows based upon the counters clock input being a divide by 16 of the system clock and the maximum count value being 255:

$$\text{Time-Out Period (us)} = \frac{\text{16 x UART Baud Rate Divisor Value (BCNST)}}{\text{System Clock Frequency (MHz)}}$$

Note: *The relationship between the XTAL1 clock frequency and the system clock frequency must be considered before making this computation and is dependent upon the programming of bit 2 of User Option Byte 1 as well as the programming of bit 0 of the SMR register. Depending on the programmed values, the system clock frequency can be a divide by 1, a divide by 2, or a divide by 16 of the XTAL1 clock.*

When the UART is disabled, the BRG can function as a basic 8-bit timer with interrupt on time-out.

Follow the steps below to configure the BRG as a timer with interrupt on time-out:

1. Disable the UART by clearing the receive and transmit enable bits, UCTL[7:6] to 0.
2. Load the appropriate 8-bit count value into the UART Baud Rate Generator Constant register. The count frequency is the system clock frequency (in Hz) divided by 16.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the Baud Rate Generator bit (UCTL bit 0) in the UART Control register to 1. When configured as an 8-bit timer, the count value, instead of the reload value, is read, and the counter begins counting down from its initial programmed value. On timing out (reaching a value of 1), if the time-out interrupt is enabled, an interrupt will be produced. The counter will then reload its programmed start value and begin counting down again.

Table 42 lists a number of BCNST register settings at various baud rates and system clock frequencies.

Table 42. BCNST Register Settings Examples

Target UART Data Rate (baud)	System Clock = 4 MHz, Crystal Clock = 8 MHz	System Clock = 3 MHz, Crystal Clock = 6 MHz
2400	BCNST = 01101000 Actual baud rate = 2403	BCNST = 01001110 Actual baud rate = 2403
4800	BCNST = 00110100 Actual baud rate = 4807	BCNST = 00100111 Actual baud rate = 4807
9600	BCNST = 00011010 Actual baud rate = 9615	BCNST = 00010100 Actual baud rate = 9375
19200	BCNST = 00001101 Actual baud rate = 19230	BCNST = 00001010 Actual baud rate = 18750

Caution: *Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to* FFFEh. *Transition from 0 to* FFFFh *is not a time-out condition.*

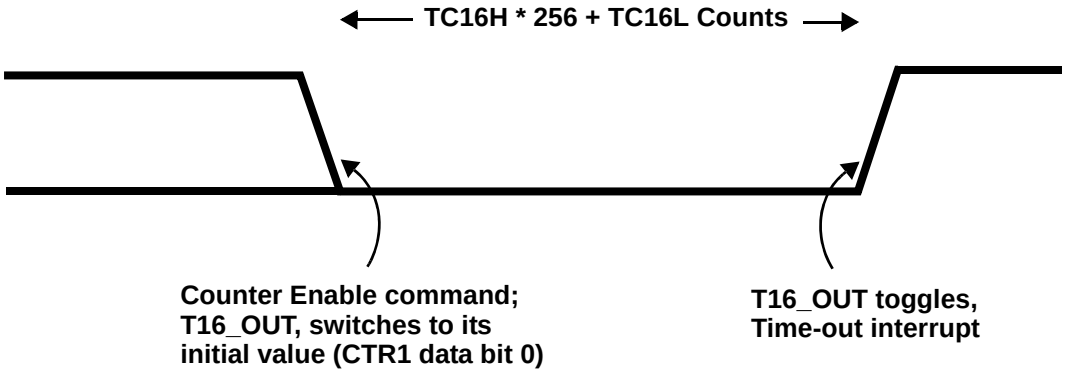


Figure 36. T16_OUT in SINGLE-PASS Mode

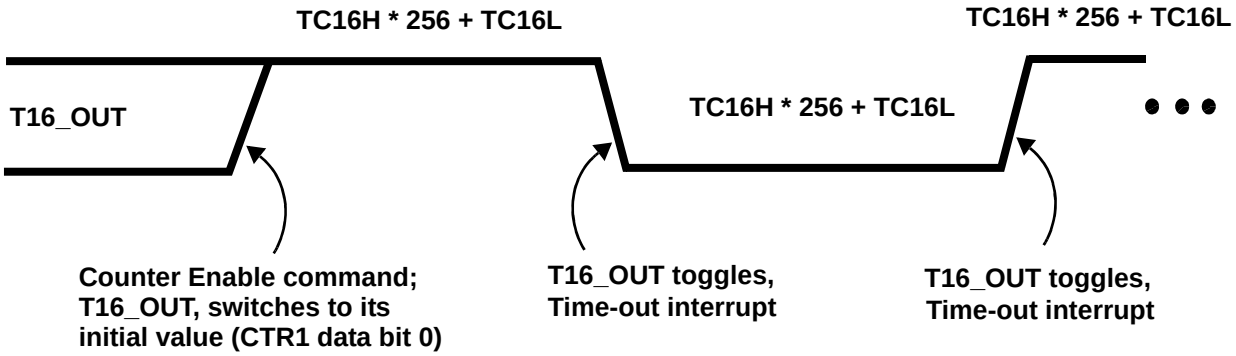


Figure 37. T16_OUT in MODULO-N Mode

T16 DEMODULATION Mode

You must program TC16L and TC16H to FFh. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 bits [5:4]) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

Counter/Timer 16 Low Hold Register

The Counter/Timer 16 Low Hold register (see Table 53) contains the low byte of the value loaded into the T16 timer.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 53. Counter/Timer 16 Low Hold Register (TC16L)

Bit	7	6	5	4	3	2	1	0
Field	T16_Data_LO							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank D: 06h; Linear: D06h							

Bit Position	Value	Description
[7:0]	0hh–FFh	**T16_Data_LO**—Read/Write Data.

Counter/Timer 8 High Hold Register

The Counter/Timer 8 High Hold register (see Table 54) contains the value to be counted while the T8 output is 1.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 54. Counter/Timer 8 High Hold Register (TC8H)

Bit	7	6	5	4	3	2	1	0
Field	T8_Level_HI							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank D: 05h; Linear: D05h							

Bit Position	Value	Description
[7:0]	0hh–FFh	**T8_Level_HI**—Read/Write Data.

Bit Position	Value	Description
[7]		**T8_Enable—**Disable/enable the T8 counter. (Note: This register bit duplicates the function of register bit 6 of the CTR3 register).
	0	Disables the T8 counter if bit 6 of the CTR3 register is also 0.
	1	Enables the T8 counter if bit 6 of the CTR3 register is also 0 and has no effect if the T8 counter is already enabled by bit 6 of the CTR3 register being 1.
[6]		**SINGLE-PASS/MODULO-N**
	0	MODULO-N mode. Counter reloads the initial value when terminal count is reached.
	1	SINGLE-PASS mode. Counter stops when the terminal count is reached.
[5]		**Time_Out**—This bit is set when the T8 terminal count is reached.
	Read	
	0	No counter time-out occurred.
	1	Counter time-out occurred.
	Write	
	0	No effect.
	1	Reset flag to 0. Software must reset this flag before using counter/timers.
[4:3]		**T8 _Clock**—Select the T8 input clock frequency.These bits are not reset upon Stop Mode Recovery.
	00	SCLK
	01	SCLK ÷ 2
	10	SCLK ÷ 4
	11	SCLK ÷ 8
[2]		**Capture_INT_Mask**—Disable/enable interrupt when data is captured into either LO8 or HI8 on a positive or negative edge detection in DEMODULATION mode. This bit is not reset upon Stop Mode Recovery.
	0	Disable data capture interrupt.
	1	Enable data capture interrupt.
[1]		**Counter_INT_Mask**—Disable/enable T8 time-out interrupt. This bit is not reset upon Stop Mode Recovery.
	0	Disable time-out interrupt.
	1	Enable time-out interrupt.
[0]		**P34_Out**—Select normal I/O or T8 output function for Port 3, pin 4.
	0	P34 as port output.
	1	T8 output on P34.

T8 and T16 Common Functions Register

The T8 and T16 Common Functions register (CTR1) controls the functions in common with Timer 8 and Timer 16. Table 57 describes the bits for this register.

Note: *Be careful to differentiate TRANSMIT mode from DEMODULATION mode, as set by CTR1[7]. The functions of CTR1[6:0] and CTR2[6] are different depending on which mode is selected. Do not change from one mode to another without first disabling the counter/timers.*

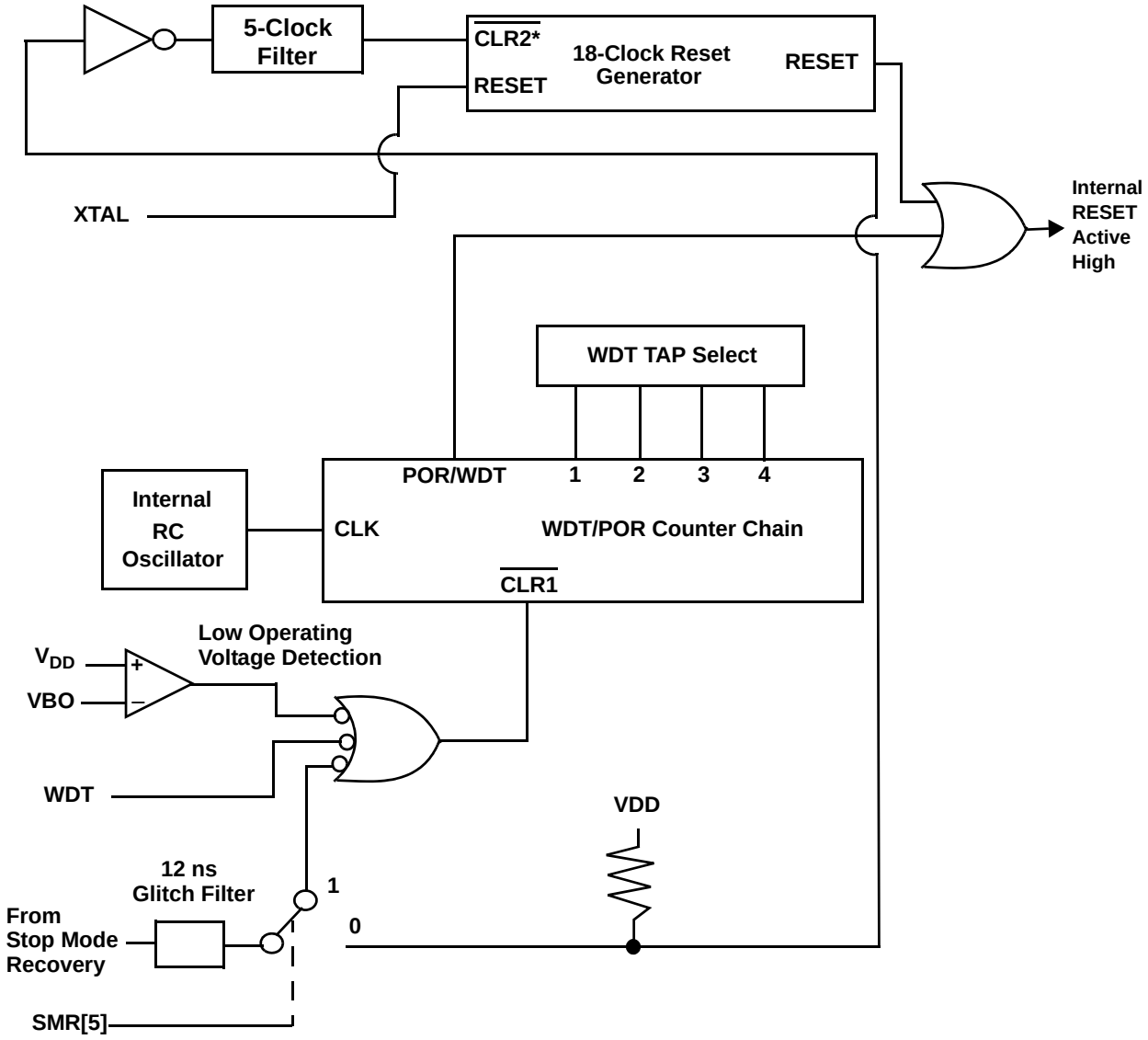
Table 57. Timer 8 and Timer 16 Common Functions Register (CTR1)

Bit	7	6	5	4	3	2	1	0
Field	Mode	P36 Out/ Demodulator Input	T8/T16 Logic/ Edge Detect		Transmit Submode/ Glitch Filter		Initial Timer 8 Out/ Rising Edge	Initial Timer 16 Out/ Falling Edge
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank D: 01h; Linear: D01h							

Bit Position	Value	Description
[7:0]		**Mode**—Selects the timer mode for signal transmission or demodulation.
	0	TRANSMIT mode.
	1	DEMODULATION mode.
[6]		**TRANSMIT Mode** P36 Out—Select normal I/O or timer output on Port 3, Pin 6.
	0	P36 acts as normal I/O port output.
	1	P36 acts as combined Timer 8/Timer 16 output.
		DEMODULATION Mode Demodulator Input—Select Port 2, Pin 0 or Port 3, Pin 1 as the counter/timer input.
	0	P31 acts as the demodulator input. If IMR[2] = 1, a P31 event can also generate an IRQ1 interrupt. To prevent this, clear IMR[2] or select P20 as input instead.
	1	P20 acts as the demodulator input.

Table 66. Reset and Power Management Registers (Continued)

Address (Hex)						
12-Bit	Bank	8-Bit	Register Description	Mnemonic	Reset	Page No
F0E	F	0E	Stop Mode Recovery Register 3	SMR3	X0h	155
F0F	F	0F	Watchdog Timer Mode Register	WDTMR	0000_1101b	142



*$\overline{\text{CLR1}}$ and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers, respectively, on a Low-to-High input transition.

Figure 43. Resets and Watchdog Timer

Table 72. Stop Mode Recovery Register 3 (SMR3)

Bit	7	6	5	4	3	2	1	0
Field	—				P33 SMR Select	P32 SMR Select	P31 SMR Select	P30 SMR Select
Reset	X	X	X	X	0	0	0	0
R/W	—	—	—	—	W	W	W	W
Address	Bank F: 0Eh; Linear: F0Eh							

Bit Position	Value	Description
[7:4]	—	**Reserved**—Reads undefined; Must be written to 1.
[3]	0 1	P33 not selected. P33 SMR source selected.
[2]	0 1	P32 not selected. P32 SMR source selected.
[1]	0 1	P31 not selected. P31 SMR source selected.
[0]	0 1	P30 not selected. P30 SMR source selected.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 81. Clock, Reset, Timers, and SMR Timing

No	Symbol	Parameter	V_{CC}	T_A = 0 °C to +70 °C 8.0 MHz		Units	WDTMR (Bits 6, 5, 4, 1, 0)
				Min	Max		
1	T_pC	Input Clock Period[1]	1.9–3.6	121	DC	ns	—
2	T_RC, T_FC	Clock Input Rise and Fall Times[1]	1.9–3.6	—	25	ns	—
3	T_WC	Input Clock Width[1]	1.9–3.6	37	—	ns	—
4	$T_WT_{IN}L$	Timer Input Low Width[1]	1.9	100	—	ns	—
			3.6	70	—	ns	—
5	$T_WT_{IN}H$	Timer Input High Width[1]	1.9–3.6	$3T_PC$	—	—	—
6	T_PT_{IN}	Timer Input Period[1]	1.9–3.6	$8T_PC$	—	—	—
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise and Fall Timers[1]	1.9–3.6	—	100	ns	—
8	T_WIL	Interrupt Request Low Time[1,2]	1.9	100	—	ns	—
			3.6	70	—	ns	—
9	T_WIH	Interrupt Request Input High Time[1,2]	1.9–3.6	$5T_PC$	—	—	—
10	T_{WSM}	Stop Mode Recovery Width Spec	1.9–3.6	12[3] 10 T_PC[4]	—	ns	—
11	T_{OST}	Oscillator Startup Time[4]	1.9–3.6	—	$5T_PC$	—	—
12	T_{WDT}	Watchdog Timer Delay Time	1.9–3.6	5	—	ms	0, 0, 0, 0, 0
			1.9–3.6	10	—	ms	0, 0, 0, 0, 1
			1.9–3.6	20	—	ms	0, 0, 0, 1, 0
			1.9–3.6	80	—	ms	0, 0, 0, 1, 1
			1.9–3.6	320	—	ms	0, 0, 1, X, X
			1.9–3.6	1, 280	—	ms	0, 1, 0, X, X
			1.9–3.6	5, 120	—	ms	1, 0, 0, X, X

timer/counter circuit 113
timer/counter configuration 27
overline, in text 3
overrun, UART 91

P

package diagram 176, 177, 178, 179, 180, 181, 182, 183
package information 176
parity, UART data 87
pin description 5
pin function
port 0 20
port 2 21, 28
port 3 23
port 3 summary 26
ping-pong mode 111, 112
pins
20-pin package 6, 8, 9
28-pin package 11, 13, 16
polled UART receive 89
polled UART transmit 87
port 0
configuration 20
pin function 20
Port 0 Mode Register (P01M) 31
Port 0 Register (P0) 32
port 2
configuration 22
pin function 21, 28
Port 2 Mode Register (P2M) 34, 39
Port 2 Register (P2) 33, 35, 40
port 3
configuration 24
counter/timer output 27
pin function 23
pin function 26
Port 3 Mode Register (P3M) 36
Port 3 Register (P3) 37
Port Configuration Register (PCON) 28, 30
power connection 3
power management 137
power-on reset timer 139
program memory
map 41
programming summary 157

R

ratings, maximum 163
register
BCNST 98
CTR1 121
CTR3 126
flash high and low byte (FFREQH and FREEQL) 79
flash page select (FPS) 77, 78
flash status (FSTAT) 77
HI16 115
HI8 114
ICP control 64
ICP status 65
IMR 133
IPR 130
IRQ 130, 131
LO16 116
LO8 115
LVD 140
P0 32
P01M 31
P2 33, 35, 40
P2M 34, 39
P3 37
P3M 36
PCON 28, 30
Register Pointer register 48
RP 48
SMR 146
SMR1 150
SMR2 152
SMR3 155
SMR4 156
SPL 48, 49
UCTL 96, 97
URDATA 95
USER 48
UST 95

Customer Support

For any comments, detail technical questions, or reporting problems, please visit Maxim's Technical Support at https://support.maxim-ic.com/micro.