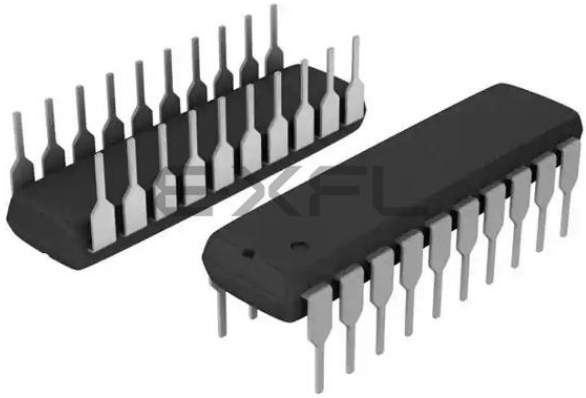
Analog Devices Inc./Maxim Integrated - ZLF645E0P2064G Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8 LXMC
Core Size	8-Bit
Speed	8MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.9V ~ 3.6V
Data Converters	-
Oscillator Type	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlf645e0p2064g

Table 5 lists the function and signal directions of each pin within the 20-pin PDIP, SOIC, and SSOP packages sequentially by pin number.

Table 5. 20-Pin PDIP/SOIC/SSOP Sequential Pin Identification

Pin No	Symbol	Function	Signal Direction
1	P25	Port 2, bit 5	Input/Output
2	P26	Port 2, bit 6	Input/Output
3	P27	Port 2, bit 7	Input/Output
4	P07	Port 0, bit 7	Input/Output
5	V_{DD}	Power Supply	Input
6	XTAL2	Crystal oscillator	Output
7	XTAL1	Crystal oscillator	Input
8	P31	Port 3, bit 1	Input
9	P32	Port 3, bit 2	Input
10	P33	Port 3, bit 3	Input
11	P34	Port 3, bit 4	Input/Output
12	P36	Port 3, bit 6	Output
13	P00	Port 0, bit 0	Input/Output
	P30	Port 3, bit 0	Input
14	P01	Port 0, bit 1	Input/Output
15	V_{SS}	Ground In	put
16	P20	Port 2, bit 0	Input/Output
17	P21	Port 2, bit 1	Input/Output
18	P22	Port 2, bit 2	Input/Output
19	P23	Port 2, bit 3	Input/Output
20	P24	Port 2, bit 4	Input/Output

Note: When the Port 0 low-nibble pull-up option is enabled and the P30 input is Low, current flows through the pull-up to Ground.

Table 12. Summary of Port 3 Pin Functions

Pin	I/O	In-Circuit Programmer	Counter/Timers	Comparator	Interrupt	IRAMP	UART
P30	IN			REF1			
P31	IN		IN	AN1	IRQ2	IR1	
P32	IN			AN2	IRQ0		UART Rx
P33	IN			REF2	IRQ1		
P34	IN/OUT	ICP	T8	AO1		IROUT	
P35	OUT		T16				
P36	OUT T8/T16						
P37	OUT			AO2			

Port 3 also provides output for each of the counter/timers and AND/OR Logic (see Figure 10). Control is performed by programming CTR1 bit 5 and bit 4, CTR0 bit 0, and CTR2 bit 0.

Table 28. In-Circuit Programmer Commands (Continued)

ICP Command	Command Byte	Enabled when NOT in FLASH CONTROL mode?	Disabled by Flash Read/Write Protect Option Bits (FLRWP and/or FLPROT1)
Read Flash Controller Registers	09H	No	—
Write Flash Memory	0AH	No	If FLRWP enabled, command is disabled for entire Flash main memory and page 3 of the Information Area. If FLPROT1 enabled, command disabled for page 3 of the Information Area and lower half of main memory only.
Read Flash Memory	0BH	No	If FLRWP enabled, command is disabled for the Flash main memory. If FLPROT1 enabled, command disabled for the lower half of main memory only.
Reserved	0CH – 0DH	—	Disabled
Read Program Memory CRC	0EH	No	—
Reserved	0FH –1AH	—	—
Read ICP Autobaud Register	1BH	Yes	—
Reserved	1CH – EFH	—	—
Write Test Mode Register	F0H	Yes	—
Read Test Mode Register	F1H	Yes	—
Reserved	F2H – FFH	—	—

In the following bulleted list of ICP commands, data and commands sent from the host to the ICP are identified by '`ICP ← Command/Data`'. Data sent from the ICP back to the host is identified by '`ICP → Data`':

- **Read ICP Revision (00H)**—The Read ICP Revision command determines the version of the ICP. If ICP commands are added, removed, or changed, the revision number changes.

```
ICP ← 00H
ICP → ICPRev[15:8] (Major revision number)
ICP → ICPRev[7:0] (Minor revision number)
```

for the command will default to the maximum memory size. The on-chip Flash Controller must be written to and unlocked for the programming operation to occur. If the Flash Controller is not unlocked, the data is discarded. Also, data is discarded for writes to protected areas of the Flash's main or information Page 3 areas based upon the settings of the read/write protect option bits in User Option Byte 1 (OPT1) register.

```
ICP ← 0AH
ICP ← Flash Memory Address[15:8]
ICP ← Flash Memory Address[7:0]
ICP ← Size[15:8]
ICP ← Size[7:0]
ICP ← 1-memsize data bytes
```

- **Read Flash Memory (0BH)**—The Read Flash Memory command is used to read data from the Flash's main memory area or Information Area. This command is equivalent to the CPU reading the memory through the LDC and LDCI instructions. Data can be read 1 to 'memsize' bytes at a time where `memsize` represents the size (32 KB or 64 KB) of the Flash memory for the product option chosen (The `memsize` number of bytes can be written by setting the size to 0). Depending on the settings of the read/write protect option bits in User Option Byte 1 register, reads to protected areas of the Flash's main memory area will return `FFH` for the data.

  ```
  ICP ← 0BH
  ICP ← Flash Memory Address[15:8]
  ICP ← Flash Memory Address[7:0]
  ICP ← Size[15:8]
  ICP ← Size[7:0]
  ICP → 1-65536 data bytes
  ```

- **Read Flash Main Memory CRC (0EH)**—The Read Flash Main Memory CRC command computes and returns the Cyclic Redundancy Check (CRC) of the Flash's Main Memory using the 16-bit CRC-CCITT polynomial. If the device is not in ICP mode, this command returns `FFFFH` for the CRC value. Unlike most other ICP Read commands, there is a delay from issuing of the command until the ICP returns the data. The ICP reads the Main Memory, calculates the CRC value, and returns the result. The delay is a function of the Flash main memory size and is approximately equal to the system clock period multiplied by the number of bytes in the Flash main memory.

  ```
  ICP ← 0EH
  ICP → CRC[15:8]
  ICP → CRC[7:0]
  ```

- **Read ICP Autobaud Register (1BH)**— The Read ICP Autobaud register command reads the 12-bit ICP autobaud value set during autobaud detection.

  ```
  ICP ← 1BH
  ICP → (4'b0000, Autobaud[11:8])
  ```

3. The CPU writes to the Page Select (PGS) register.

Figure 20 displays the basic Flash Controller operation considering code based CPU Flash accesses and based upon the programming of the Flash Controllers Flash Control (FCTL), Sector Protect (FSEC), and Page Select (FPS) Registers. As mentioned previously for ICP based Flash accesses, the only modification to Figure 20 is that the programming of the Sector Protect (FSEC) register is ignored and the ICP has programming and erase access to a page independent of whether it resides in a protected sector. Figure 20 does not display the effects of the Flash read/write protect bits of User Option byte 1.

If either of these bits is enabled, their function takes priority over the operation description displayed in Figure 20 in terms of when a page erase or byte programming access is allowed (for more details, see Flash Code Protection Against External Access on page 73).

Flash Status Register

The Flash Status (FSTAT) register (see Table 34) indicates the current state of the Flash Controller. This register can be read any time. The read-only Flash Status (FSTAT) register shares its Register File address with the Write-only Flash Control (FCTL) register.

Table 34. Flash Status Register (FSTAT)

Bits	7	6	5	4	3	2	1	0
Field	Reserved		FSTAT					
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	Bank F, Register address: 01H							

Bit Position	Value	Description
[7:6]	—	**Reserved**—Reads as 0's.
[5:0]		**FSTAT**—Flash Controller Status
	000000	Flash Controller locked.
	000001	First unlock command received (73H written).
	000010	Second unlock command received (8CH written).
	000011	Flash Controller unlocked.
	000100	Sector protect register selected.
	001xxx	Program operation in progress.
	010xxx	Page erase operation in progress.
	100xxx	Mass erase operation in progress.

Flash Page Select Register

The Flash Page Select (FPS) register (see Table 35) shares address space with the Flash Sector Protect (FSEC) register. Unless the Flash Controller is in 'locked' state and its Flash Control (FCTL) register is written with 5EH, writes to this address target the Flash Page Select (FPS) register.

The FPS register is used to select one page within the Flash Main Memory or Information Block for programming or erasure depending upon whether its IFEN bit is 0 or 1 respectively. Each Flash Main Memory Page contains 512 bytes of Flash memory. During a Page Erase operation to the Main Memory, the page that will be erased is the one containing the 512 Flash memory locations where bits 15 through 9 of their addresses is equal to bits 6 through 0 of FPS register. For Main Memory programming operations, bits 15 through 9 of the address to be programmed must equal bits 6 through 0 of the FPS register for the Flash Controller to execute the operation. For page erase or programming operations to the Flash's Information Block as indicated by the IFEN bit being 1, the programming or

UART Receive Data Register/UART Transmit Data Register

The UART Receive/Transmit Data register (see Table 43) is used to send and retrieve data from the UART channel. When the UART receives a data byte, it can be read from this register. The UART receive interrupt is cleared when this register is used. Data written to this register is transmitted by the UART.

Table 43. UART Receive/Transmit Data Register (URDATA/UTDATA)

Bit	7	6	5	4	3	2	1	0
Field	UART Receive/Transmit							
Reset	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank Independent: F1h; Linear: 0F1h							

Bit Position	Description
[7:0]	**UART Receive/Transmit** When read, returns received data. When written, transmits written data.

UART Status Register

The UART Status register (see Table 44) displays the status of the UART. Bits [6:3] are cleared by reading the UART Receive/Transmit register (F1h).

Table 44. UART Status Register (UST)

Bit	7	6	5	4	3	2	1	0
Field	Receive Status	Parity Error	Overrun Error	Framing Error	Break	Transmit Data	Transmit Complete	Noise Filter
Reset	0	0	0	0	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank Independent: F2h; Linear: 0F2h							

Bit Position	Value	Description
[7]		**Receive Status**—Set when data is received; cleared when URDATA is read.
	0	UART Receive Data register empty.
	1	UART Receive Data register full.

The system clock is usually the crystal clock divided by 2. When the UART baud rate generator is used as an additional timer, a Read from this register returns the actual value of the count of the BRG in progress and not the reload value. See Table 46.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 46. UART Baud Rate Generator Constant Register (BCNST)

Bit	7	6	5	4	3	2	1	0
Field	Baud Rate Generator Constant							
Reset	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank Independent: F4h; Linear: 0F4h							

Bit Position	Description
[7:0]	**Baud Rate Generator Constant** When read, returns the actual timer count value (when UCTL[0]=1). When written, sets the Baud Rate Generator Constant. The actual baud rate frequency = XTAL ÷ (32 x BCNST).

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, bit 1). If the initial value (CTR1, bit 1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter.

In SINGLE-PASS mode (CTR0, bit 6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0, bit 5) is set, and a time-out interrupt can be generated if it is enabled (CTR0, bit 1).

In MODULO-N mode, on reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the time-out status bit (CTR0, bit 5), thereby generating an interrupt if enabled (CTR0, bit 1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 29.

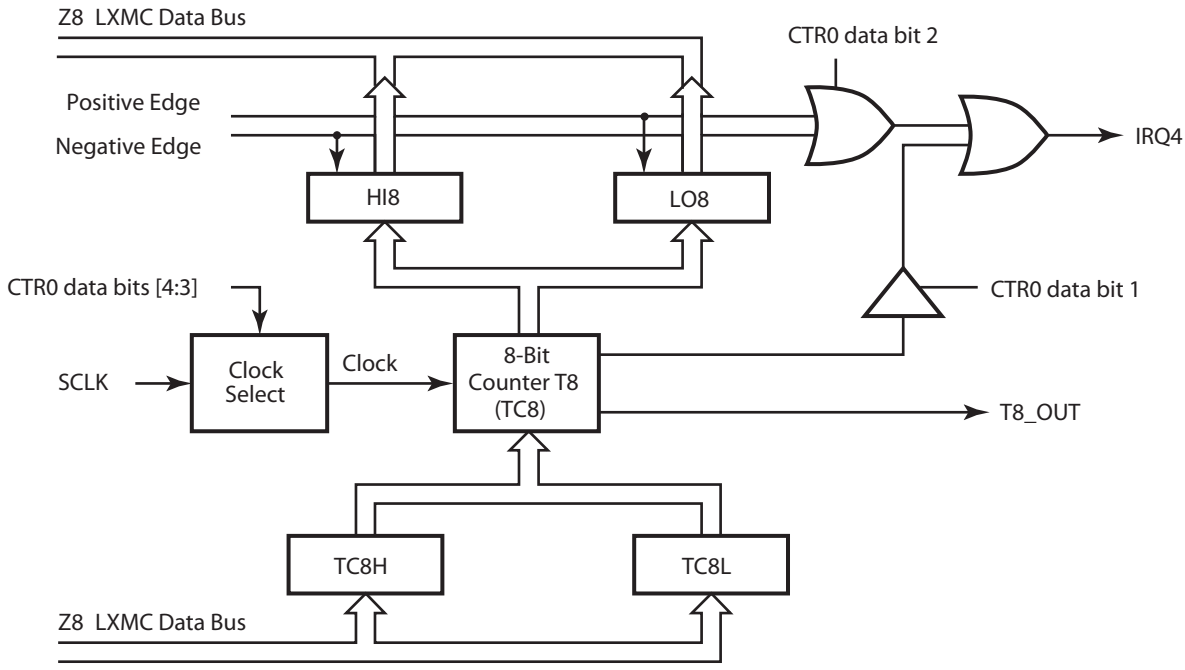

Figure 29. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Caution: *An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFh to FEh.*

T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 bits [5:4]) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 bits [5:4]) is detected during counting, the current value of T8 is complemented and put into one of the capture registers.

If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, bits [1:0]) is set, and an interrupt can be generated if enabled (CTR0, bit 2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, bit 5) is set, and an interrupt can be generated if enabled (CTR0, bit 1). T8 then continues counting from FFh(see Figure 32 on page 106).

Table 61. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location (Program Memory)	Comments
IRQ0	P32, UART Rx	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33, UART Tx, BRG, SMR Event	2, 3	External (P33), Falling Edge Triggered
IRQ2	P31	4, 5	External (P31), Rising, Falling Edge Triggered
IRQ3	Timer 16	6, 7	Internal
IRQ4	Timer 8	8, 9	Internal
IRQ5	Low-Voltage Detection	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the Program Memory vector location reserved for that interrupt.

All ZLF645 MCU interrupts are vectored through locations in the Program Memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request Register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are user-programmable. The software can poll to identify the state of the pin.

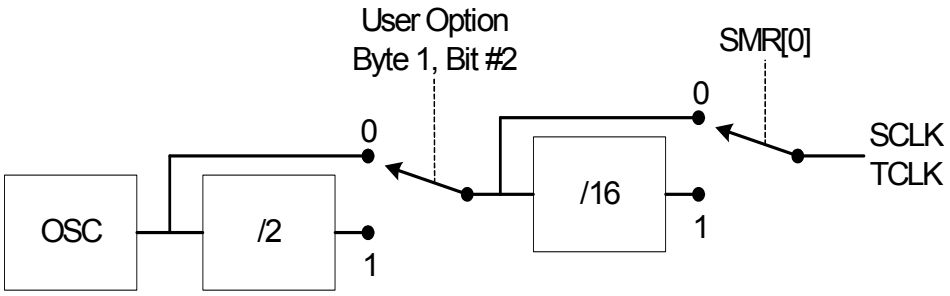

Figure 42. SCLK/TCLK Circuit

Voltage Brownout Standby

An on-chip voltage comparator circuit (VBO) checks that the V_{DD} is at the required level for correct operation of the device in terms of Flash memory reads. A second on-chip comparator circuit (subVBO) checks that the V_{DD} level is high enough for proper operation of the VBO circuit. If the V_{DD} level drops below the VBO trip point, the ZLF645 will be held in a reset state as long as V_{DD} remains below this trip point value, and the XTAL1 and XTAL2 oscillator circuitry will be disabled thereby stopping the clock input to the ZLF645 and saving power. If the V_{DD} level continues to drop below the subVBO trip point, the ZLF645 will remain in a reset state and the VBO comparator circuit will be disabled for further power savings. When the power level returns to a value above the VBO trip point, the device performs a power-on reset and functions normally.

STOP Mode

`STOP` instruction turns OFF the internal clock and external crystal oscillation, thus reducing the MCU supply current to a very low level. For STOP mode current specifications, see Table 80 on page 165.

To enter STOP mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP instruction (OpCode = `FFh`) immediately before the appropriate sleep instruction, as given below:

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP mode
```

STOP mode is terminated only by a reset, such as WDT time-out, POR, or one of the Stop Mode Recovery events as described in Stop Mode Recovery Event Sources on page 144. This condition causes the processor to restart the application program at address `000Ch`.

Unlike a normal POR or WDT reset, a Stop Mode Recovery reset does not reset the contents of some registers and bits. Register bits not reset by a Stop Mode Recovery are highlighted in grey in the register tables. Register bit SMR[7] is set to 1 by a Stop Mode Recovery.

HALT Mode

`HALT` instruction turns off the internal CPU clock, but not the XTAL oscillation.
The counter/timers, UART, and interrupts (IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5) remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after HALT mode.

AC Characteristics

Figure 49 and Table 81 lists the alternating current (AC) characteristics of ZLF645 Flash MCU.

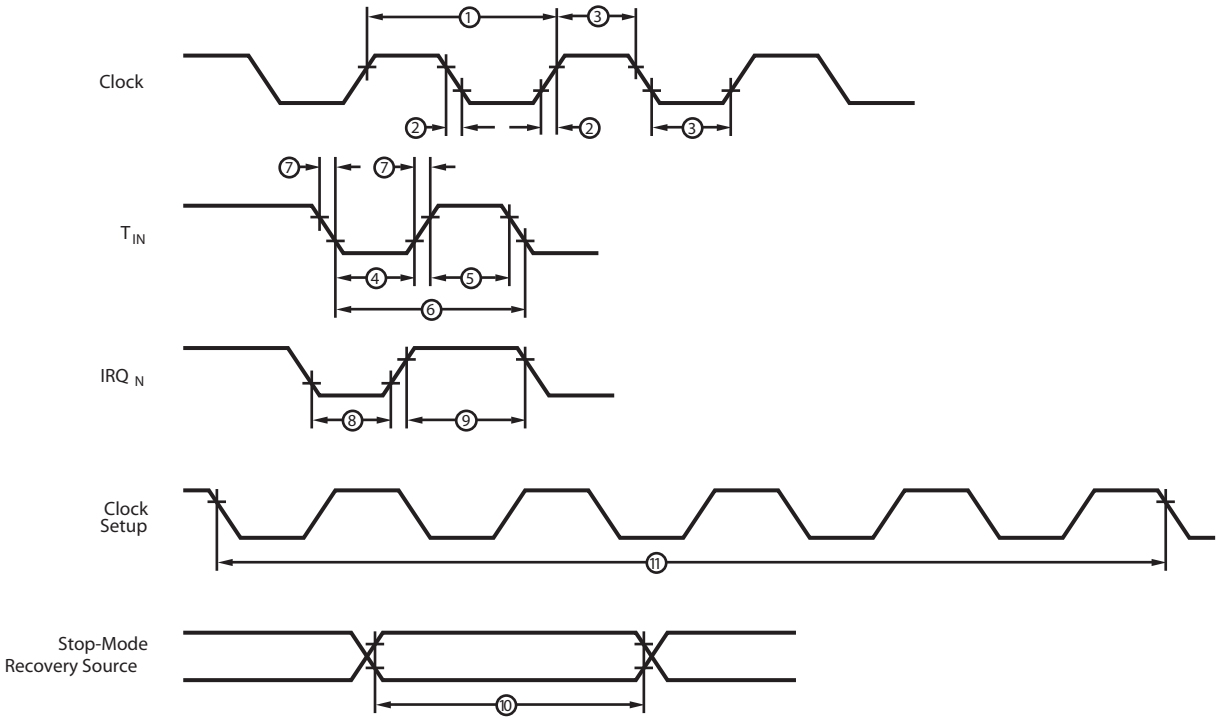

Figure 49. AC Timing Diagram

Flash Option Bits

Programmable Flash Option Bits allow user configuration of certain aspects of ZLF645 MCU functionality. This configuration data is stored in the Flash memory Information Block and then read into option byte shadow registers during the last portion of the ZLF645 MCUs reset period.

Features available for control through the Flash Option Bits include:

- Port 0 low nibble pull-ups
- Port 0 high nibble pull-ups
- Port 1 low nibble pull-ups
- Port 1 high nibble pull-ups
- Port 2 pull-ups
- Port 3 low nibble pull-ups
- Port 4 pull-ups
- WDT always enabled
- Flash protect entire main memory
- Flash protect lower half main memory
- XTAL1 to System Clock (no division enable)
- 16-bit Stack addressiblity enable

Operation

Option Bit Shadow Register Loading By Reset

For each Flash memory option bit, there is an associated option bit shadow register that is used to register the value of the option bit. The output of the option bit shadow registers are used by the ZLF645 MCU to enable various features and functions for the ZLF645 MCU. Each time the Flash Memory Information Block Option Bits are programmed or erased, the device must be reset for the change in ZLF645 configuration to take effect.

A POR or Stop Mode Recovery Reset with SMR bit 5 set to 1, loads the option bits from the Flash memory to the Option Bit Shadow registers during the last few clock cycles of the reset period. In some cases, in order to provide a required value before being loaded, the Option Bit Shadow registers are reset to a predefined value on the start of the reset period.

Index

Numerics

A

B

C

P

R

S

T

U

V

W

X

Z